Nov. 30, 2007

Preliminary

10G 850nm SFP+ Transceiver

(With monitor function, up to 300m transmission)

Members of Flexon™ Family

Features

- Support 10GE application at the data rate 9.95Gbps and 10.3125Gbps
- Up to 300m transmission distance on 50μm MMF (2000MHz.km)
- 850nm high-speed VCSEL and PIN receiver
- CDR included
- SFI electrical interface
- 2-wire interface for integrated Digital Diagnostic monitoring
- SFP+ MSA package with duplex LC connector
- Hot pluggable
- Very low EMI and excellent ESD protection
- Single +3.3V power supply
- Power consumption less than 1.0W
- Operating case temperature: 0~+70°C

Applications

- 10GBASE-SR at 10.3125Gbps
- 10GBASE-SW at 9.953Gbps
- Other optical links

Standard

- Compliant with SFF-8431
- Compliant with SFF-8472 Rev 10.1
- Compliant with IEEE 802.3-2005 10GBASE-SR and 10GBASE-SW
- Compliant with FCC 47 CFR Part 15, Class B
- Compliant with FDA 21 CFR 1040.10 and 1040.11, Class I
- Compliant with Telcordia GR-468-CORE
- RoHS compliance

Description

FTM-811XC-L03DG is a high performance, cost effective module, which is optimized for 10G Ethernet, supporting data-rate of 10.3125Gbps (10GBASE-SR) or 9.953Gbps (10GBASE-SW), and transmission distance up to 300m on 50μm MMF (2000MHz.km).

The transceiver consists of two sections: The transmitter section incorporates an 850nm VCSEL, driver. The receiver section consists of a PIN photodiode integrated with a transimpedance preamplifier (TIA) and a CDR.

The module is hot pluggable into the 20-pin connector. The high-speed electrical interface is based on low voltage logic, with nominal 100 Ohms differential impedance and AC coupled in the module. The optical output can be disabled by LVTTL logic high-level input of TX_Disable. Loss of signal (RX_LOS) output is provided to indicate the loss of an input optical signal of receiver.

Regulatory Compliance

The transceivers are tested according to American and European product safety and electromagnetic compatibility regulations (See Table 1). For further information regarding regulatory certification, please refer to Fiberxon regulatory specification and safety guidelines, or contact with Fiberxon, Inc. America sales office listed at the end of the documentation.

Table 1- Regulatory Compliance

Feature	Standard	Performance
Electrostatic Discharge (ESD) to the Electrical Pins	MIL-STD-883E Method 3015.7	Class 1(>1000 V)
Electrostatic Discharge (ESD) to the Duplex LC Receptacle	IEC 61000-4-2 GR-1089-CORE	Compliant with standards
Electromagnetic Interference (EMI)	FCC Part 15 Class B EN55022 Class B (CISPR 22B) VCCI Class B	Compliant with standards
Immunity	IEC 61000-4-3	Compliant with standards
Laser Eye Safety	FDA 21CFR 1040.10 and 1040.11 EN60950, EN (IEC) 60825-1,2	Compliant with Class 1 laser product.
Component Recognition	UL and CSA	UL file E223705

Absolute Maximum Ratings

Stress in excess of the maximum absolute ratings can cause permanent damage to the module.

Table 2 - Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit
Storage Temperature	T_S	-40	+85	°C
Supply Voltage	V_{CC}	-0.5	4.0	V
Operating Relative Humidity	RH		85	%

Recommended Operating Conditions

Table 3 - Recommended Operating Conditions

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Operating Case Temperature	T_C	0		+70	°C	
Power Supply Voltage	V_{CC}	3.15	3.3	3.45		
Power Supply Current	I_{CC}		240	300	mA	
Power Dissipation	P_D		0.8	1.0	W	
Data Rate			10.3125		Gbps	

Optical Characteristics

Table 4 - Optical Characteristics

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Transmitter						
Operating Data Rate			10.3125		Gbps	
Centre Wavelength	λ_C	840		860	nm	
Average Output Power	P_{0UT}	-7.3		-1.0	dBm	1
Extinction Ratio	ER	3.0			dB	2
Optical Modulation Amplitude	OMA	See Note 3			dBm	3
Spectral Width	$\Delta\lambda$	See Note 3			nm	3
Dispersion Penalty	DP			3.9	dB	
Optical Eye Mask	Compliant with IEEE 802.3-2005					
Receiver						
Operating Data Rate			10.3125		Gbps	
Centre Wavelength	λ_C	840		860	nm	
Receiver Sensitivity	P_{IN}			-9.9	dBm	4
Receiver Sensitivity in OMA	P_{IN}			-11.1	dBm	4
Receiver Totle Jitter	TJ			0.70	UI	
Receiver Determinstic Jitter	DJ			0.42	UI	
Receiver Overload	P_{IN}	-1.0			dBm	4
LOS Hysteresis		0.5		5	dB	
LOS Deassert	LOS_D			-13	dBm	
LOS Assert	LOS_A	-25			dBm	
Receiver Reflectance				-12	dB	

Notes:

1. The optical power is launched into MMF.
2. Measured with a PRBS 2^{31}-1 test pattern @10.3125Gbps.
3. Reference to Table 52-8 of IEEE 802.3-2005.
4. Measured with a PRBS 2^{31}-1 test pattern @10.3125Gbps, BER$\leqslant 10^{-12}$.

Electrical Characteristics

Table 5 - Electrical Characteristics

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
High-speed Signal (CML) Interface Specification						
Differential Data Input Amplitude		180		1200	mVpp	1
Input Differential Impedance		80	100	120	Ω	
Differential Data Output Amplitude		300		850	mVpp	1
Output Differential Impedance		80	100	120	Ω	
Low-speed Signal (LVTTL) Interface Specification						
Input High Voltage		2.0		3.3	V	
Input Low Voltage		GND		0.8	V	
Output High Voltage		2.4		3.3	V	
Output Low Voltage		GND		0.4	V	
2 Wire Serial Interface (LVTTL) Specification						
Clock Frequency	f_{SCL}			100	KHz	

Transmission Link Length

Table 6 – Transmission Link Length

Data Rate/Standard	Fiber Type	Modal Bandwidth @850 nm (MHz*Km)	Distance Range
10.3Gbps	62.5/125um MMF	160	2 to 26
	62.5/125um MMF	200	2 to 33
	50/125um MMF	400	2 to 66
	50/125um MMF	500	2 to 82
	50/125um MMF	2000	2 to 300

Notes:

Distances, shown in the Table are those specified for 10GBASE-SR/W, and for bandwidths not specified in this standard, the distances are calculated for worst case fiber and transceiver characteristics based on the optical and electrical specifications shown in this document using techniques utilized in IEEE 802.3-2005. In the nominal case, longer distances are achievable.

EEPROM Information.

EEPROM describing the transceiver's capabilities, standard interfaces, manufacturer, and other information, which is accessible over a 2 wire serial interface at the 8-bit address 1010000X (A0h). The memory contents refer to Table 7

Table 7 - Digital Diagnostic Memory Map

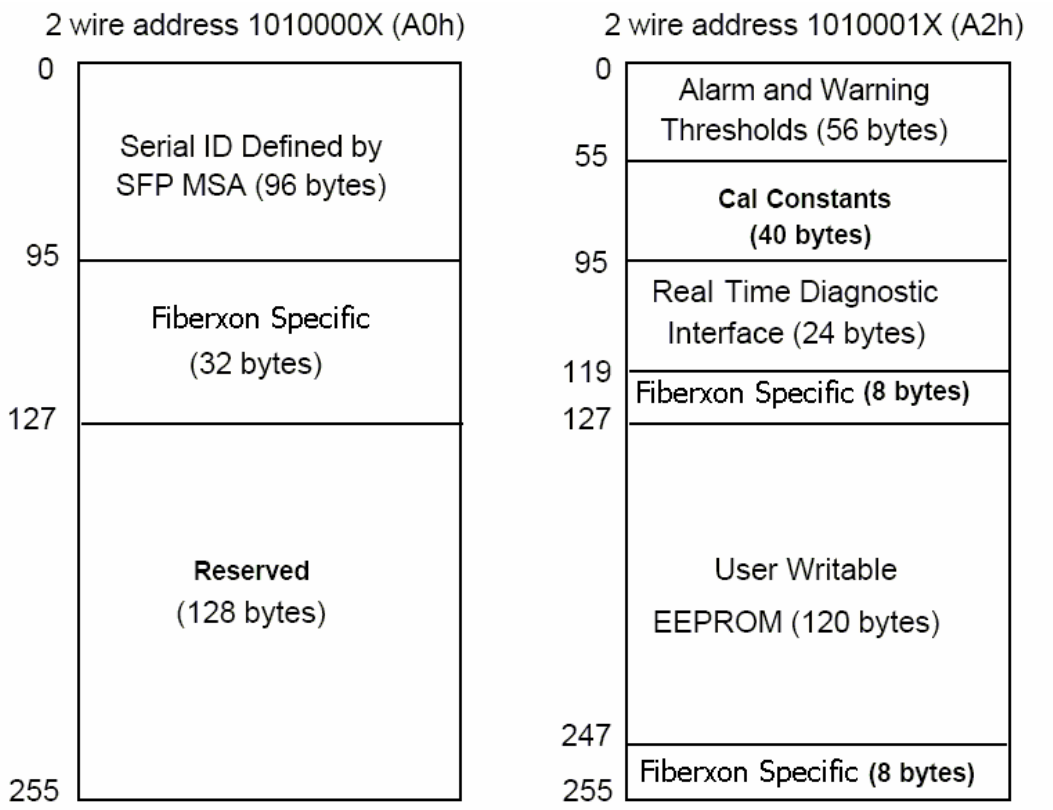


Table 8 - EEPROM Serial ID Memory Contents (A0h)

Addr.	(Bytes)	Name of Field	Hex	Description
0	1	Identifier	03	SFP
1	1	Ext. Identifier	04	SFP with Serial ID
2	1	Connector	07	LC
3-10	8	Transceiver	10 00 00 00 00 00 00 00	10GBASE-SR
11	1	Encoding	06	64B/66B
12	1	BR, nominal	67	10.3G
13	1	Rate identifier	00	unspecified
14	1	Length (9um)-km	00	
15	1	Length (9um)	00	
16	1	Length (50um,OM2)	08	82m of 50/125μm fiber (500MHz.km)
17	1	Length (62.5um,OM1)	03	33m of 62.5/125μm fiber (200MHz.km)
18	1	Length (copper)	00	

19	1	Length (50um, OM3)	1E	300m of OM3 fiber (2000MHz.km)
20-35	16	Vendor name	46 49 42 45 52 58 4F 4E 20 49 4E 43 2E 20 20 20	“FIBERXON INC. “(ASC Ⅱ)
36	1	Reserved	00	
37-39	3	Vendor OUI	00 00 00	
40-55	16	Vendor PN	46 54 4D 2D 38 31 31 58 43 2D 4C 30 33 44 47 20	“FTM-811XC-L03DG” (ASC Ⅱ)
56-59	4	Vendor rev	xx xx xx xx	ASC Ⅱ (“31 30 20 20” means 1.0 revision)
60-61	2	Wavelength	03 52	850nm
62	1	Reserved	00	
63	1	CC BASE	xx	Check sum of bytes 0-62
64-65	2	Options	00 1A	LOS, TX_FAULT and TX_DISABLE
66	1	BR, max	00	
67	1	BR, min	00	
68-83	16	Vendor SN	xx xx xx xx xx xx xx xx	ASC Ⅱ
84-91	8	Vendor date code	xx xx xx xx xx xx 20 20	Year (2 bytes), Month (2 bytes), Day (2 bytes)
92	1	Diagnostic type	68	Diagnostics (Int.Cal)
93	1	Enhanced option	F0	Alarm/warning flags, soft LOS, TX_FAULT and TX_DISABLE
94	1	SFF-8472	03	Diagnostics (SFF-8472 Rev 10.0)
95	1	CC_EXT	xx	Check sum of bytes 64-94
96-255	160	Fiberxon specific		Fiberxon specific EEPROM

Note: The “xx” byte should be filled in according to practical case.

Table 9 - EEPROM Diagnostics Data Map (A2h)

Addr.	(Bytes)	Name of Field	Description
0-1	2	Temp High Alarm	MSB at low address
2-3	2	Temp Low Alarm	MSB at low address
4-5	2	Temp High Warning	MSB at low address
6-7	2	Temp Low Warning	MSB at low address
8-9	2	Voltage High Alarm	MSB at low address
10-11	2	Voltage Low Alarm	MSB at low address
12-13	2	Voltage High Warning	MSB at low address
14-15	2	Voltage Low Warning	MSB at low address
16-17	2	Bias High Alarm	MSB at low address
18-19	2	Bias Low Alarm	MSB at low address
20-21	2	Bias High Warning	MSB at low address
22-23	2	Bias Low Warning	MSB at low address
24-25	2	TX Power High Alarm	MSB at low address
26-27	2	TX Power Low Alarm	MSB at low address
28-29	2	TX Power High Warning	MSB at low address
30-31	2	TX Power Low Warning	MSB at low address
32-33	2	RX Power High Alarm	MSB at low address
34-35	2	RX Power Low Alarm	MSB at low address
36-37	2	RX Power High Warning	MSB at low address
38-39	2	RX Power Low Warning	MSB at low address
40-55	16	Reserved	For future definition
56-59	4	Rx_PWR(4)	External calibration constant
60-63	4	Rx_PWR(3)	External calibration constant
64-67	4	Rx_PWR(2)	External calibration constant
68-71	4	Rx_PWR(1)	External calibration constant
72-75	4	Rx_PWR(0)	External calibration constant
76-77	2	Tx_I(Slope)	External calibration constant
78-79	2	Tx_I(Offset)	External calibration constant
80-81	2	Tx_PWR(Slope)	External calibration constant
82-83	2	Tx_PWR(Offset)	External calibration constant
84-85	2	T(Slope)	External calibration constant
86-87	2	T(Offset)	External calibration constant
88-89	2	V(Slope)	External calibration constant
90-91	2	V(Offset)	External calibration constant
92-94	3	Reserved	
95	1	Checksum	Low order 8 bits of sum from 0-94
96	1	Temperature MSB	Internal temperature AD values
97	1	Temperature LSB	

98	1	Vcc MSB	Internally measured supply voltage AD values
99	1	Vcc LSB	
100	1	TX Bias MSB	TX bias current AD values
101	1	TX Bias LSB	
102	1	TX Power MSB	Measured TX output power AD values
103	1	TX Power LSB	
104	1	RX Power MSB	Measured RX input power AD values
105	1	RX Power LSB	
106-109	4	Reserved	For future definition
110-7		TX Disable State	Digital state of Tx disable Pin
110-6		Soft TX Disable Control	Writing “1” disables laser, this is OR’d with Tx_Dissable pin
110-5		RS(1) State	Digital state of input pin RS(1) per SFF-8431
110-4		Rate Select State	Digital State of Rate Select Pin RS(0)
110-3		Soft Rate Select Control	
110-2		TX Fault State	Digital state
110-1		LOS State	Digital state
110-0		Data Ready State	Digital state; “1” until transceiver is ready
111	1	Reserved	Reserved
112-117	8	Optional alarm & warning flag bit	Refer to SFF-8472 rev 10.1
118	1	Extended module control/status	Refer to SFF-8472 rev 10.1
119	1	unallocated	
120-127	8	Vendor specific	Vendor specific
128-247	16	User/Customer EEPROM	Field writeable EEPROM
248-255	8	Vendor specific	Vendor specific

Recommended Host Board Power Supply Circuit

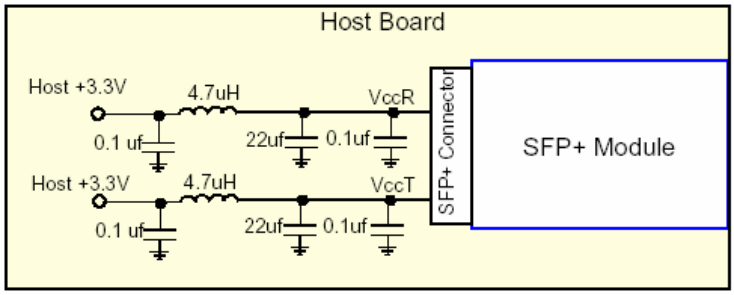


Figure 1, Recommended Host Board Power Supply Circuit

Recommended Interface Circuit

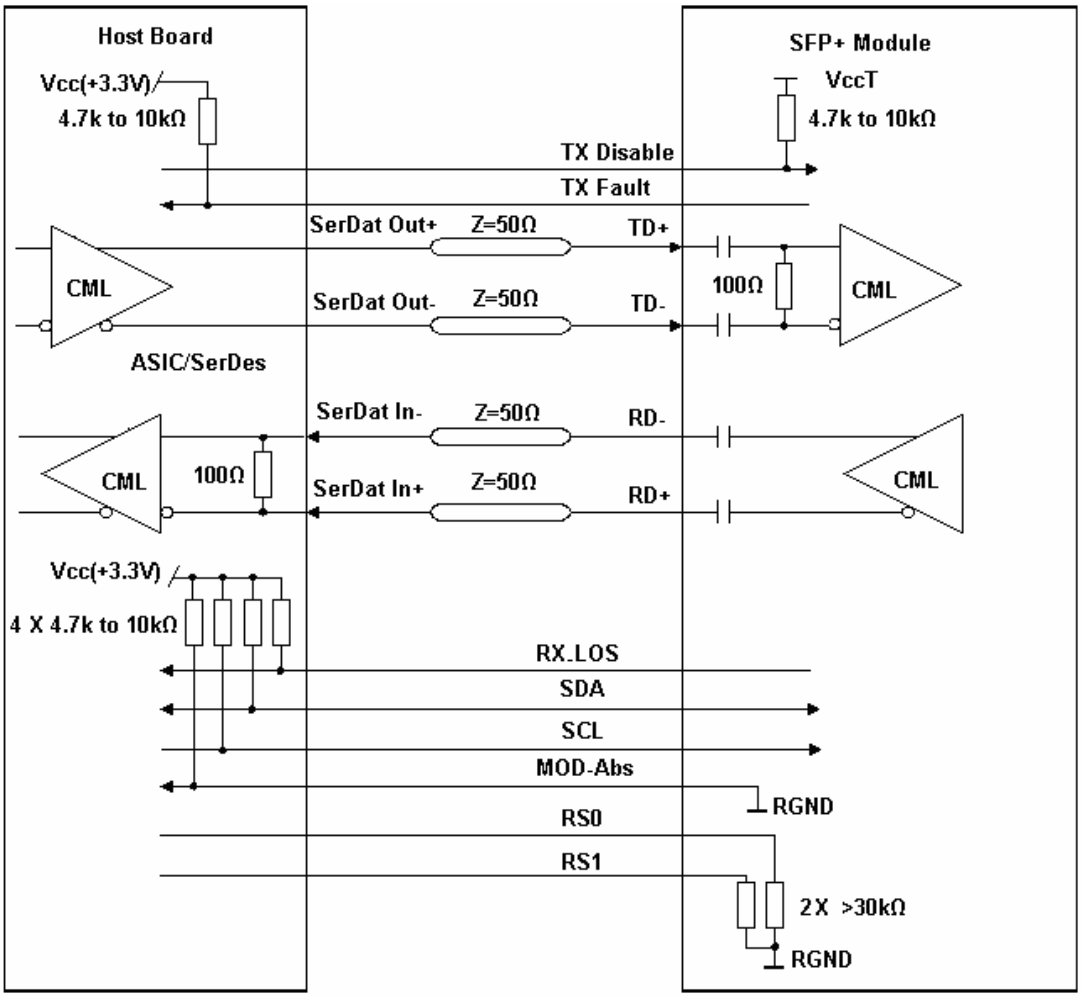


Figure 2, Recommended Interface Circuit

Pin Definitions

Figure 3 below shows the pin numbering of SFP+ electrical interface. The pin functions are described in Table 7 with some accompanying notes. SFP+ module pins make contact to the host in the order of ground, power, and followed by signal as given by Figure 4.

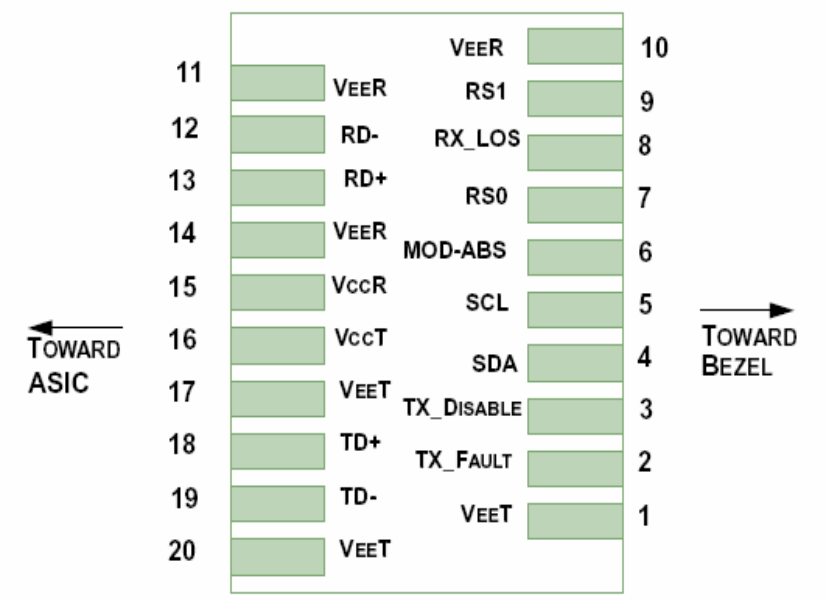


Figure 3, Host PCB Pinout Top View

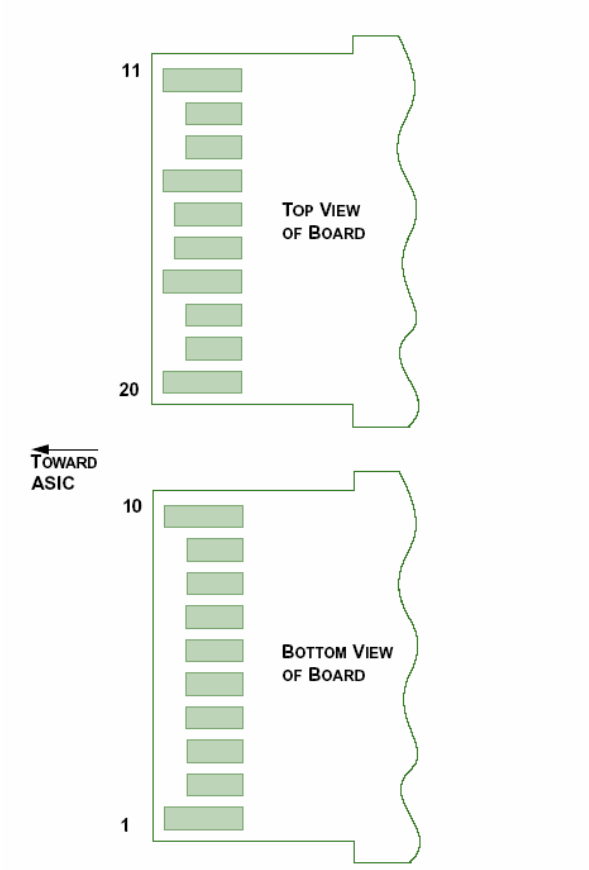


Figure 4, SFP+ module PCB Pinout

Table 10 – Pin Function Definitions

Pin	Logic	Symbol	Name/Description	Note
1		VeeT	Module Transmitter Ground	1
2	LVTTL-O	TX_Fault	Module Transmitter Fault	2
3	LVTTL-I	TX_DISABLE	Transmitter Disable; Turns off transmitter laser output	3
4	LVTTL-I/O	SDL	2-Wire Serial Interface Data Line (MOD-DEF2)	
5	LVTTL-I/O	SCL	2-Wire Serial Interface Clock (MOD-DEF1)	
6		MOD_ABS	Module Absent, connected to VeeT or VeeR in the module	3
7	LVTTL-I	RS0	Rate Select 0, optionally controls SFP+ module receiver as the following when HIGH input data rate>4.25 Gb/s and when LOW input data rate ≤4.25 Gb/s.	
8	LVTTL-O	RX_LOS	Receiver Loss of Signal Indication (in FC designated as RX_LOS, in SONET designated as LOS, and in Ethernet designated as NOT Signal Detect)	2
9	LVTTL-I	RS1	Rate Select 1, optionally controls SFP+ module transmitter as the following when HIGH input data rate>4.25 Gb/s and when LOW input data rate ≤4.25 Gb/s.	
10		VeeR	Module Receiver Ground	1
11		VeeR	Module Receiver Ground	1
12	CML-O	RD-	Receiver Inverted Data Output	
13	CML-O	RD+	Receiver Non-Inverted Data Output	
14		VeeR	Module Receiver Ground	1
15		VccR	Module Receiver 3.3 V Supply	
16		VccT	Module Transmitter 3.3 V Supply	
17		VeeT	Module Transmitter Ground	1
18	CML-I	TD+	Transmitter Non-Inverted Data Input	
19	CML-I	TD-	Transmitter Inverted Data Input	
20		VeeT	Module Transmitter Ground	1

Notes:

1. The module ground pins, VeeR and VeeT, shall be isolated from the module case.
2. This pin is an open collector/drain output pin and shall be pulled up with 4.7K-10Kohms to a Host_Vcc on the host board.
3. Shall be pulled up with 4.7K-10Kohms to VccT in the module.
4. This pin is an open collector/drain input pin and shall be pulled up with 4.7K-10Kohms to VccT in the module.

Mechanical Design Diagram

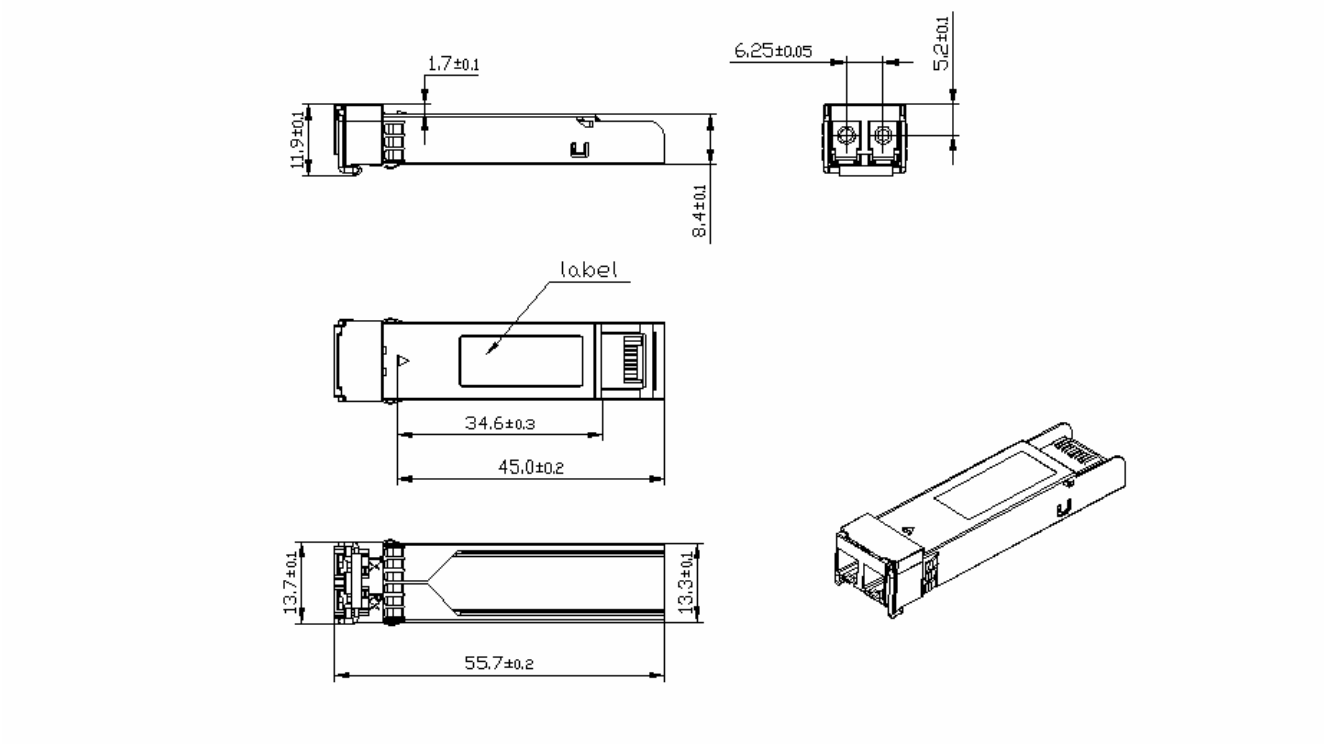
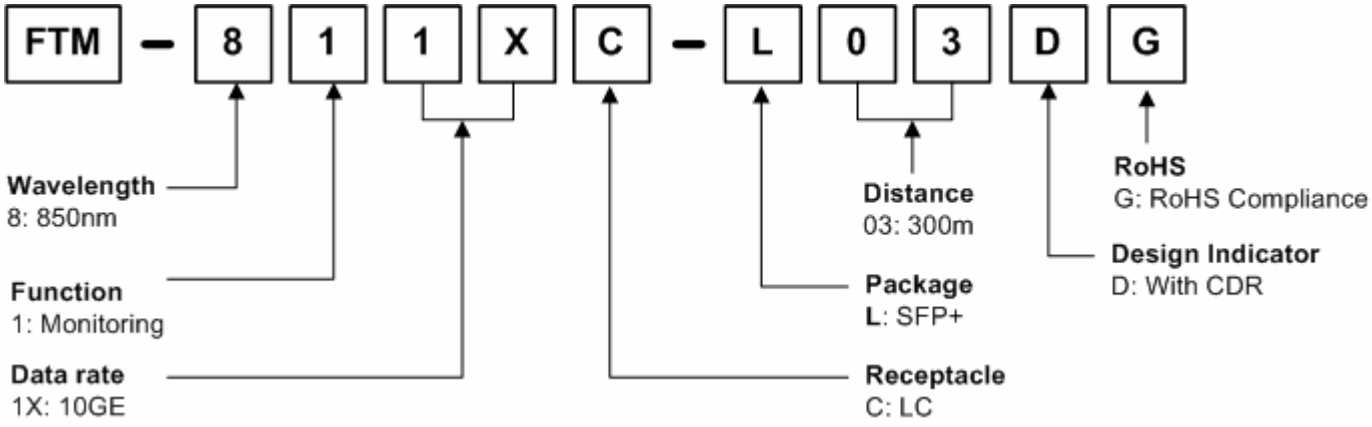


Figure 5, Mechanical Design Diagram of SFP+

Ordering information



Part No.	Product Description
FTM-811XC-L03DG	850nm VCSEL, 10Gbps, 300m, SFP+, RoHS compliance, with CDR

Related Documents

SFF-8431 (Specifications for Enhanced 8.5 and 10 Gigabit Small Form Factor Pluggable Module "SFP+"), Revision 1.3 February 16, 2007.
SFF-8432 (Specifications for Improved Pluggable Form factor), Revision 3.6 October 25, 2006.
SFF-8083 (Specifications for 0.8 mm SFP+ Card Edge Connector Dimensioning), Rev 0.9 January 2, 2007

Revision History

Revision	Initiate	Review	Approve	Subject	Release Date
Rev. 1a	Andy Xiao	Tripper Huang	Walker Wei	Initial datasheet	2007-10-11
Rev. 1b	Andy.Xiao	Tripper Huang	Alain.Shang	Update EEPROM contents	2007-11-30

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