AND-TFT-64PA-DHB

320 x 234 Pixels
LCD Color Monitor

The AND-TFT-64PA-DHB is a compact full color TFT LCD module, that is suitable for applications such as a car TV, portable DCD, GPS, multimedia applications and other AV equipment. This device consists of a twisted nematic (TN) liquid crystal cell, that incorporates a TFT-array that has 320 x 234 pixels on a 6.4 inch diagonal screen, X and Y drivers, an LSI controller, and a built-in CCFL backlight and inverter (with optional board.)

Features

- 6.4 inch (16 cm) diagonal screen
- Compatible with NTSC & PAL system
- Accepts VGA Input (Analog RGB)
- High brightness CCFL backlight (300 Nits)
- Slim and compact
- Operating temperature range -10 to 60° C
- Storage temperature range -30 to 80° C
- 12V single power supply (with optional board)
- RoHS compliant

Mechanical Characteristics

Item	Specification	Unit
Screen Size	6.4 inch (16 cm) diagonal	inch
Surface Treatment	Anti-Glare + WV film	–
Display Format	320 (W) x 234 (H)	dot
Active Area	129.6 (W) x97.34 (H)	mm
Dot Pitch	0.135 (W) x 0.416 (H)	mm
Pixel Configuration	Stripe	–
Outline Dimensions	156.3 typ. (W) x 120 (H) x 14.3 typ (D)	mm
Weight	TBD ± 10	g

Absolute Maximum Rating

Item		Symbol	Conditions	Absolute Maximum Rating		Unit
				Min.	Max.	
Supply Voltage for Source Driver	Analog	V_{CC}	–	-0.3	+7.0	V
	Digital	V_{DD}		-0.3	+7.0	
Supply Voltage for Gate Driver	Positive	V_{GH}	–	-0.3	+45	V
	Negative	V_{GL}	–	-23	+0.3	V
		V_{GH} V_{GL}		+15	+40	V
Analog input voltage (V_R, V_G, V_B)		V_{DD}	–	-0.3	+7.3	V
Digital input signals		–	$\overline{HSY}$, POLC, CSY, $\overline{VSY}$, CLKC PSI, COMPS, $\overline{VIY}$	-0.5	+5.5	V
Digital output signals		–		-0.5	+5.5	V
Storage Temperature		–	–	-30	+80	°C
Operation Temperature (defines that contrast, response time & other display optical characteristics are Ta=+25.)		–	–	-20	+70	°C

Product specifications contained herein may be changed without prior notice.
It is therefore advisable to contact Purdy Electronics before proceeding with the design of equipment incorporating this product.

Electrical Specification

Item		Symbol	Conditions	Specifications			Units
				Min.	Typ.	Max.	
Current Consumption for Driver		I_{GH}	V_{GH} = +17V	–	TBD	TBD	mA
		I_{GL}	V_{GL} = -15V	–	TBD	TBD	mA
		I_{CC}	V_{CC} = +5V	–	TBD	TBD	mA
		I_{DD}	V_{DD} = +5V	–	TBD	TBD	mA
Lamp voltage		V_L	I_L = 6mA	–	TBD	–	Vrms
Lamp current		I_L	–	–	6	–	mA
Lamp frequency		P_L	The waveform of lamp driving voltage should be as close to a perfect SIN wave as possible	TBD	TBD	TBD	KHz
Kick-off voltage (25_)		V_S	–	–	–	TBD	Vrms
Kick-off voltage (0_)		V_S	–	–	–	TBD	Vrms
Power Consumption	for LCD Panel	–	–	–	TBD	–	mW
	for Backlight Lamp	–	calculated by I_L_V_L	–	TBD	–	W
	TOTAL	–	–	–	TBD	–	W

Recommended Operating Conditions

Item		Symbol	Conditions	Specifications			Unit
				Min.	Typ.	Max.	
Power Supply		V_{CC}	–	+4.5	+5.0	+5.5	V
		V_{DD}	–	+4.5	+5.0	+5.5	V
		V_{GH}	–	+15.0	+17.0	+19.0	V
		$V_{GL\ AC}$	AC Component of V_{GL}	–	+6.0	–	V_{P-P}
		$V_{GL\ DC}$	DC Component of V_{GL}	-16.0	-15.0	-14.0	V
Video Signal (V_R, V_G, V_B)		$V_{i\ AC}$	AC Component STH1, STh2, CPH1, CPH2, CPH3, Q2H, INH, CPV, XOE, DIO1, DIO2	–	+4.0	+4.2	V_{P-P}
		$V_{i\ DC}$	DC Component	–	+2.5	–	V
V_{COM}		$V_{COM\ AC}$	AC Component of V_{COM}	–	+6.0	–	V_{P-P}
		$V_{COM\ DC}$	DC Component of V_{COM}	+1.6	+1.7	+1.8	V
	H Level	V_{IH}	Both NTSC & PAL system Video Signal input waveform is based on 8 steps grayscale.	+0.7 V_{DD}	–	–	V
	L Level	V_{IL}		–	–	+0.3 V_{DD}	V

Optical Specifications

Item		Symbol	Conditions	Specifications			Unit
				Min.	Typ.	Max.	
Viewing Angle	Horizontal	θ	CR>10	± 50	± 60	–	deg
	Vertical	θ (to 12 o'clock)		35	40	–	deg
		θ (to 6 o'clock)		50	55	–	deg
Contrast Ratio		CR	at optimized viewing angle*	110	150	–	–
Response Time	Rise	Tr	θ = 0°	–	15	30	ms
	Fall	Tf		–	25	50	ms
Transmission Ratio		T	–	7.5	8.0	8.5	%
Uniformity ***		U	–	70	75	–	%
Brightness **		LUM	–	–	500	–	cd/m^2
White Chromaticity **		x	θ = 0°	0.280	0.310	0.340	–
		y		0.300	0.330	0.360	–
		Tc		TBD	TBD	TBD	–
Lamp Life Time	+25°C	–	+25°C	10,000	–	–	hr

* Note: Contrast Ratio is measured in optimum common electrode voltage.

$$CR> \frac{\text{Luminance when LCD is White}}{\text{Luminance when LCD is Black}}$$

** 1. Topcon BM-7 (fast) luminance meter 2.0 field of view is used in the testing (after 20~30 minutes operation.)
2. Lamp Current: 6mA
3. Inverter model: TDK-347.

*** The uniformity of LCD is defined as:

$$U= \frac{\text{The Minimum Brightness of the 9 testing Points}}{\text{The Maximum Brightness of the 9 testing Points}}$$

Luminance meter: BM-5A or MB-7 fast (TOPCON)
Measurement distance: 500mm +/- 50 mm
Ambient illumination: < 1 Lux
Measurement direction: Perpendicular to the surface of module.
The test pattern is white (Gray Level 63.)

1. **Input/Output Connector**
   A) **LCD Connector: 6200-20P (Molex)**
   FFC Up Connector
   20 Pins
   Pitch: 1.0 mm

   B) **Backlight Connector: JST BHR-03VS-1**
   Pin No: 3
   Pitch: 4.0 mm
   Pink: High Voltage
   White: Low Voltage

Interface Pin Assignment Connector 1: Connector 1 (28 Pins) (Elco) 6200-500-28-800

Pin No.	Symbol	Function	I/O
1	$\overline{HSY}$	Horizontal Sync. Input / Output	Input/Output
2	POLC	Video Polarity Alternating Signal	Output
3	CSY/MCLK	Composite Sync. Signal / Mclk Signal	Input
4	V_{GH}	Gate on voltage	Input
5	V_{GL}	Gate off voltage (alternate every 1-H)	Input
6	V_B	Video Input B	Input
7	V_R	Video Input R	Input
8	V_G	Video Input G	Input
9	GND	Ground	Input
10	V_{DD}	Digital power input	Input
11	V_{CC}	Logic power for gate driver	Input
12	GND	Ground	Input
13*	CLKC	Control pin for select I/O signal	Input/Output
14	$\overline{VSY}$	Vertical Sync. Input / Output	Input/Output
15	PSI	Synchronize pulse for external clock	Input
16	COMPS	Select composite sync. mode & sync. separate mode	Input
17	$\overline{VIY}$	Vertical sync. input pin for sync. separate mode	Input
18	U/D	Up/Down control for gate driver	Input
19	R/L	Left/Right control for gate driver	Input
20	NP	NTSC/PAL Input	Input

1. Pin 13 (CLKC) can select the function of pin 1 ($\overline{HSY}$), 3 (CSY), and 14 ($\overline{VSY}$) as follows:

CKC	Pin 1 ($\overline{HSY}$)	Pin 3 (CSY)	Pin 14 ($\overline{VSY}$)
Hi	$\overline{HSY}$ output	CSY input	$\overline{VSY}$ output
Low	External Horizontal Sync. input	External Clock input	External Vertical Sync input

2. CKC = High:

a.	If CKC = 1, the phase lock loop (pll) is adopted in the LCd module.
b.	Inputs CSY, the controller of LCD module will separate the Vertical Sync and Horizontal Synch from CSY.
c.	Out put Horizontal Sync ($\overline{HSY}$, Pin 1) and Vertical Sync ($\overline{VSY}$, Pin 14.)
d.	The internal detect will detect Vertical Sync to reset the vertical counter.

3. CKC = Low:

a.	If CKC = 0, the phase lock loop (PLL) is not adopted in the LCD module.
b.	If CKC = 0, the external clock input frequency of Pin 3 is 6.4 MHz.
c.	Input external Vertical Sync. ($\overline{VIY}$, Pin 17) and Horizontal Sync. (Pin1) to synchronize the LCD module. External Horizontal Sync and External Vertical Sync. input pulse can be high going or low going.
d.	The pulse width of external Horizontal SYnc. input is 4.7 μs ±2 μs. The pulse width of external Vertical Sync. input is 2H~4H.
e.	The pulse length of external input Vertical Sync. of system is 262H ±4H.

4. If there is any question about CKC = 0, please contact Purdy Electronics.

5. V_{GH} TYP._+17V ; V_{GL} TYP._-15V ; V_{DD} TYP._+5V ; V_{CC} TYP._+5V

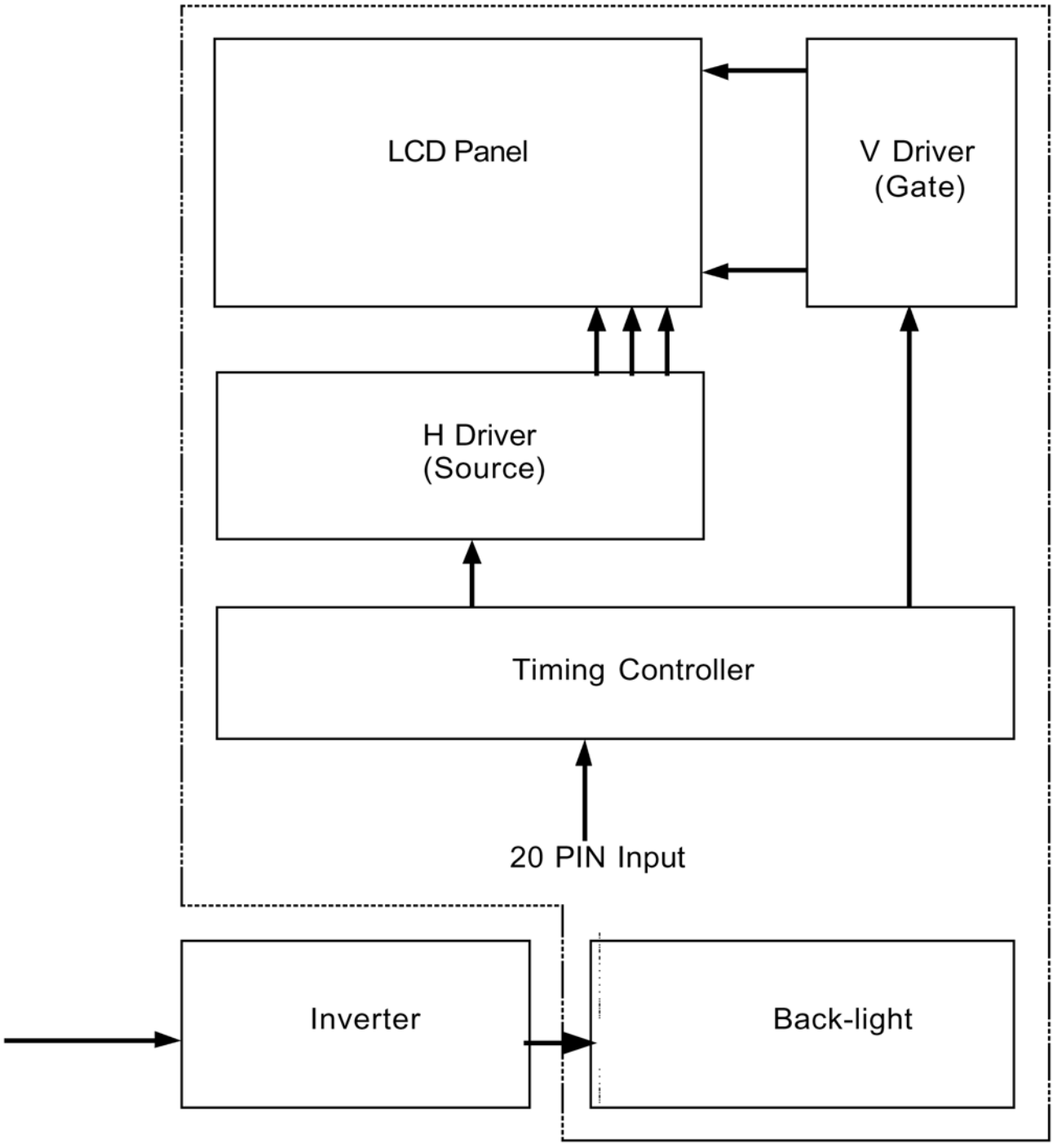
6. The frequency of PSI is 15.75 KHz.

7. Pin 16 (COMPS) can select composite sync. mode OR sync. separate mode

Pin 16 (COMPS)	Pin 3 (CSY)	Pin 17 ($\overline{VIY}$)
Hi	CSY (Positive Edge)	NC
Low	H_{sync} (Negative Edge)	V_{sync} (Negative Edge)

8. Default Hi (+5V) for shift Right; Input Low (0V) for inverst (shift Left.)
9. Default Hi (+5V) for DOWN; Low (0V) for UP.
10. NTSC = Hi (+5V), PAL = LOW (0V).

Block Diagram



Dimensional Outline

General mechanical tolerance = 0.5mm