?@QMJSRC K?VGKSK P?RGLEQ

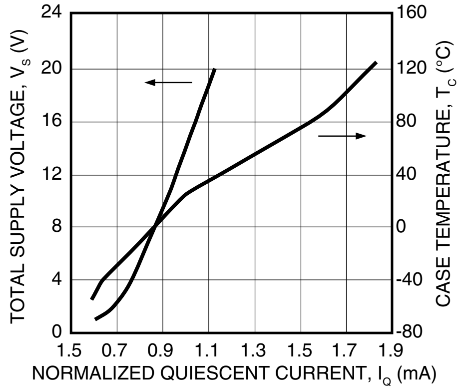
SUPPLY VOLTAGE, total	5V to 40V
OUTPUT CURRENT	SOA
POWER DISSIPATION, internal, (per ampli er)	19.5W
POWER DISSIPATION, internal (both ampli ers)	28.6W
INPUT VOLTAGE, differential	$–V_S$
INPUT VOLTAGE, common mode	$+V_S$, $-V_S$ 0.5V
JUNCTION TEMPERATURE, max[1]	150°C
TEMPERATURE, pin solder 10 sec max	220°C
TEMPERATURE RANGE, storage	55°C to 150°C
OPERATING TEMPERATURE RANGE, case	40°C to 125°C

SPECIFICATIONS

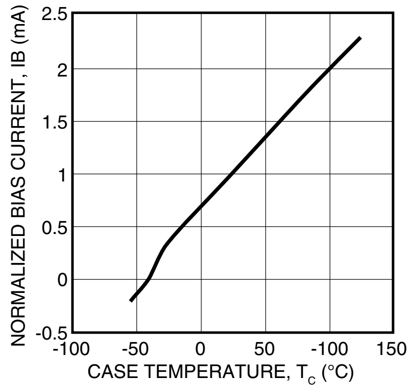
PARAMETER	TEST CONDITIONS [2]	MIN	TYP	MAX	UNITS
INPUT					
OFFSET VOLTAGE, initial			1	15	mV
OFFSET VOLTAGE, vs. temperature	Full temperature range		20		µV/°C
BIAS CURRENT, initial			100	500	nA
COMMON MODE RANGE	Full temperature range	V_S		$+V_S$ 1.3	V
COMMON MODE REJECTION, DC	Full temperature range	60	90		dB
POWER SUPPLY REJECTION	Full temperature range	60	90		dB
CHANNEL SEPARATION	I_{OUT} = 500mA, = 1kHz	50	68		dB
INPUT NOISE VOLTAGE	R_S = 100 , = 1 to 100kHz		22		nV/ Hz
GAIN					
OPEN LOOP GAIN	Full temperature range	89	100		dB
GAIN BANDWIDTH PRODUCT	A_V = 40dB	0.9	1.4		MHz
PHASE MARGIN	Full temperature range, R_L = 2K , C_L = 100pF		65		°
POWER BANDWIDTH	$V_{O(P-P)}$ = 28V		13.6		kHz
OUTPUT					
CURRENT, peak				1.5	A
SLEW RATE		1	1.4		V/µs
VOLTAGE SWING	Full Temperature Range, I_O = 100mA	$\|V_S\|$ - 1.1	$\|V_S\|$ - .8		V
VOLTAGE SWING	Full Temperature Range, I_O = 1A	$\|V_S\|$ - 1.8	$\|V_S\|$ - 1.4		V
HARMONIC DISTORTION	A_V = 1, R_2 = 50 , V_O = .5V_{RMS}, = 1kHz		.02		%
POWER SUPPLY					
VOLTAGE, V_{SS}[3]		5	30	40	V
CURRENT, quiescent, total			8	10	mA
THERMAL					
RESISTANCE,DC junction to case (single)			5.84	6.42	°C/W
RESISTANCE,AC junction to case (single)			4.38	4.81	°C/W
RESISTANCE,DC junction to case (both)			3.97	4.36	°C/W
RESISTANCE,AC junction to case (both)			2.98	3.27	°C/W
RESISTANCE,junction to air (CD,CX)			60		°C/W
RESISTANCE,junction to air (CC)[4]			27		°C/W
TEMPERATURE RANGE,case	Meets full range speci cations	25		85	°C

NOTES:
1. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF.
2. Unless otherwise noted, the following conditions apply: $–V_S$ = –15V, T_C = 25°C.
3. $+V_S$ and V_S denote the positive and negative supply rail respectively. V_{SS} denotes the total rail-to-rail supply voltage.
4. Heat tab attached to 3/32" FR-4 board with 2oz. copper. Topside copper area (heat tab directly attached) = 1000 sq. mm, back-side copper area = 2500 sq. mm, board area = 2500 sq. mm.

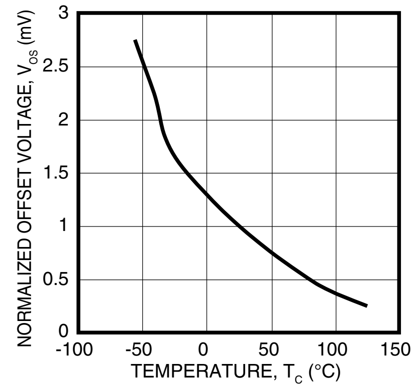
QUIESCENT CURRENT



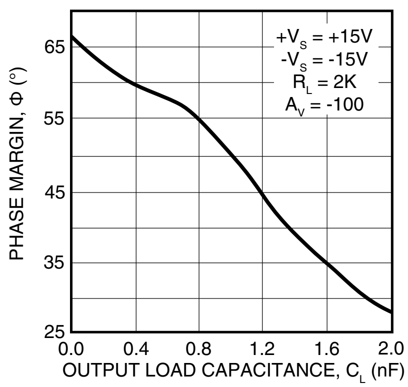
BIAS CURRENT



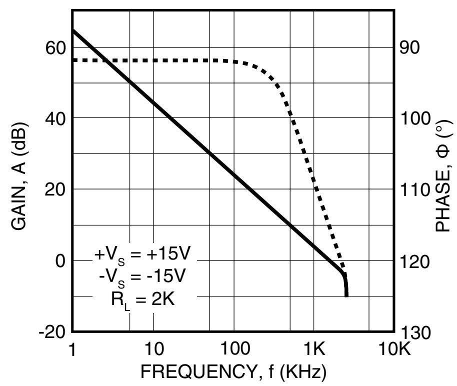
OFFSET VOLTAGE



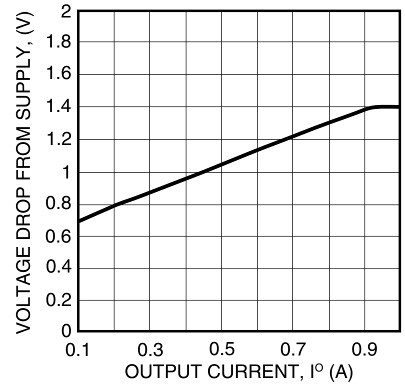
PHASE MARGIN vs. OUTPUT LOAD CAPACITANCE



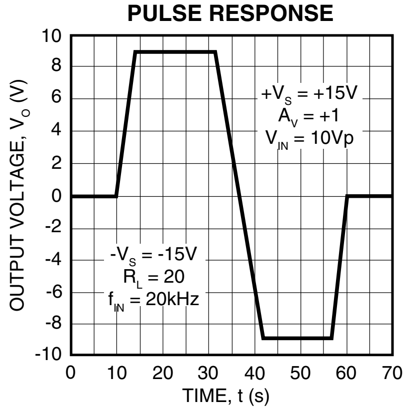
VOLTAGE GAIN & PHASE vs. FREQUENCY



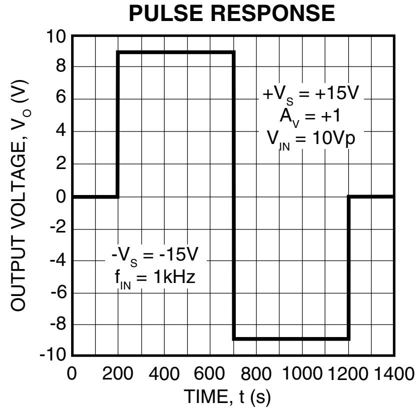
OUTPUT VOLTAGE SWING



PULSE RESPONSE



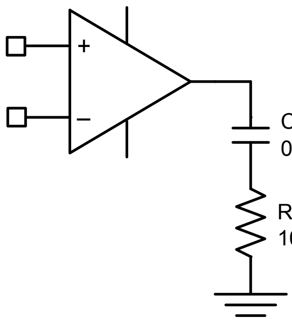
PULSE RESPONSE



GENERAL

Please read Application Note 1 General Operating Considerations which covers stability, supplies, heatsinking, mounting, SOA interpretation, and speci cation interpretation. Visit www. Cirrus.com for design tools that help automate tasks such as calculations for stability, internal power dissipation, heatsink selection; Apex Precision Power s complete Application Notes library; Technical Seminar Workbook; and Evaluation Kits.

QR?@GJGRW AMLQGBCP?RGMLQ

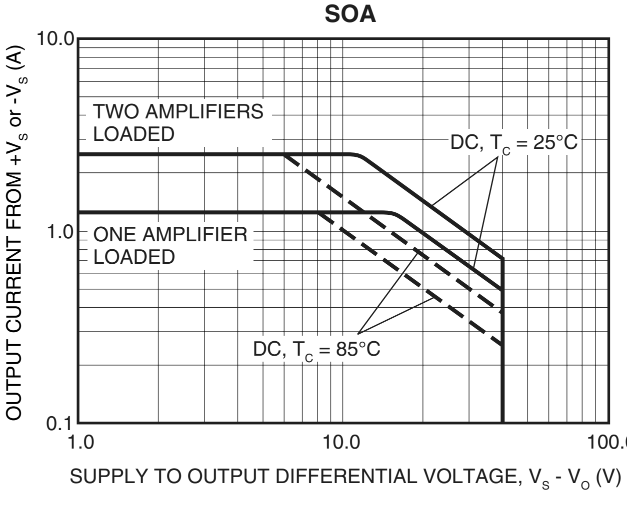


All monolithic power op amps use output stage topologies that present special stability problems. This is primarily due to non-complementary (both devices are NPN) output stages with a mismatch in gain and phase response for different polarities of output current. It is dif- cult for the op amp manufacturer to optimize compensation for all operating conditions. For applications with load current exceeding 300ma, oscillation may appear. The oscillation may occur only with the output voltage swing at the negative or positive half cycle. Under most operating and load conditions acceptable stability can be achieved by providing a series RC snubber network connected from the output to ground. The recommended component values of the of the network are, R_{SN} = 10 and C_{SN} = 0.01µF. Please refer to Application Note 1 for further details.

Q?DC MNCP?RGLE ?PC? &QM?

The SOA curves combine the effect of all limits for this power op amp. For a given application, the direction and magnitude of the output current should be calculated or measured and checked against the SOA curves. This is simple for resistive loads but more complex for reactive and EMF generating loads.

SOA



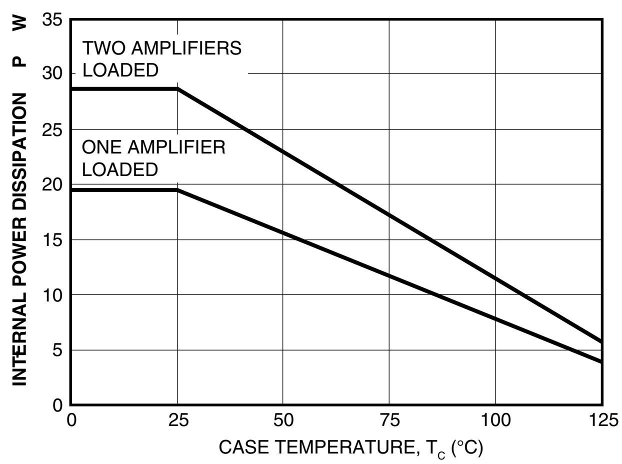
RFCPK?J AMLQGBCP?RGMLQ

The PA75CD and CX have a large exposed copper heat tab to which the monolithic is directly attached. The PA75CD and CX may require a thermal washer, which is electrically insulating since the tab is directly tied to -VS. This can result in a thermal impedance RCS of up to 1 C/W or greater.

The PA75CC has a large exposed integrated copper heatslug to which the monolithic is directly attached. The solder connection of the heatslug to a minimum of 1 square inch foil area of the printed circuit board will result in thermal performance of 25°C/W junction to air rating of the PA75CC. Solder connection to an area of 1 to 2 square inches of foil is required for minimal power applications

Where the PA75CC is used in higher power applications, it is necessary to use surface mount techniques of heatsinking. Surface mount techniques include the use of a surface mount fan in combination with a surface mount heatsink on the backside of the FR4/ PC board with through hole thermal vias. Other highly thermal conductive substrate board materials are available for maximum heat sinking.

POWER DERATING



KMSLRGLE NPCA?SRGMLQ

1. Always use a heat sink. Even unloaded the PA75 can dissipate up to .4 watts.
2. Avoid bending the leads. Such action can lead to internal damage.
3. Always fasten the tab of the CD and CX package to the heat sink before the leads are soldered to xed terminals.
4. Strain relief must be provided if there is any probability of axial stress to the leads.