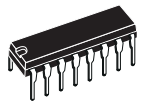
STPIC6D595

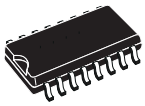
Power logic 8-bit shift register

Features

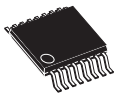
- Low $R_{DS(on)}$: 4Ω typ
- Eight 100mA DMOS outputs
- 250mA current limit capability
- Device are cascadable
- Low power consumption



DIP-16



SO-16



TSSOP16

Description

This STPIC6D595 is a monolithic, medium-voltage, low current power 8-bit shift register designed for use in systems that require relatively moderate load power such as LEDs.

The device contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. Data transfers through both the shift and storage register clock (SRCK) and the register clock ($\overline{RCK}$), respectively. The device transfers data out the serial output (SER OUT) port on the rising edge of SRCK. The storage register transfers data to the output buffer when shift register clear (CLR) is high. When $\overline{CLR}$ is low, the input shift register is cleared. When output enable ($\overline{G}$) is held high, all data in the output buffer is held low and all drain output are off. When G is held low, data from the storage register is transparent to the output buffer.

When data in the output buffers is low, the DMOS transistor outputs are off. When data is high, the DMOS transistor outputs have sink-current capability. The SER OUT allows for cascading of the data from the shift register to additional devices.

Output are low-side, open-drain DMOS transistors with output ratings of 20V and 120mA continuous sink-current capability. Each output provides a 250 mA maximum current limit at T_C = 25°C. The current limit decreases as the junction temperature increases for additional device protection. The device also provides up to 2.0KV of ESD protection when tested using the human-body model.

The STPIC6D595 is characterized for operation over the operating case temperature range of -40°C to 125°C.

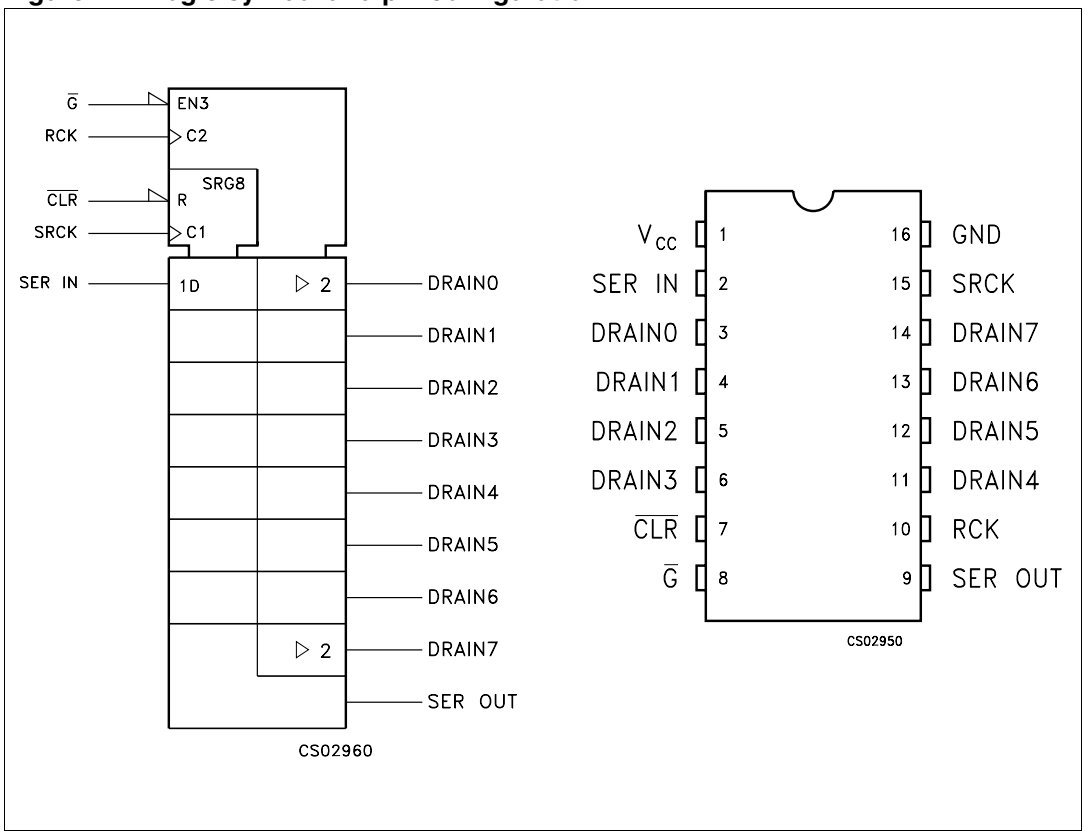
Table 1. Device summary

Order code	Package	Packaging
STPIC6D595M	SO-16 (Tube)	50 parts per tube / 20 tube per box
STPIC6D595MTR	SO-16 (Tape & Reel)	2500 parts per reel
STPIC6D595TTR	TSSOP16 (Tape & Reel)	2500 parts per reel
STPIC6D595B1	DIP-16	2500 parts per reel

Contents

1 Logic symbol and pin configuration

Figure 1. Logic symbol and pin configuration



2 Maximum rating

Stressing the device above the rating listed in the “Absolute Maximum Ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

2.1 Absolute maximum ratings

Table 2. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_{CC}	Logic supply voltage (See *Note 1*)	7	V
V_I	Logic input voltage range	-0.3 to 7	V
V_{DS}	Power DMOS drain to source voltage (See *Note 2*)	20	V
I_{DS}	Continuous source to drain diode anode current	250	mA
I_D	Pulsed drain current, each output, all output ON (T_C = 25°C)	250	mA
I_D	Continuous current, each output, All Output ON (T_C = 25°C)	100	mA
I_D	Peak drain current single output (T_C = 25°C) (See *Note 3*)	250	mA
P_d	Continuous total dissipation ($T_C \leq 25$°C)	1087	mW
P_d	Continuous total dissipation (T_C = 125°C)	217	mW
T_J	Operating virtual junction temperature range	-40 to +150	°C
T_C	Operating case temperature range	-40 to +125	°C
T_{stg}	Storage temperature range	-65 to +150	°C
T_L	Lead temperature 1.6mm (1/16inch) from case for 10 seconds	260	°C

2.2 Thermal data

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{th(JA)}$	Thermal resistance junction-ambient	115	°C/W

2.3 Recommended operating conditions

Table 4. Recommended operating conditions

Symbol	Parameter	Min	Max	Unit
V_{CC}	Logic supply voltage	4.5	5.5	V
V_{IH}	High level input voltage	$0.85V_{CC}$	V_{CC}	V
V_{IL}	LoW Level Input Voltage	0	$0.15V_{CC}$	V
I_{DP}	Pulse drain output current (T_C = 25°C, V_{CC} = 5V,all outputs ON) (see *Note 3*, *Note 4*)		250	mA
t_{su}	Set-up Time, SER IN High Before SRCK ↑ (see *Figure 3* and *Figure 7*)	20		ns
t_h	Hold Time, SER IN High Before $\overline{G}$ ↑ (see Figure *Figure 3*, *Figure 6*, *Figure 7*)	20		ns
t_W	Pulse duration (see *Figure 7*)	40		ns
T_C	Operating case temperature	-40	125	°C

3 Electrical characteristics

3.1 DC characteristics

Table 5. DC characteristics (V_{CC} = 5V, T_C = 25°C, unless otherwise specified.)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$V_{(BR)DSX}$	Drain-to-source breakdown voltage	I_D = 1mA			20	V
V_{OH}	High level output voltage SER OUT	I_{OH} = -20 µAV_{CC} = 4.5V	4.4	4.49		V
		I_{OH} = -4 mAV_{CC} = 4.5V	4			V
V_{OL}	Low level output voltage SER OUT	I_{OH} = 20 µAV_{CC} = 4.5V		1	100	mV
		I_{OH} = 4 mAV_{CC} = 4.5V		145	300	mV
I_{IH}	High level input current	V_{CC} = 5.5VV_I = V_{CC}		1	100	nA
I_{IL}	Low level input current	V_{CC} = 5.5VV_I = 0		-1	-100	nA
I_{CC}	Logic supply current	V_{CC} = 5.5V All outputs OFF or ON		23	40	µA
$I_{CC(FRQ)}$	Logic supply current at frequency	f_{SRCK} = 5MHzC_L = 30pF All outputs OFF (See *Figure 5*,(1))		70	250	µA
I_N	Nominal current	$V_{DS(on)}$ = 0.5VI_N = I_D T_C=85°C (See *Note 4*, *Note 5*, *Note 6*) (1)		120	200	µA
I_{DSX}	Off-state drain current	V_{DS} = 20VV_{CC} = 5.5V		0.02	1	µA
		V_{DS} = 20VV_{CC} =5.5V or 0V T_C = 125°C		0.5	1	µA
$R_{DS(on)}$	Static drain source on state resistance (See *Note 4*, and *Note 5*)	I_D = 50mAV_{CC} = 4.5V		3.4	4	Ω
		I_D = 50mAV_{CC} = 4.5V T_C = 125°C		4.8	6	Ω
		I_D = 100mAV_{CC} = 4.5V		3.5	6	Ω

1. Not tested, specified by design

3.2 Switching characteristics

Table 6. Switching characteristics (V_{CC} = 5V, T_C = 25°C, unless otherwise specified.)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
t_{PHL}	Propagation delay time, high to low level output from $\overline{G}$	C_L = 30pF I_D = 75mA (See *Figure 3*, *Figure 4*, *Figure 5*, *Figure 6*,)		19	30	ns
t_{PLH}	Propagation delay time, low to high level output from $\overline{G}$			46	70	ns
$t_{PHL-SDO}$	Propagation delay time, Clock to SDO			14	20	ns
$t_{PLH-SDO}$	Propagation delay time, Clock to SDO			14	20	ns
t_{PLH-R_O}	Propagation delay low to high level RCK to OUT			62	90	ns
t_{PHL-R_O}	Propagation delay high to low level RCK to OUT			13	18	ns
t_{PLH-S_SO}	Propagation delay low to high level SCK to SDO			14	20	ns
t_{PHL-S_SO}	Propagation delay high to low level SCK to SDO			14	20	ns
t_r	Rise time, drain output			20	30	ns
t_f	Fall time, drain output			15	20	ns

Note: 1 All voltage value are with respect to GND

2 Each power DMOS source is internally connected to GND

3 Pulse duration ≤ 100μs and duty cycle ≤ 2%

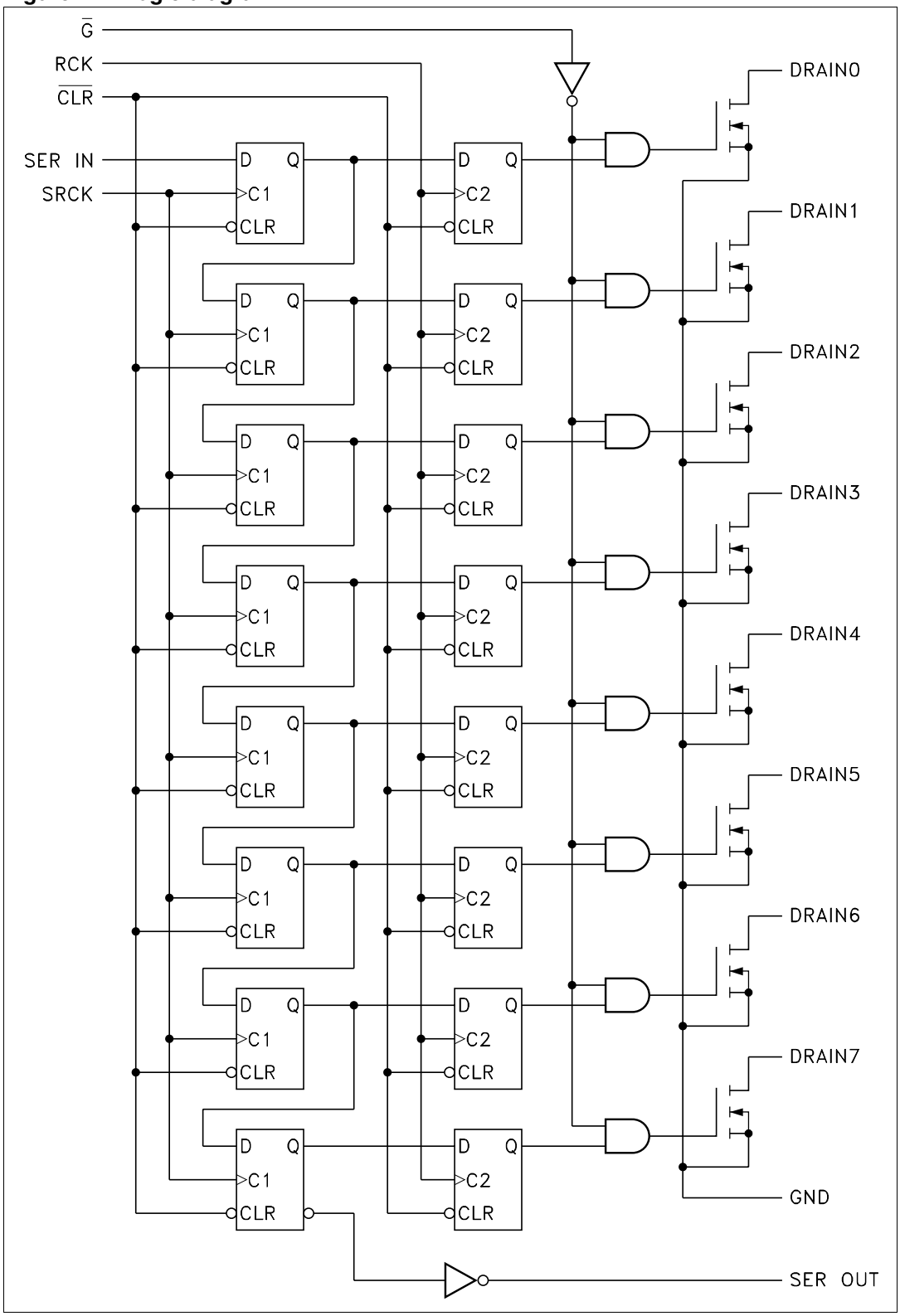
4 Technique should limit T_J - T_C to 10°C maximum

5 These parameters are measured with voltage sensing contacts separate from the current-carrying contacts.

6 Nominal Current is defined for a consistent comparison between devices from different sources. It is the current that produces a voltage drop of 0.5V at T_C = 85°C.

4 Logic diagram

Figure 2. Logic diagram



5 Typical operating circuit

Figure 3. Typical operation mode test circuits

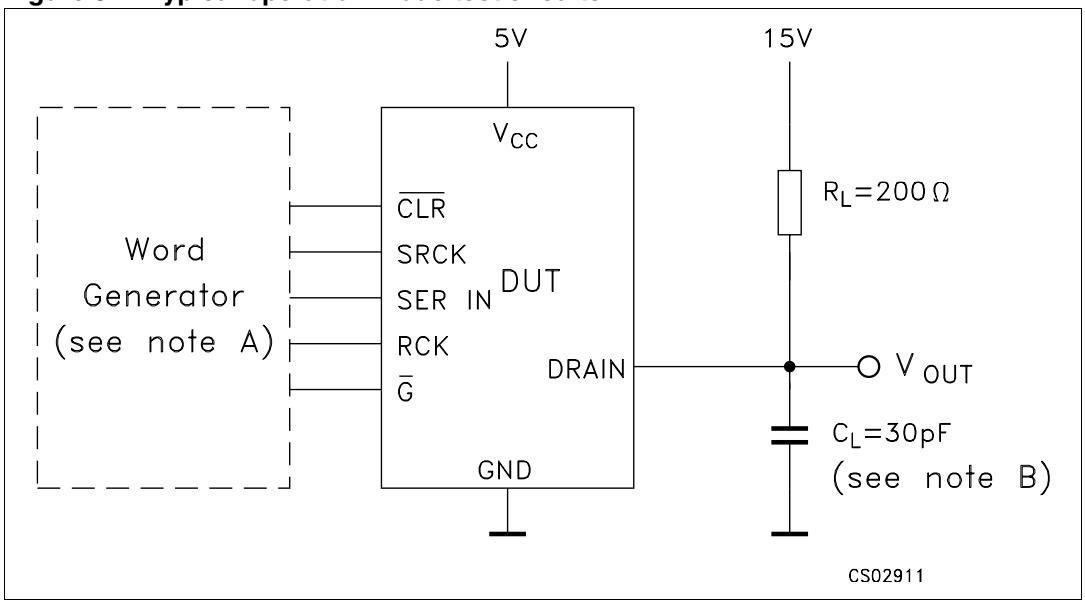
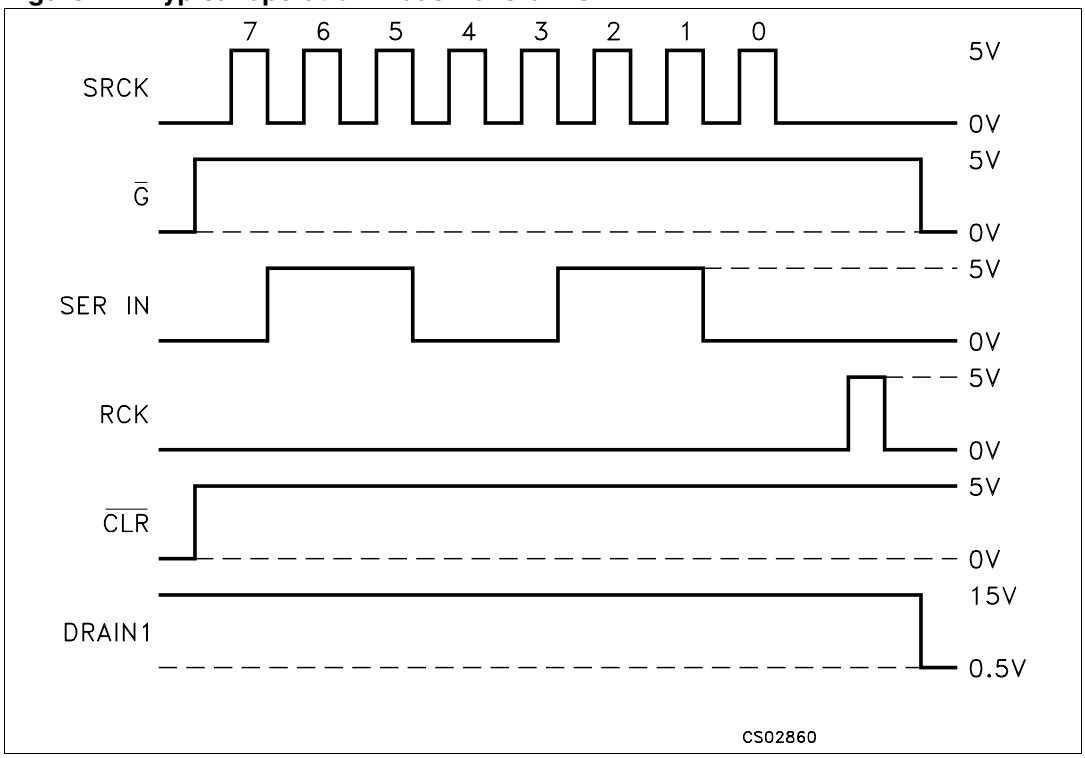


Figure 4. Typical operation mode waveforms



Note: 1 A) The word generator has the following characteristics: $t_r \leq 10ns$, $t_f \leq 10ns$, $t_W = 300ns$, pulse repetition rate (PRR) = 5KHz, $Z_O = 50\Omega$

2 B) C_L includes probe and jig capacitance.

Figure 5. Typical operation mode test circuits

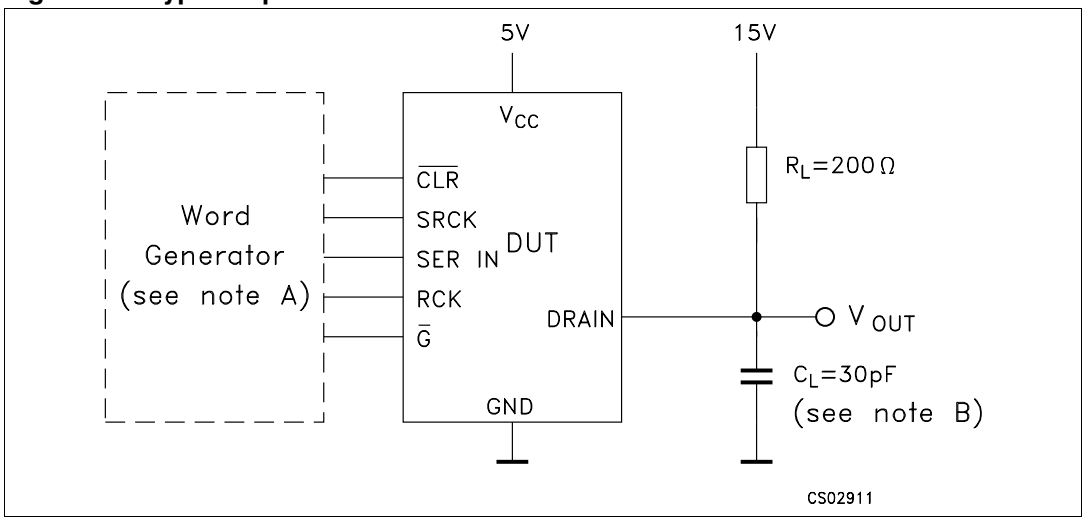


Figure 6. Switching time waveform

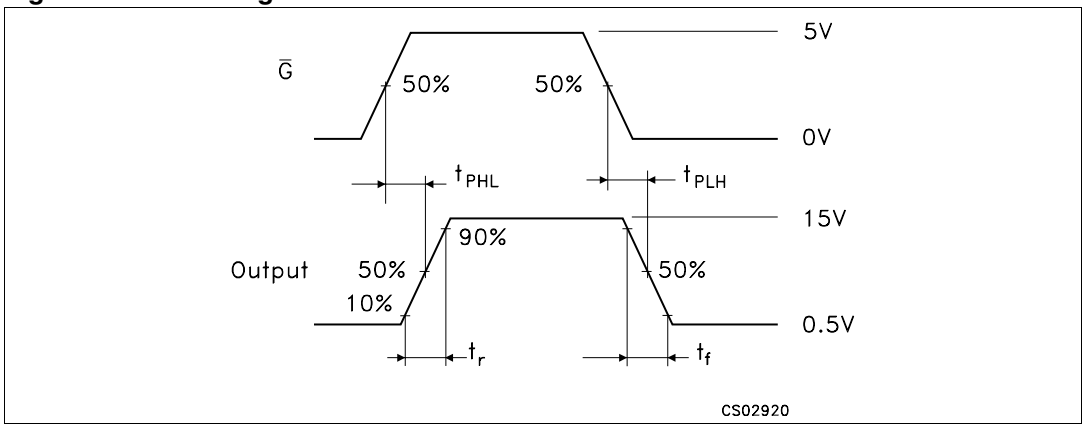
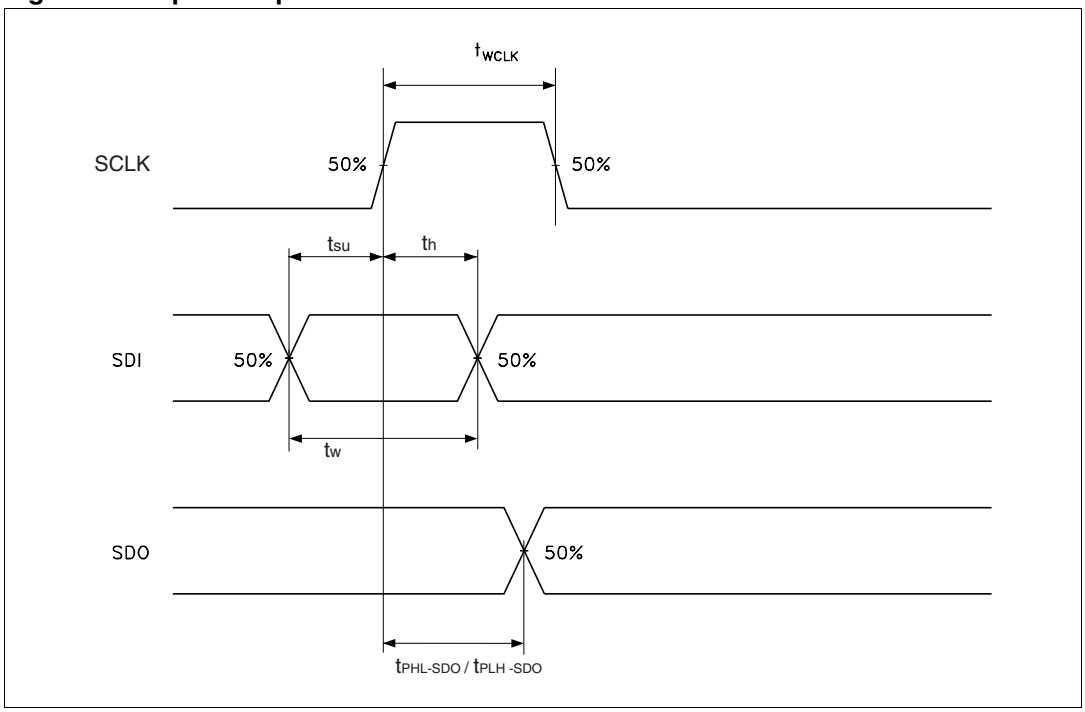


Figure 7. Input setup and hold waveform



Note: 1 A) The word generator has the following characteristics: $t_r \leq 10ns$, $t_f \leq 10ns$, $t_W = 300ns$, pulse repetition rate (PRR) = 5KHz, $Z_O = 50\Omega$

2 B) C_L includes probe and jig capacitance.

Figure 8. Input equivalent circuit

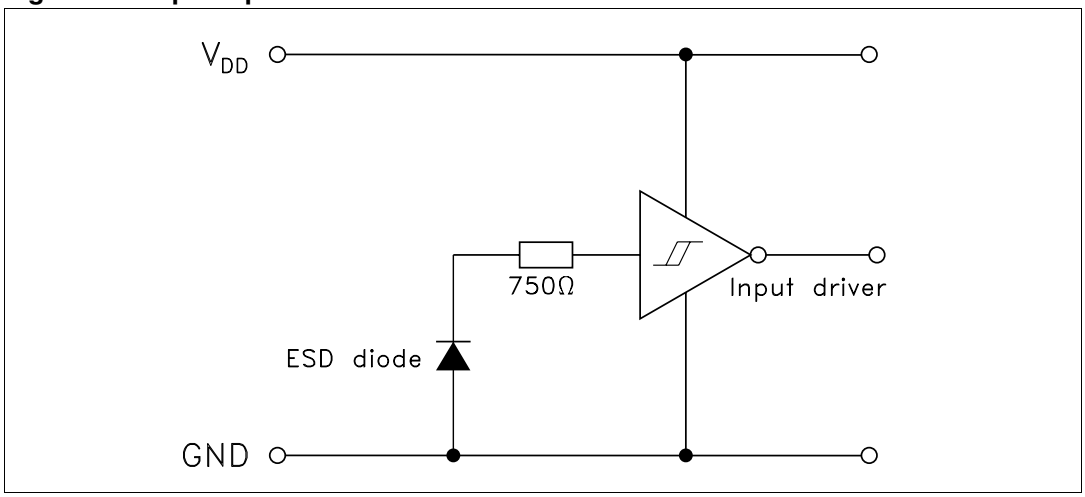
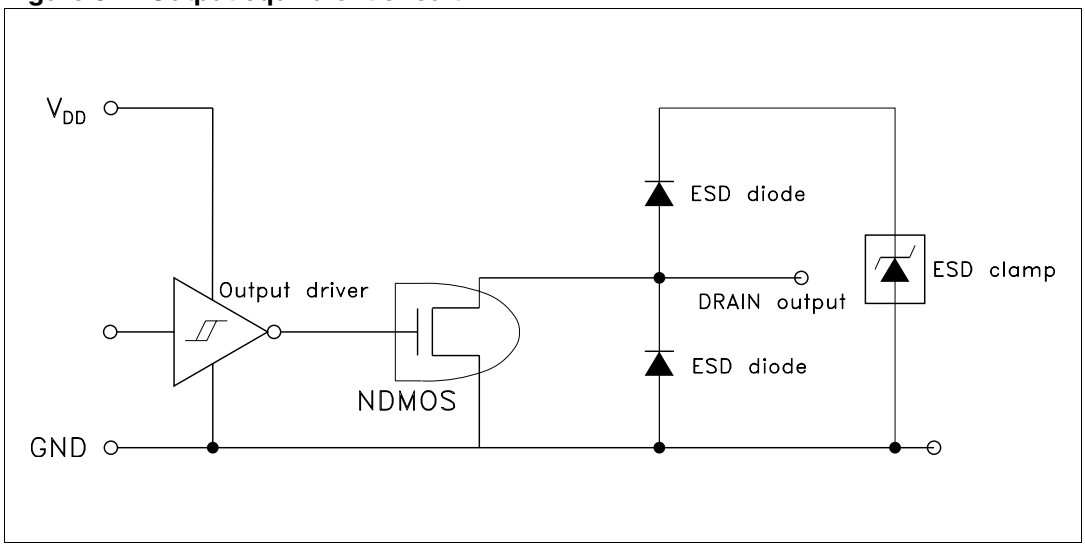


Figure 9. Output equivalent circuit

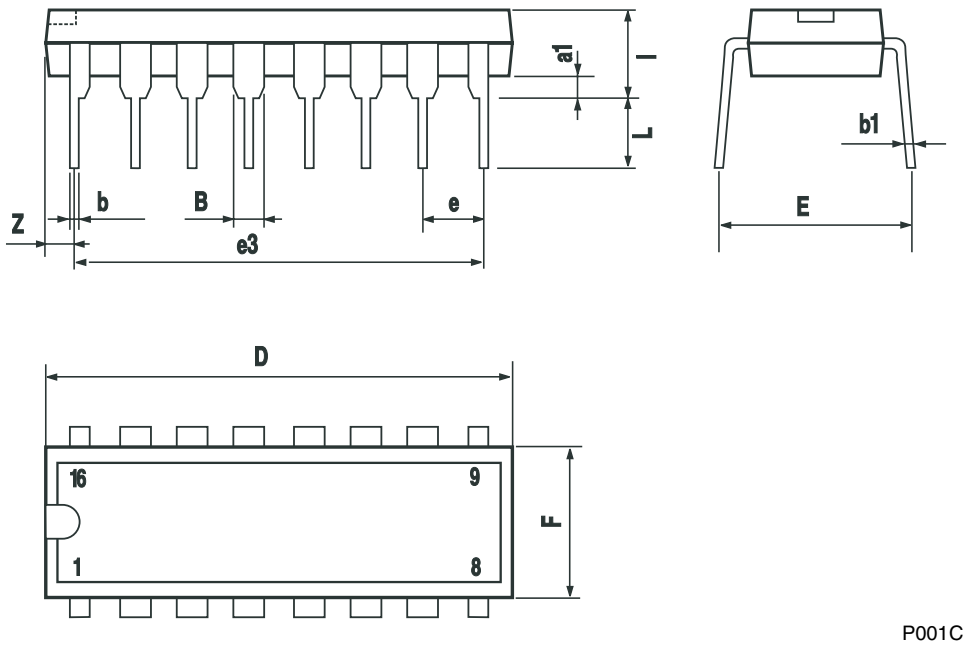


6 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

Plastic DIP-16 (0.25) MECHANICAL DATA

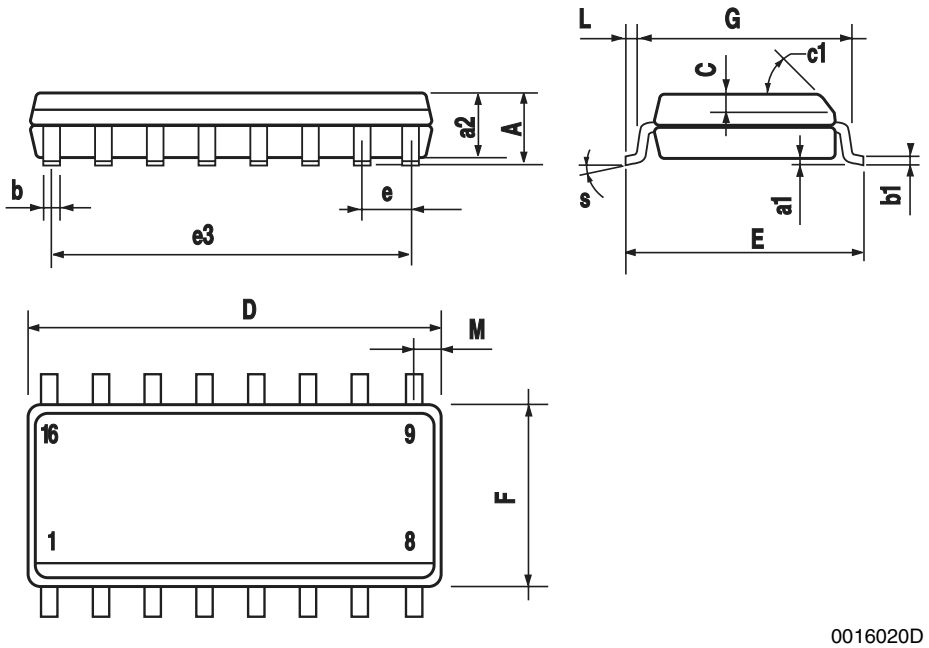
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050



P001C

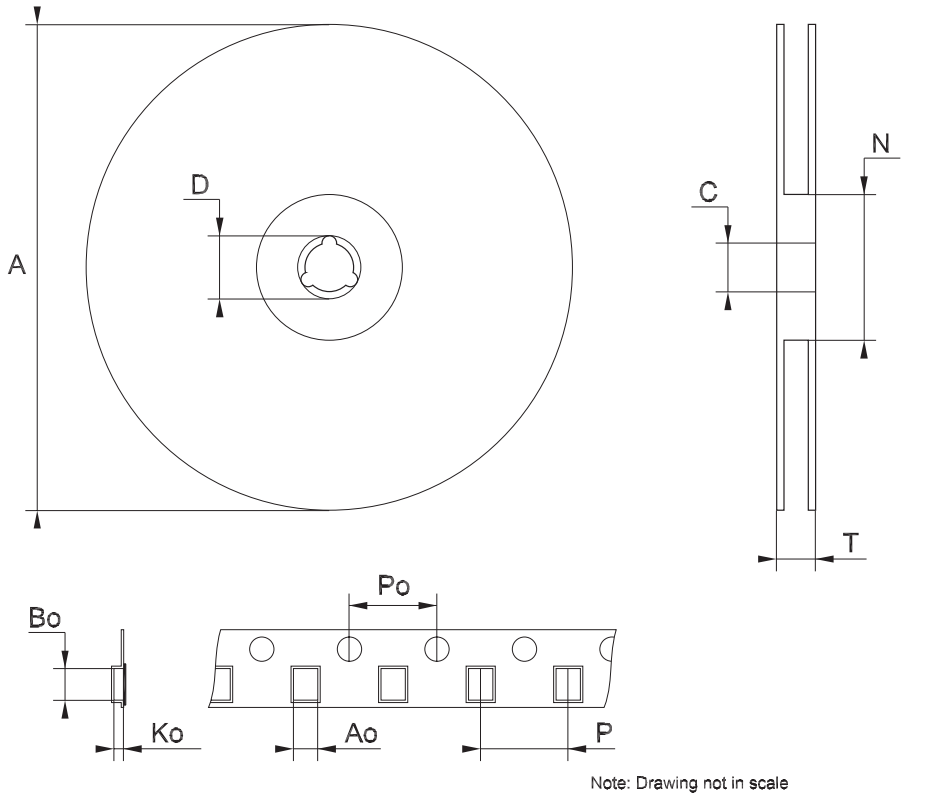
SO-16 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.25	0.004		0.010
a2			1.64			0.063
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	9.8		10	0.385		0.393
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.62			0.024
S	8° (max.)					



Tape & Reel SO-16 MECHANICAL DATA

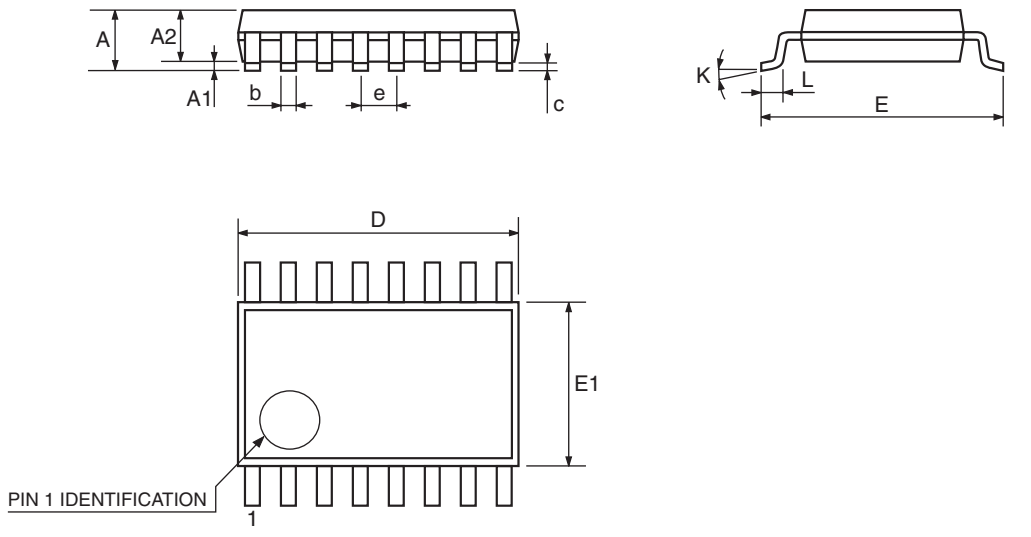
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			22.4			0.882
Ao	6.45		6.65	0.254		0.262
Bo	10.3		10.5	0.406		0.414
Ko	2.1		2.3	0.082		0.090
Po	3.9		4.1	0.153		0.161
P	7.9		8.1	0.311		0.319



Note: Drawing not in scale

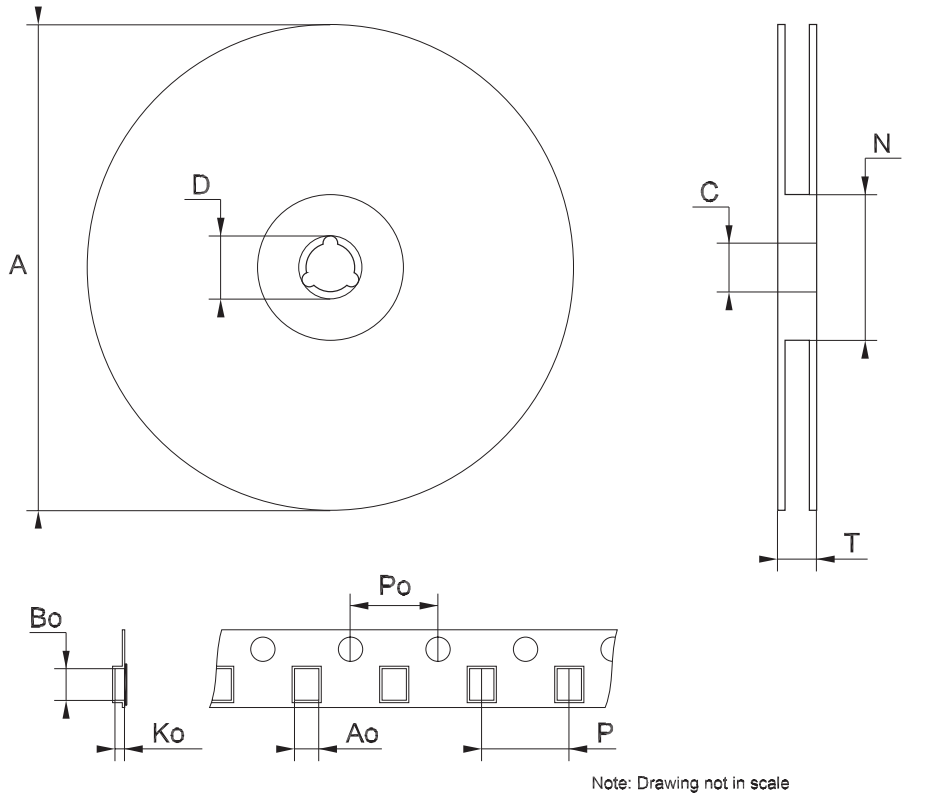
TSSOP16 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.2			0.047
A1	0.05		0.15	0.002	0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0079
D	4.9	5	5.1	0.193	0.197	0.201
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030



Tape & Reel TSSOP16 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			22.4			0.882
Ao	6.7		6.9	0.264		0.272
Bo	5.3		5.5	0.209		0.217
Ko	1.6		1.8	0.063		0.071
Po	3.9		4.1	0.153		0.161
P	7.9		8.1	0.311		0.319



Note: Drawing not in scale

7 Revision history

Table 7. Document revision history

Date	Revision	Changes
20-Jun-2007	1	First release
06-Sep-2007	2	Change from Preliminary to final version

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