Timing-Safe™ Peak EMI reduction IC

General Features

- Clock distribution with Timing-Safe™ Peak EMI Reduction
- Input frequency range: 20MHz - 50MHz
- Zero input - output propagation delay
- Low-skew outputs
  - Output-output skew less than 250pS
  - Device-device skew less than 700pS
- Less than 200pS cycle-to-cycle jitter
- Available in 8pin, 150 mil SOIC, 4.4mm TSSOP Packages (ASM3P623S00B/C/J)
- 3.3V operation
- Industrial temperature range
- Advanced 0.35µ CMOS technology
- The First True Drop-in Solution

Functional Description

ASM3P623S01B/C/J is a versatile, 3.3V zero-delay buffer designed to distribute high-speed Timing-Safe™ clocks with Peak EMI reduction. ASM3P623S01B/C accepts one reference input and drives out three low-skew clocks. It is available in 8pin package. The ASM3P623S01J is the eight-pin version with crystal interface and accepts one reference input and drives out two low-skew clocks.

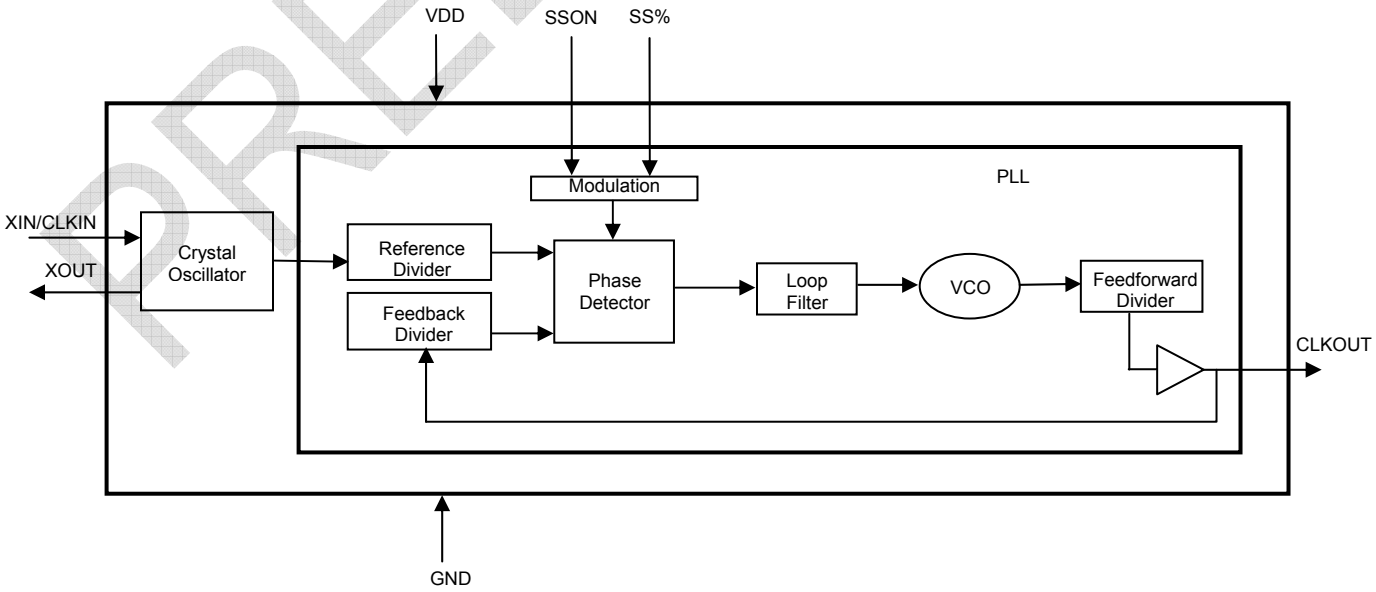
All parts have on-chip PLLs that lock to an input clock on the CLKIN pin. The PLL feedback is on-chip and is obtained from the CLKOUT pad, internal to the device.

Multiple ASM3P623S01B/C/J devices can accept the same input clock and distribute it. In this case, the skew between the outputs of the two devices is guaranteed to be less than 700pS.

All outputs have less than 200pS of cycle-to-cycle jitter. The input and output propagation delay is guaranteed to be less than 250pS, and the output-to-output skew is guaranteed to be less than 250pS.

Refer "Spread Spectrum Control and Input-Output Skew Table" for deviations and Input-Output Skew for ASM3P623S01B/C/J devices

Block Diagram



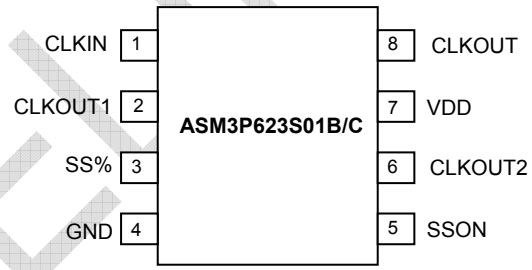
Spread Spectrum Frequency Generation

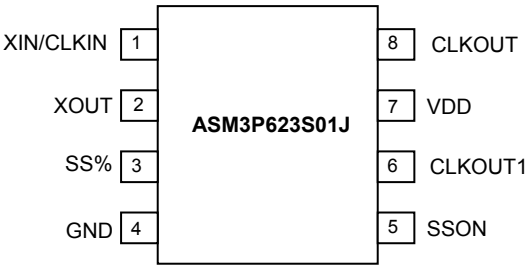
The clocks in digital systems are typically square waves with a 50% duty cycle and as frequencies increase the edge rates also get faster. Analysis shows that a square wave is composed of fundamental frequency and harmonics. The fundamental frequency and harmonics generate the energy peaks that become the source of EMI. Regulatory agencies test electronic equipment by measuring the amount of peak energy radiated from the equipment. In fact, the peak level allowed decreases as the frequency increases. The standard methods of reducing EMI are to use shielding, filtering, multi-layer PCBs etc. These methods are expensive. Spread spectrum clocking reduces the peak energy by reducing the Q factor of the clock. This is done by slowly modulating the clock frequency. The ASM3P623S01B/C/J uses the center modulation spread spectrum technique in which the modulated output frequency varies above and below the reference frequency with a specified modulation rate. With center modulation, the average frequency is the same as the unmodulated frequency and there is no performance degradation

Timing-Safe™ technology

Timing-Safe™ technology is the ability to modulate a clock source with Spread Spectrum technology and maintain synchronization with any associated data path.

Pin Configuration





Pin Description for ASM3P623S01B/C

Pin #	Pin Name	Description
1	CLKIN	Input reference frequency, 5V-tolerant input
2	CLKOUT[2]	Buffered clock output
3	SS%[3]	Spread Spectrum Selection
4	GND	Ground
5	SSON[3]	Spread Spectrum enable and disable option When SSON is HIGH, the spread spectrum is enabled and when LOW, it turns off the spread spectrum.
6	CLKOUT[2]	Buffered clock output
7	VDD	3.3V supply
8	CLKOUT[1,2]	Buffered clock output

Notes:
1. This output is driven and has an internal feedback for the PLL.
2. Weak pull-down on all outputs. 3. Weak pull-up on these inputs
4. Buffered clock outputs are Timing-Safe™

Pin Description for ASM3P623S01J

Pin #	Pin Name	Description
1	XIN/CLKIN	Crystal connection or external reference frequency input. This pin has dual functions. It can be connected either to an external crystal or an external reference clock.
2	XOUT	Crystal connection. If using an external reference, this pin must be left unconnected.
3	SS%[2]	Spread Spectrum Selection
4	GND	Ground
5	SSON[2]	Spread Spectrum enable and disable option When SSON is HIGH, the spread spectrum is enabled and when LOW, it turns off the spread spectrum.
6	CLKOUT[1]	Buffered clock output
7	VDD	3.3V supply
8	CLKOUT[1,3]	Buffered clock output

Notes:
1. Weak pull-down on all outputs. 2. Weak pull-up on these inputs
3. This output is driven and has an internal feedback for the PLL.
4. Buffered clock outputs are Timing-Safe™

Spread Spectrum Control and Input-Output Skew Table
(Note: The values given in the table are for an input frequency of 32 MHz)

Device	SS%	Deviation	Input-Output Skew($\pm T_{SKEW}$)
ASM3P623S01B	0	±0.25 %	0.125
	1	±0.5 %	0.25
ASM3P623S01C	0	±.125 %	0.125
	1	±0.25 %	0.25
ASM3P623S01J	0	±0.125 %	0.125
	1	±0.25 %	0.25

Note: T_{SKEW} is measured in units of the Clock Period

Absolute Maximum Rating

Symbol	Parameter	Rating	Unit
VDD	Voltage on any pin with respect to Ground	-0.5 to +4.6	V
T_{STG}	Storage temperature	-65 to +125	°C
T_s	Max. Soldering Temperature (10 sec)	260	°C
T_J	Junction Temperature	150	°C
T_{DV}	Static Discharge Voltage (As per JEDEC STD22- A114-B)	2	KV

Note: These are stress ratings only and are not implied for functional use. Exposure to absolute maximum ratings for prolonged periods of time may affect device reliability.

Operating Conditions for ASM3P623S01B/C/J Devices

Parameter	Description	Min	Max	Unit
VDD	Supply Voltage	3.0	3.6	V
T_A	Operating Temperature (Ambient Temperature)	-40	+85	°C
C_L	Load Capacitance		30	pF
C_{IN}	Input Capacitance		7	pF

Electrical Characteristics for ASM3P623S01B/C/J

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
V_{IL}	Input LOW Voltage[5]				0.8	V
V_{IH}	Input HIGH Voltage[5]		2.0			V
I_{IL}	Input LOW Current	V_{IN} = 0V			50	µA
I_{IH}	Input HIGH Current	V_{IN} = VDD			100	µA
V_{OL}	Output LOW Voltage[6]	I_{OL} = 8mA			0.4	V
V_{OH}	Output HIGH Voltage[6]	I_{OH} = -8mA	2.4			V
I_{DD}	Supply Current	Unloaded outputs		15		mA
Z_o	Output Impedance			23		Ω

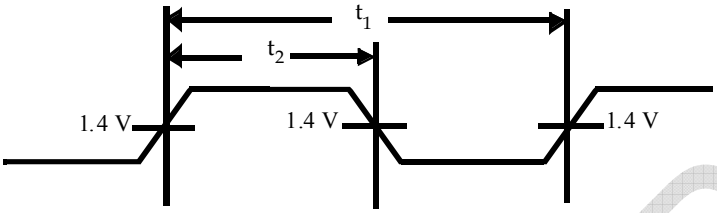
Switching Characteristics for ASM3P623S01B/C/J[7]

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
$1/t_1$	Output Frequency	30pF load	20		50	MHz
	Duty Cycle [6] = (t_2 / t_1) * 100	Measured at VDD/2	40	50	60	%
t_3	Output Rise Time [6]	Measured between 0.8V and 2.0V			2.5	nS
t_4	Output Fall Time [6]	Measured between 2.0V and 0.8V			2.5	nS
t_5	Output-to-output skew [6]	All outputs equally loaded			250	pS
t_6	Delay, CLKIN Rising Edge to CLKOUT Rising Edge [6]	Measured at VDD /2			±350	pS
t_7	Device-to-Device Skew [6]	Measured at VDD/2 on the CLKOUT pins of the device			700	pS
t_J	Cycle-to-cycle jitter [6]	Loaded outputs			200	pS
t_{LOCK}	PLL Lock Time [6]	Stable power supply, valid clock presented on CLKIN pin			1.0	mS

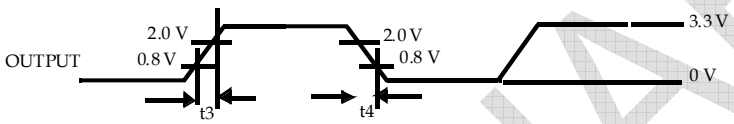
Notes:
5. CLKIN input has a threshold voltage of VDD/2
6. Parameter is guaranteed by design and characterization. Not 100% tested in production
7. All parameters specified with loaded outputs.

Switching Waveforms

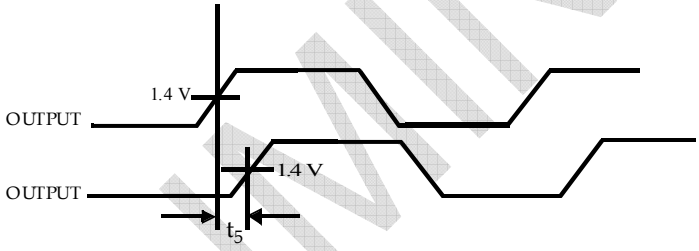
Duty Cycle Timing



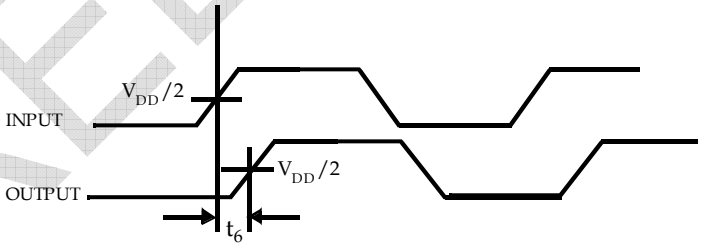
All Outputs Rise/Fall Time



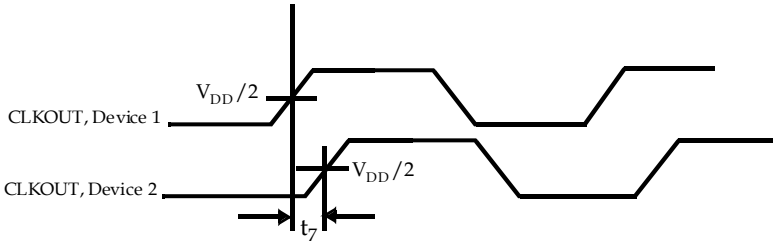
Output - Output Skew



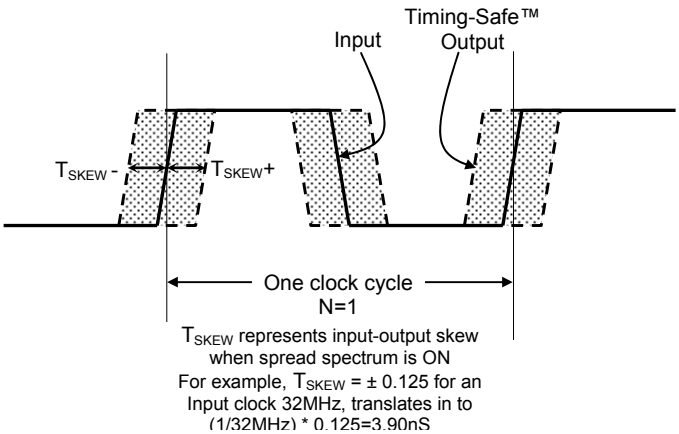
Input - Output Propagation Delay



Device - Device Skew



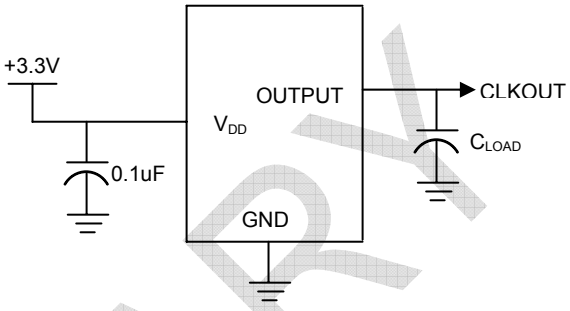
Input-Output Skew



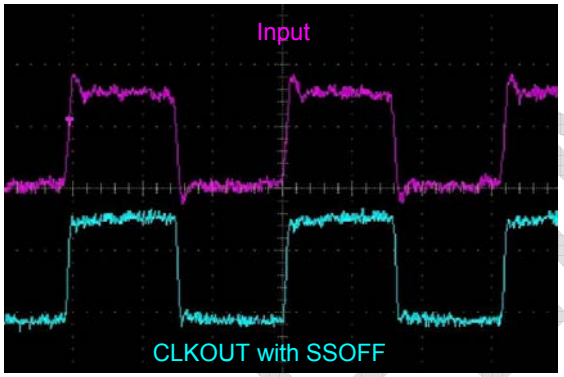
T_{SKEW} represents input-output skew when spread spectrum is ON

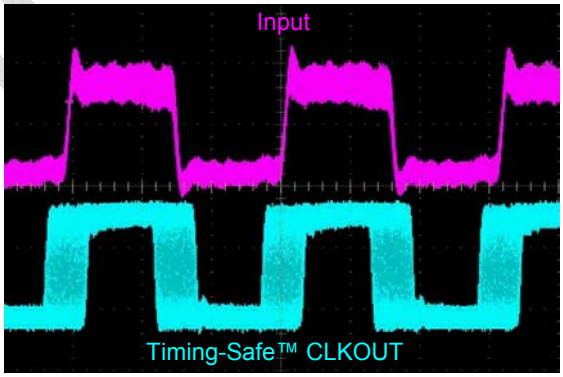
For example, T_{SKEW} = ± 0.125 for an Input clock 32MHz, translates in to (1/32MHz) * 0.125=3.90nS

Test Circuit



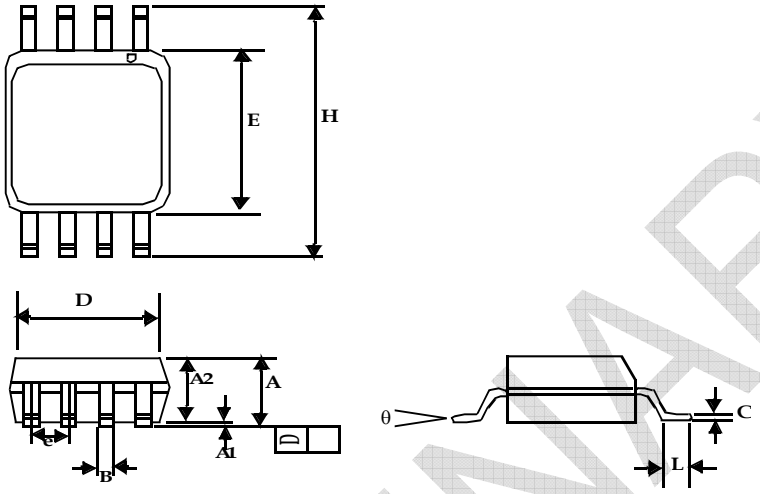
A Typical example of Timing-Safe™ waveform





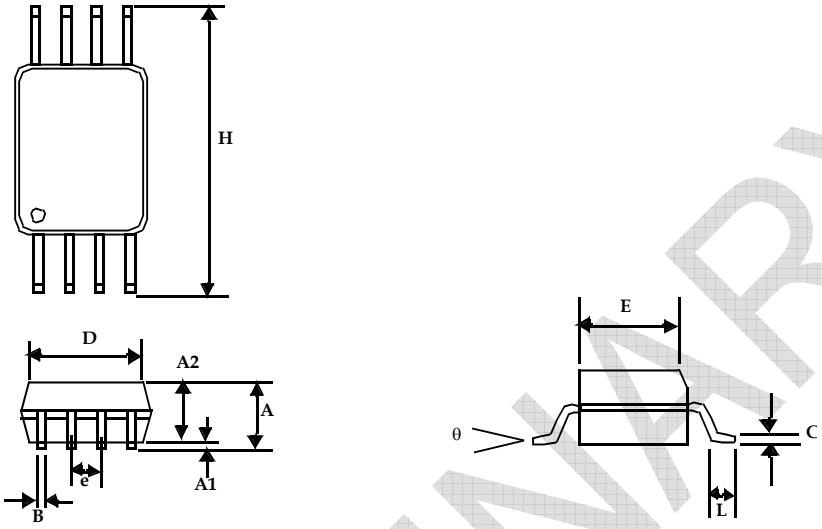
Package Information

8-lead SOIC Package(150-mil)



Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A1	0.004	0.010	0.10	0.25
A	0.053	0.069	1.35	1.75
A2	0.049	0.059	1.25	1.50
B	0.012	0.020	0.31	0.51
C	0.007	0.010	0.18	0.25
D	0.193 BSC		4.90 BSC	
E	0.154 BSC		3.91 BSC	
e	0.050 BSC		1.27 BSC	
H	0.236 BSC		6.00 BSC	
L	0.016	0.050	0.41	1.27
θ	0°	8°	0°	8°

8-lead TSSOP Package(4.40-MM Body)



Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A		0.043		1.10
A1	0.002	0.006	0.05	0.15
A2	0.033	0.037	0.85	0.95
B	0.008	0.012	0.19	0.30
c	0.004	0.008	0.09	0.20
D	0.114	0.122	2.90	3.10
E	0.169	0.177	4.30	4.50
e	0.026 BSC		0.65 BSC	
H	0.252 BSC		6.40 BSC	
L	0.020	0.028	0.50	0.70
θ	0°	8°	0°	8°

Ordering Codes

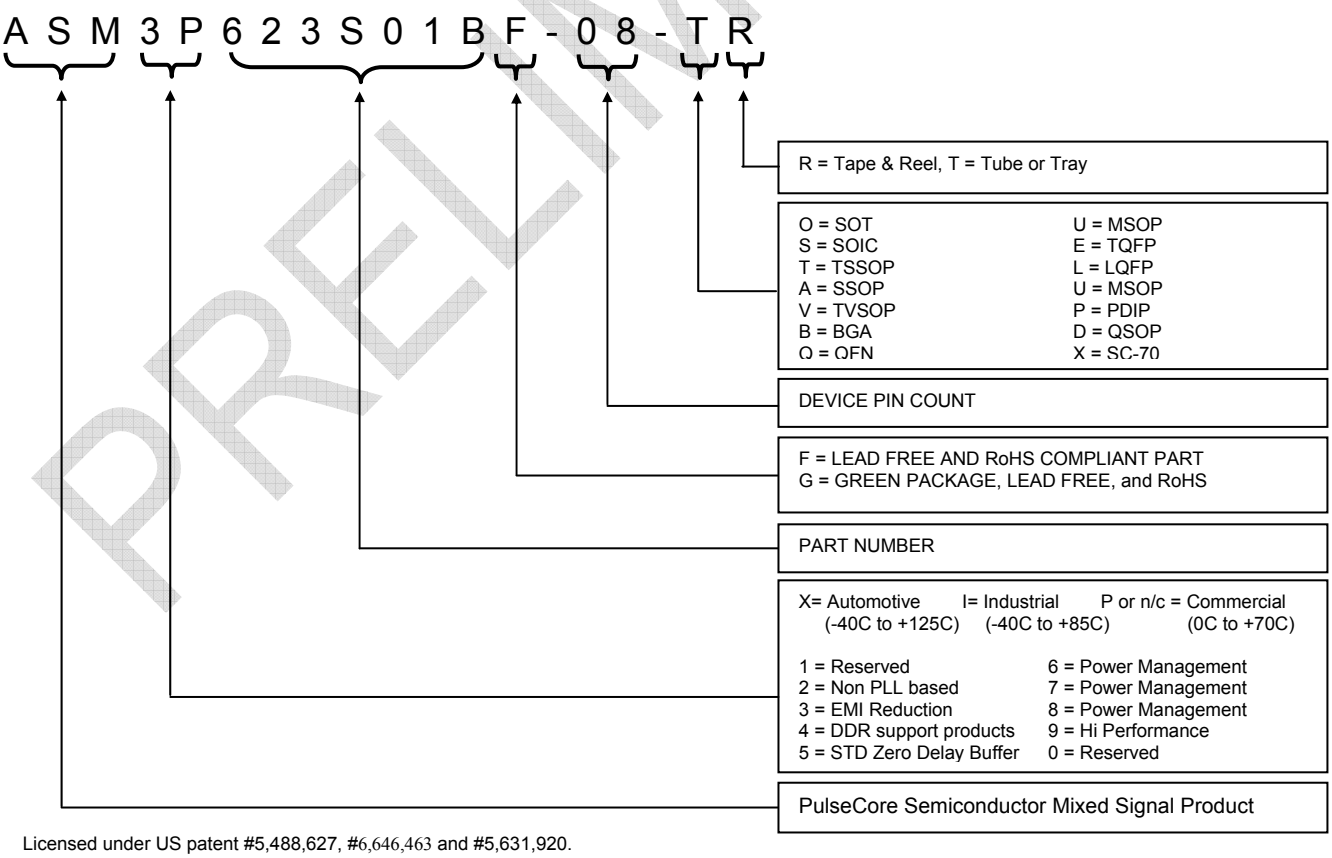
Ordering Code	Marking	Package Type	Temperature
ASM3P623S01BF-08-ST	3P623S01BF	8-pin 150-mil SOIC- TUBE, Pb Free	Commercial
ASM3I623S01BF-08-ST	3I623S01BF	8-pin 150-mil SOIC- TUBE, Pb Free	Industrial
ASM3P623S01BF-08-SR	3P623S01BF	8-pin 150-mil SOIC-TAPE & REEL, Pb Free	Commercial
ASM3I623S01BF-08-SR	3I623S01BF	8-pin 150-mil SOIC-TAPE & REEL, Pb Free	Industrial
ASM3P623S01BF-08-TT	3P623S01BF	8-pin 4.4-mm TSSOP - TUBE, Pb Free	Commercial
ASM3I623S01BF-08-TT	3I623S01BF	8-pin 4.4-mm TSSOP - TUBE, Pb Free	Industrial
ASM3P623S01BF-08-TR	3P623S01BF	8- pin 4.4-mm TSSOP - TAPE & REEL, Pb Free	Commercial
ASM3I623S01BF-08-TR	3I623S01BF	8-pin 4.4-mm TSSOP - TAPE & REEL, Pb Free	Industrial
ASM3P623S01BG-08-ST	3P623S01BG	8-pin 150-mil SOIC- TUBE, Green	Commercial
ASM3I623S01BG-08-ST	3I623S01BG	8-pin 150-mil SOIC- TUBE, Green	Industrial
ASM3P623S01BG-08-SR	3P623S01BG	8-pin 150-mil SOIC-TAPE & REEL, Green	Commercial
ASM3I623S01BG-08-SR	3I623S01BG	8-pin 150-mil SOIC-TAPE & REEL, Green	Industrial
ASM3P623S01BG-08-TT	3P623S01BG	8-pin 4.4-mm TSSOP - TUBE, Green	Commercial
ASM3I623S01BG-08-TT	3I623S01BG	8-pin 4.4-mm TSSOP - TUBE, Green	Industrial
ASM3P623S01BG-08-TR	3P623S01BG	8- pin 4.4-mm TSSOP - TAPE & REEL, Green	Commercial
ASM3I623S01BG-08-TR	3I623S01BG	8-pin 4.4-mm TSSOP - TAPE & REEL, Green	Industrial
ASM3P623S01CF-08-ST	3P623S01CF	8-pin 150-mil SOIC- TUBE, Pb Free	Commercial
ASM3I623S01CF-08-ST	3I623S01CF	8-pin 150-mil SOIC- TUBE, Pb Free	Industrial
ASM3P623S01CF-08-SR	3P623S01CF	8-pin 150-mil SOIC-TAPE & REEL, Pb Free	Commercial
ASM3I623S01CF-08-SR	3I623S01CF	8-pin 150-mil SOIC-TAPE & REEL, Pb Free	Industrial
ASM3P623S01CF-08-TT	3P623S01CF	8-pin 4.4-mm TSSOP - TUBE, Pb Free	Commercial
ASM3I623S01CF-08-TT	3I623S01CF	8-pin 4.4-mm TSSOP - TUBE, Pb Free	Industrial
ASM3P623S01CF-08-TR	3P623S01CF	8- pin 4.4-mm TSSOP - TAPE & REEL, Pb Free	Commercial
ASM3I623S01CF-08-TR	3I623S01CF	8-pin 4.4-mm TSSOP - TAPE & REEL, Pb Free	Industrial
ASM3P623S01CG-08-ST	3P623S01CG	8-pin 150-mil SOIC- TUBE, Green	Commercial
ASM3I623S01CG-08-ST	3I623S01CG	8-pin 150-mil SOIC- TUBE, Green	Industrial
ASM3P623S01CG-08-SR	3P623S01CG	8-pin 150-mil SOIC-TAPE & REEL, Green	Commercial
ASM3I623S01CG-08-SR	3I623S01CG	8-pin 150-mil SOIC-TAPE & REEL, Green	Industrial
ASM3P623S01CG-08-TT	3P623S01CG	8-pin 4.4-mm TSSOP - TUBE, Green	Commercial
ASM3I623S01CG-08-TT	3I623S01CG	8-pin 4.4-mm TSSOP - TUBE, Green	Industrial
ASM3P623S01CG-08-TR	3P623S01CG	8- pin 4.4-mm TSSOP - TAPE & REEL, Green	Commercial
ASM3I623S01CG-08-TR	3I623S01CG	8-pin 4.4-mm TSSOP - TAPE & REEL, Green	Industrial
ASM3P623S01JF-08-ST	3P623S01JF	8-pin 150-mil SOIC- TUBE, Pb Free	Commercial

rev 0.4

Ordering Codes (Cont'd)

Ordering Code	Marking	Package Type	Temperature
ASM3I623S01JF-08-ST	3I623S01JF	8-pin 150-mil SOIC- TUBE, Pb Free	Industrial
ASM3P623S01JF-08-SR	3P623S01JF	8-pin 150-mil SOIC-TAPE & REEL, Pb Free	Commercial
ASM3I623S01JF-08-SR	3I623S01JF	8-pin 150-mil SOIC-TAPE & REEL, Pb Free	Industrial
ASM3P623S01JF-08-TT	3P623S01JF	8-pin 4.4-mm TSSOP - TUBE, Pb Free	Commercial
ASM3I623S01JF-08-TT	3I623S01JF	8-pin 4.4-mm TSSOP - TUBE, Pb Free	Industrial
ASM3P623S01JF-08-TR	3P623S01JF	8- pin 4.4-mm TSSOP - TAPE & REEL, Pb Free	Commercial
ASM3I623S01JF-08-TR	3I623S01JF	8-pin 4.4-mm TSSOP - TAPE & REEL, Pb Free	Industrial
ASM3P623S01JG-08-ST	3P623S01JG	8-pin 150-mil SOIC- TUBE, Green	Commercial
ASM3I623S01JG-08-ST	3I623S01JG	8-pin 150-mil SOIC- TUBE, Green	Industrial
ASM3P623S01JG-08-SR	3P623S01JG	8-pin 150-mil SOIC-TAPE & REEL, Green	Commercial
ASM3I623S01JG-08-SR	3I623S01JG	8-pin 150-mil SOIC-TAPE & REEL, Green	Industrial
ASM3P623S01JG-08-TT	3P623S01JG	8-pin 4.4-mm TSSOP - TUBE, Green	Commercial
ASM3I623S01JG-08-TT	3I623S01JG	8-pin 4.4-mm TSSOP - TUBE, Green	Industrial
ASM3P623S01JG-08-TR	3P623S01JG	8- pin 4.4-mm TSSOP - TAPE & REEL, Green	Commercial
ASM3I623S01JG-08-TR	3I623S01JG	8-pin 4.4-mm TSSOP - TAPE & REEL, Green	Industrial

Device Ordering Information



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Part Number: ASM3P623S00B/C/J
Document Version: 0.4

Note: This product utilizes US Patent # 6,646,463 Impedance Emulator Patent issued to PulseCore Semiconductor, dated 11-11-2003
Timing-Safe™ US Patent Pending.