SA56

FEATURES

- DELIVERS UP TO 5A CONTINUOUS OUTPUT
- OPERATES AT SUPPLY VOLTAGES UP TO 60V
- NO "SHOOT-THROUGH" CURRENT
- THERMAL SHUTDOWN (OUTPUTS OFF) AT 160°C
- SHORTED LOAD PROTECTION (to V_S or P_{GND} or SHORTED LOAD)
- NO BOOTSTRAP CAPACITORS REQUIRED
- PROGRAMMABLE ONBOARD PWM

APPLICATIONS

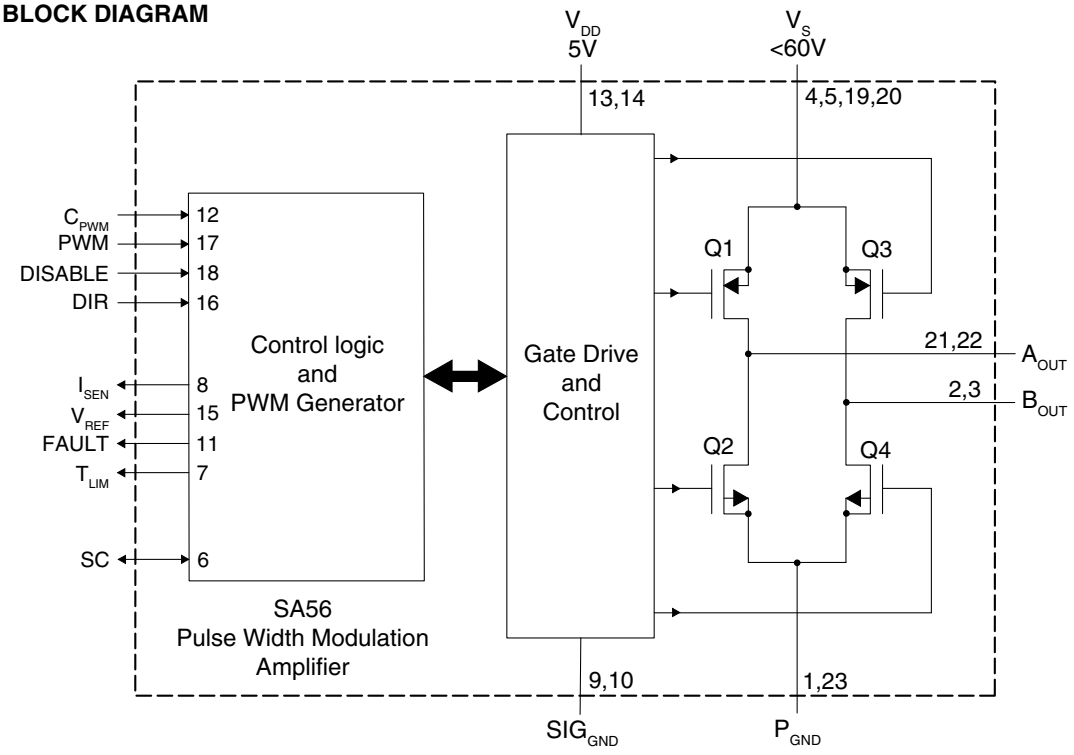
- DC BRUSH-TYPE MOTOR DRIVES
- POSITION AND VELOCITY SERVOMECHANISMS
- FACTORY AUTOMATION ROBOTS
- NUMERICALLY CONTROLLED MACHINERY
- COMPUTER PRINTERS AND PLOTTERS

23 PIN SIP
PACKAGE STYLE EX

DESCRIPTION

The SA56 is a 5-ampere PWM Amplifier designed for motion control applications. The device is built using a multi-technology process that combines bipolar and CMOS control circuitry with DMOS power devices in a single monolithic structure. Ideal for driving DC and stepper motors, the SA56 accommodates peak output currents up to 10 amperes. An innovative circuit that facilitates low-loss sensing of the output current has been implemented. An on-board PWM oscillator and comparator are used to convert an analog signal into PWM direction of rotation and magnitude for motor control applications. TTL or CMOS digital inputs allow direct external control in 2-quadrant or 4-quadrant modes.

FIGURE 1. BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

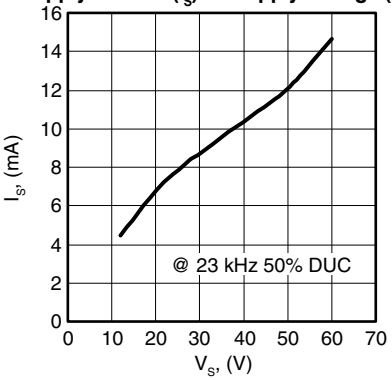
SUPPLY VOLTAGE, V_{DD}	5.5V
SUPPLY VOLTAGE, V_S	60V
PEAK OUTPUT CURRENT (100mS)	10A
CONTINUOUS OUTPUT CURRENT	5A
POWER DISSIPATION	125W
POWER DISSIPATION (T_A = 25°C, Free Air)	10W
JUNCTION TEMPERATURE, $T_{J(MAX)}$	150°C
ESD SUSCEPTIBILITY (Logic Pins Only)	1500V
STORAGE TEMPERATURE, T_{STG}	–40°C to +150°C
LEAD TEMPERATURE (Soldering, 10 sec.)	300°C
JUNCTION TEMPERATURE, T_J	–40°C to +150°C

SPECIFICATIONS

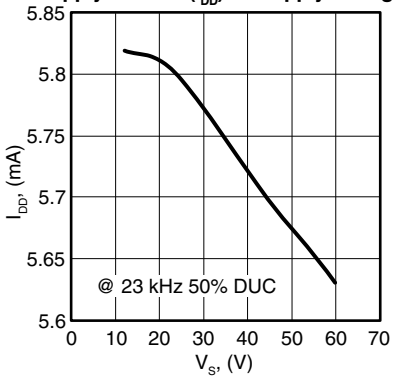
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_S		12		60	V
VDD		4.5		5.5	V
SWITCH ON RESISTANCE, R_{DS}(ON) N-Channel	Output Current = 5A		0.23	0.6	Ω
SWITCH ON RESISTANCE, R_{DS}(ON) P-Channel	Output Current = 5A		0.27	0.6	Ω
CLAMP DIODE FORWARD DROP, V_{CLAMP}	Clamp Current = 5A		1.43		V
LOGIC LOW INPUT VOLTAGE, V_{IL}		-0.5		0.8	V
LOGIC LOW INPUT CURRENT, I_{IL}	V_{IN} = –0.1V	-10		+10	µA
LOGIC HIGH INPUT VOLTAGE, V_{IH}		2		V_{DD}	V
LOGIC HIGH INPUT CURRENT, I_{IH}	V_{IN} = 5.5V	-10		10	µA
CURRENT SENSE OUTPUT	I_{OUT} = 1A	180	240	300	µA
	I_{OUT} = 5A	.79	1.0	1.32	mA
CURRENT SENSE LINEARITY ERROR	1A ≤ I_{OUT} ≤ 5A		±1	±5	%
	100 mA ≤ I_{OUT} ≤ 5A			±8	%
	5A ≤ I_{OUT} ≤ 10A (Peak Currents only)			±8	%
SHUTDOWN TEMPERATURE, T_{JSD}	Outputs Turn OFF		160		°C
QUIESCENT SUPPLY CURRENT, I_S	No Load, F_{SW} = 100kHz 50% DUC		26	50	mA
QUIESCENT SUPPLY CURRENT, I_{DD}	No Load, F_{SW} = 100kHz 50% DUC		6	15	mA
OUTPUT TURN-ON DELAY TIME, t_{Don}	No Load		200		ns
OUTPUT TURN-ON SWITCHING TIME, t_{on}	No Load		41		ns
OUTPUT TURN-OFF DELAY TIMES, t_{Doff}	No Load		272		ns
OUTPUT TURN-OFF SWITCHING TIME, t_{off}	No Load		46		ns
MINIMUM INPUT PULSE WIDTH, t_p (DIGITAL MODE)	No Load		140		ns
REFERENCE VOLTAGE	I_{REF} = 1mA	2.3	2.5	2.7	V
Vref OUTPUT CURRENT (Vref 2.5V), I_{REF}	Source Only, No current sink capability			1	mA
ANALOG INPUT RANGE FOR FULL MODULATION	Load Current = 400µA	1		4	V
HIGH CURRENT SHUTDOWN RESPONSE	Output shorted (No bypass capacitor at SCin pin)		250	800	ns
THERMAL					
RESISTANCE, Junction to Case	Full Temperature Range		1		°C/W
RESISTANCE, Junction to Air	Full Temperature Range		12.21		°C/W
TEMPERATURE RANGE, Case		-40		125	°C

NOTE: These specifications apply for V_S = 50V and V_{DD} = 5V at 25°C, unless otherwise specified.

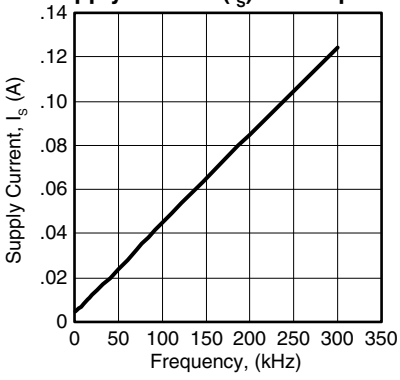
Supply Current (I_S) vs Supply Voltage (V_S)



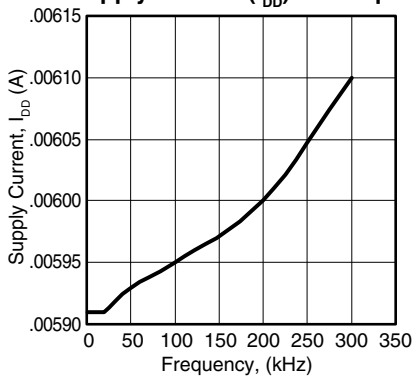
5V Supply Current (I_{DD}) vs Supply Voltage (V_S)



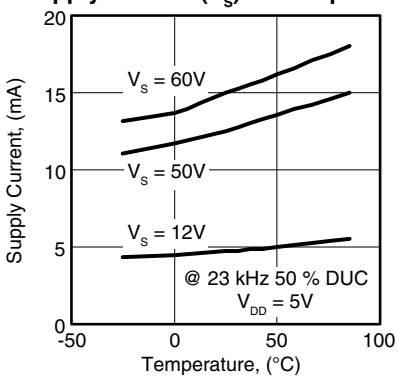
Supply Current (I_S) vs Frequency



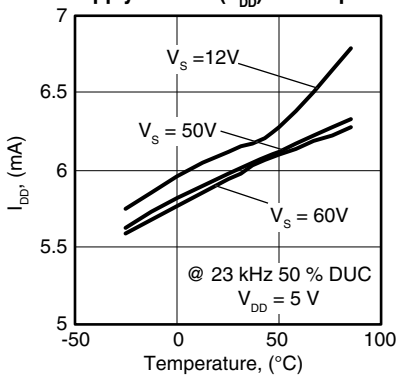
5V Supply Current (I_{DD}) vs Frequency



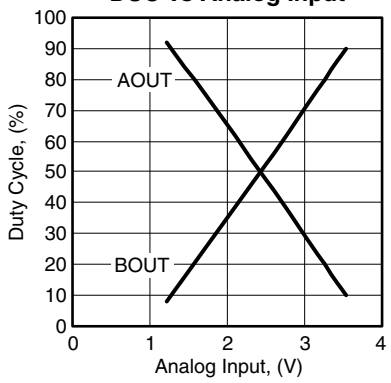
Supply Current (V_S) vs Temperature



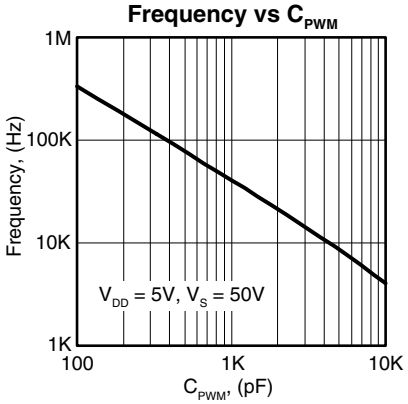
5V Supply Current (V_{DD}) vs Temperature



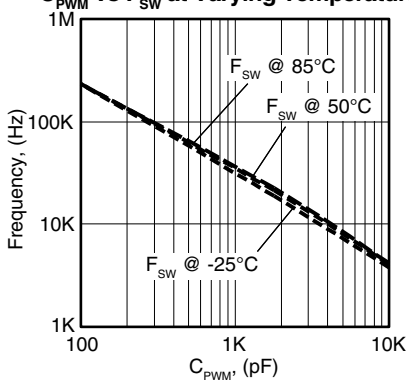
DUC vs Analog Input



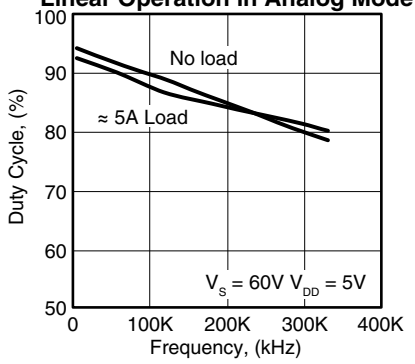
Frequency vs C_{PWM}



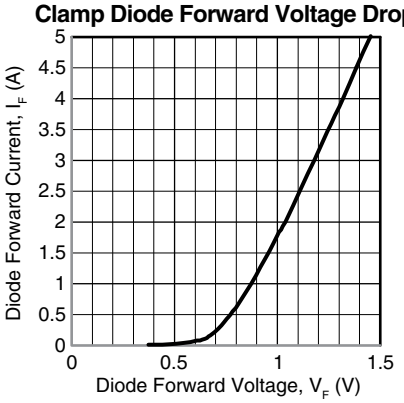
C_{PWM} vs F_{SW} at Varying Temperatures



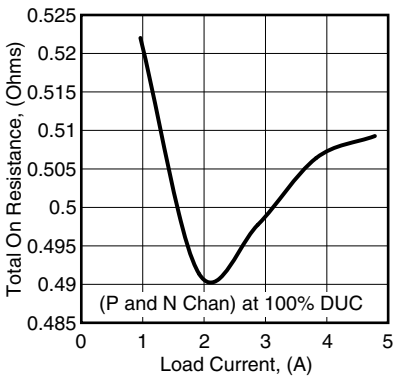
Maximum Duty Cycle for Linear Operation in Analog Mode

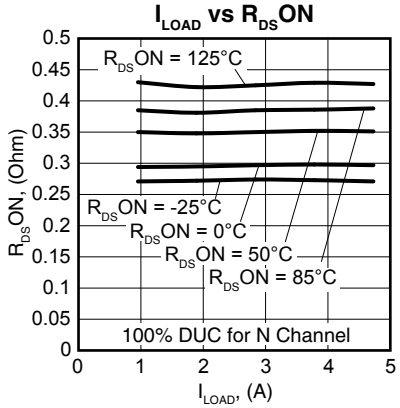


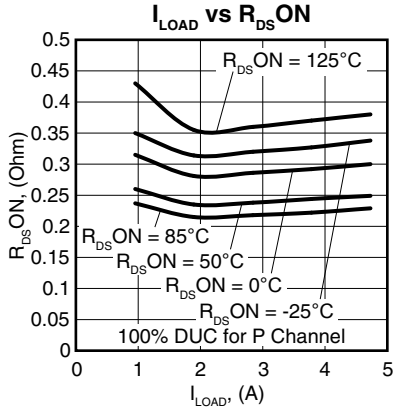
Clamp Diode Forward Voltage Drop

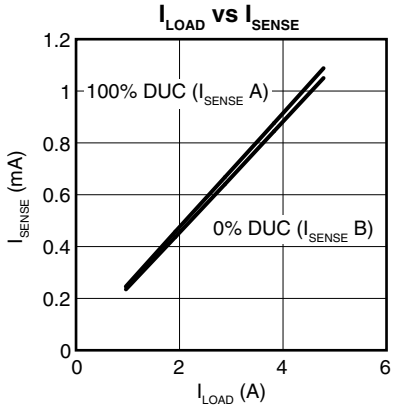


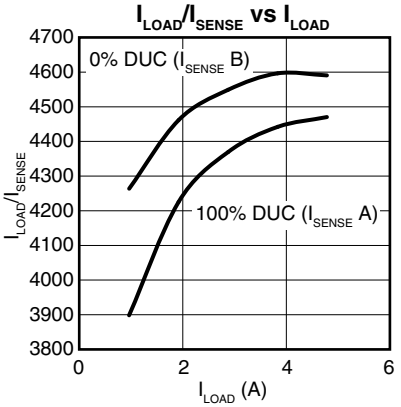
Load Current vs Total On Resistance

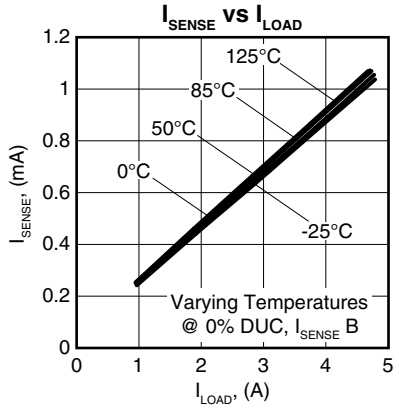


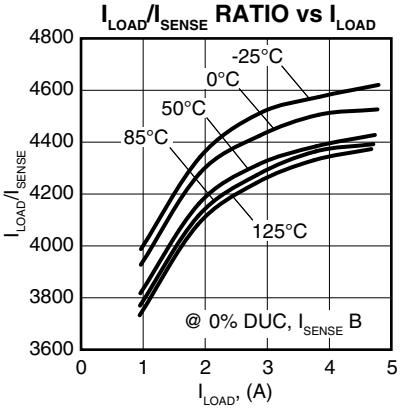

I_{LOAD} vs $R_{DS}ON$
$R_{DS}ON$ = 125°C
$R_{DS}ON$ = -25°C
$R_{DS}ON$ = 0°C
$R_{DS}ON$ = 50°C
$R_{DS}ON$ = 85°C
100% DUC for N Channel
$R_{DS}ON$, (Ohm)
I_{LOAD}, (A)

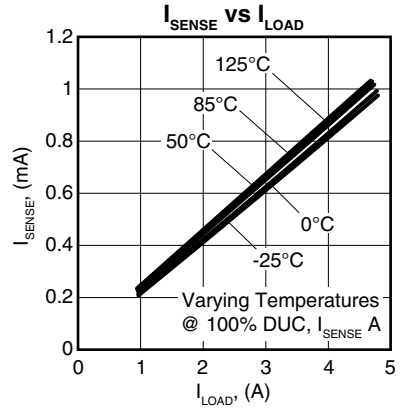

I_{LOAD} vs $R_{DS}ON$
$R_{DS}ON$ = 125°C
$R_{DS}ON$ = 85°C
$R_{DS}ON$ = 50°C
$R_{DS}ON$ = 0°C
$R_{DS}ON$ = -25°C
100% DUC for P Channel
$R_{DS}ON$, (Ohm)
I_{LOAD}, (A)

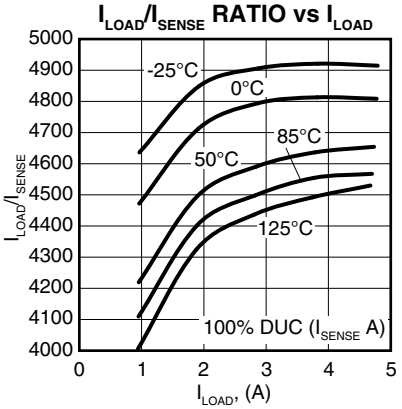

I_{LOAD} vs I_{SENSE}
100% DUC (I_{SENSE} A)
0% DUC (I_{SENSE} B)
I_{SENSE} (mA)
I_{LOAD} (A)

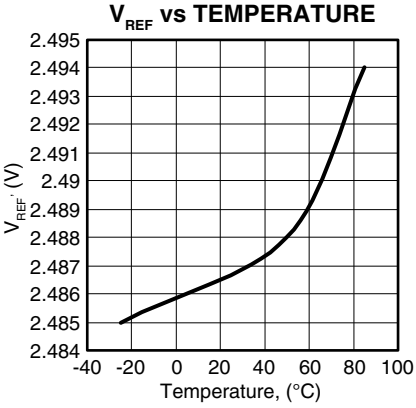

I_{LOAD}/I_{SENSE} vs I_{LOAD}
0% DUC (I_{SENSE} B)
100% DUC (I_{SENSE} A)
I_{LOAD}/I_{SENSE}
I_{LOAD} (A)


I_{SENSE} vs I_{LOAD}
125°C
85°C
50°C
0°C
-25°C
Varying Temperatures
@ 0% DUC, I_{SENSE} B
I_{SENSE}, (mA)
I_{LOAD}, (A)


I_{LOAD}/I_{SENSE} RATIO vs I_{LOAD}
-25°C
0°C
50°C
85°C
125°C
@ 0% DUC, I_{SENSE} B
I_{LOAD}/I_{SENSE}
I_{LOAD}, (A)


I_{SENSE} vs I_{LOAD}
125°C
85°C
50°C
0°C
-25°C
Varying Temperatures
@ 100% DUC, I_{SENSE} A
I_{SENSE}, (mA)
I_{LOAD}, (A)


I_{LOAD}/I_{SENSE} RATIO vs I_{LOAD}
-25°C
0°C
85°C
50°C
125°C
100% DUC (I_{SENSE} A)
I_{LOAD}/I_{SENSE}
I_{LOAD}, (A)


V_{REF} vs TEMPERATURE
V_{REF}, (V)
Temperature, (°C)

GENERAL

Please read "SA56 Design Ideas" that covers the various SA56 applications in considerable detail. Also see Application Note 1 "General Operating Considerations" which covers stability, power supplies, heat sinking, mounting, and specification interpretation. Visit www.apexmicrotech.com for design tools that help automate tasks such as calculations for stability, internal power dissipation, current limit, heat sink selection, Apex's complete Application Notes library, Technical Seminar Workbook and Evaluation Kits.

GROUND PINS

The two SIG_{GND} pins, 9 & 10, are for input signal grounds. Pins 1 and 23, P_{GND}, are power grounds. The P_{GND} & SIG_{GND} pins are connected at one point inside the IC. It is also recommended the user connect both pins at a single point on the board in a way that no current flows through that connection.

POWER SUPPLY BYPASSING

Bypass capacitors to power supply terminals V_S and V_{DD} must be connected physically close to the pins to prevent erratic, low-efficiency operation and excessive ringing at the outputs. Electrolytic capacitors, at least 10 µF per output ampere are required for suppressing V_S to P_{GND} noise. High quality ceramic capacitors (X7R) 1 µF or greater should also be used. Only capacitors rated for switching applications should be considered. The bypass capacitors must be located as close to the power supply pins as possible. Due to the very fast switching times of the outputs, the inductance of 1 inch of circuit trace could cause noticeable degradation in performance. The bypassing requirements of V_{DD} are less stringent, but still necessary. A 0.1 µF to 0.47 µF capacitor connected directly between the V_{DD} and SIG_{GND} pins will suffice.

PIN DESCRIPTIONS

Pin #	Name	Description
1,23	P_{GND}	Power high current ground return path of the motor.
2,3	B_{OUT}	Half bridge output B
4,5, 19,20	V_S	High voltage supply
6	SC	The short-circuit protection circuits will sense a direct short from either output (A_{OUT} or B_{OUT}) to P_{GND} or V_S – as well as across the load. If the high-current protection circuit engages it will place all four MOSFETs in the tristate state (high-impedance output). The SC output, pin 6, will go HIGH though not latch, thereby denoting that this protection feature has been triggered.
7	T_{LIM}	Temperature limit, CMOS. This pin can be used as a flag for an over-temperature condition. Under normal operation this pin will be logic low. When a junction temperature exceeds approximately 160°C this pin will change to logic high and the output will be latched off. Grounding this pin disables over temperature protection. This pin should be left open if over temperature protection is desired but the flag is not used.
8	I_{SEN}	Current Sense output and programmable current limit. A current proportional to the output current is sourced by this pin. Typically this pin is connected to a resistor for programmable current limit or transconductance operation.
9,10	SIG_{GND}	Ground connection for all internal digital and low-current analog circuitry.
11	FAULT	This pin latches high whenever the four MOSFETs have been placed in the tristate condition which occurs when either the high-current or the thermal protection has engaged.
12	C_{PWM}	An external timing capacitor is connected to this pin to set the frequency of the internal oscillator and ramp generator for analog control mode. The capacitor value (pF) = $4.05x10^7/F_{SW}$, where F_{SW} = the desired switching frequency. This pin is grounded for digital control mode.
13,14	V_{DD}	5V supply for input logic and low voltage analog circuitry.
15	V_{REF}	Reference voltage. Can be used at low current for biasing analog loop circuits.
16	DIR	Direction of rotation control; In 2 quadrant, digital control, determines the active output FETs. This pin should be grounded in analog control mode.
17	PWM	CMOS/TTL input for digital PWM control, or 1-4V analog input for duty cycle control in analog control mode.
18	DISABLE	Following a fault, pulling the DISABLE pin HIGH and then LOW will reset a latched fault condition. (When pulled HIGH, all four output MOSFETs are disabled. A logic LOW on this pin allows the four output FETs to function normally.) When the DISABLE and FAULT pins are tied to a microcontroller, the FAULT pin will generate an interrupt in the microcontroller, so that the interrupt, can in turn, generate a pulse on the DISABLE pin. When a fault occurs, the SA56 fault circuitry will be reset.
21,22	A_{OUT}	Half bridge output A

MODES OF OPERATION

The following chart shows the 3 modes of operation.

Mode	C_{PWM} pin 12	PWM pin 17	DIR pin 16	A_{OUT} pins 21, 23	B_{OUT} pins 2, 3
2 Quadrant – Analog Mode	Connect capacitor to set frequency	Analog control voltage (1 – 4V)	Low (SIG_{GND})	Control voltage greater than V_{REF}: $(A_{OUT} - B_{OUT}) < 0$ average voltage	Control voltage greater than V_{REF}: $(B_{OUT} - A_{OUT}) > 0$ average voltage
2 Quadrant – Digital Mode	SIG_{GND}	Modulation In	High (V_{DD})	High (V_S)	$\overline{PWM}$
	SIG_{GND}	Modulation In	Low (SIG_{GND})	$\overline{PWM}$	High (V_S)
4 Quadrant – Digital Mode	SIG_{GND}	High (V_{DD})	Modulated In	DIR	$\overline{DIR}$

4-QUADRANT - ANALOG MODE

The SA56 can operate in 4-quadrant mode with analog or digital inputs. In the analog mode, the capacitor from C_{PWM} to SIG_{GND} sets the frequency of an internal triangular ramp signal. See Figure 2. An analog voltage applied to the PWM pin is compared to a 2.5 volt reference within the SA56 thereby governing the duty cycle of the output. Note that the analog pin DIR pin 16 is connected to signal ground (SIG_{GND}).

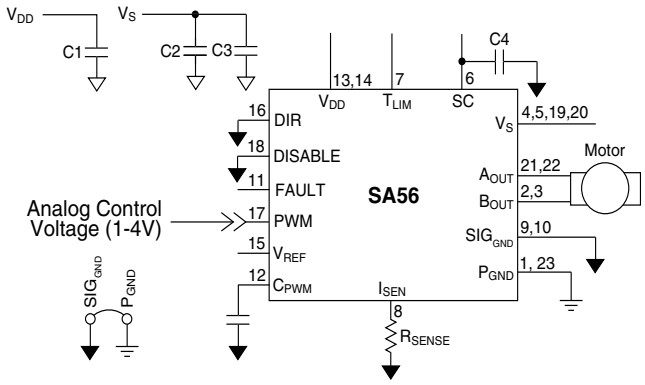


FIGURE 2. 4–QUADRANT ANALOG OPERATION

OPERATING WITH DIGITAL INPUTS

Two and 4-quadrant operation are possible with the SA56 when driven with a digital PWM signal from a microcontroller or DSP. When using a digital modulation signal, tie the C_{PWM} pin to SIG_{GND} to disable the internal oscillator and ramp generator. When operating in the digital mode, pulse widths should be no less than 100 ns and the switching frequency should remain less than 500 kHz. This will allow enough time for the output MOSFETs to reach their full on and off states before receiving a command to reverse state.

2-QUADRANT - DIGITAL MODE

Two-quadrant operation of the FETs is realized by driving PWM pin 17 of the SA56 with a digital PWM signal supplied by a microcontroller or DSP, as depicted in Figure 3. When using a digital modulation signal, connect the C_{PWM} pin to SIG_{GND} to disable the internal oscillator and its companion ramp generator.

A digital PWM signal applied to the PWM pin controls the output duty cycle at one output pin while the other output pin is held "HIGH". The input at the DIR pin (V_{DD} or SIG_{GND}) governs the output behavior. If DIR is a logic HIGH, the A_{OUT} output will be held high and the B_{OUT} output will be switched as the complement of the PWM input signal. The average output at A_{OUT} will always be greater than at B_{OUT}. Whereas if DIR is a logic LOW, the B_{OUT} output will be held "HIGH" and the A_{OUT} output will be switched.

Operating in two-quadrant mode reduces switching noise and power dissipation, but limits the ability to control the motor at very low speed.

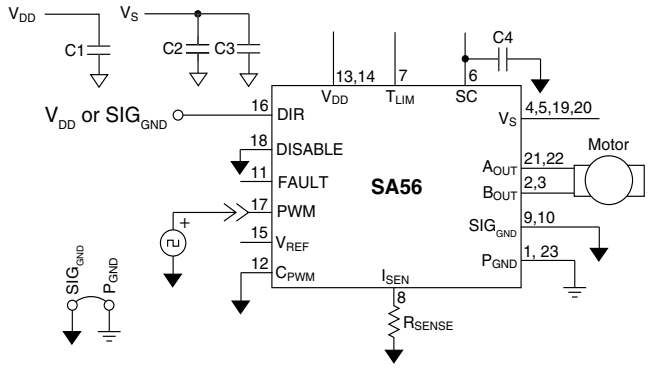


FIGURE 3. 2-QUADRANT – DIGITAL MODE

4 QUADRANT DIGITAL MODE

During four-quadrant operation a single digital PWM input includes magnitude and direction information. The digital PWM input signal is applied to the DIR pin, as shown in Figure 4, and the PWM pin is tied HIGH to V_{DD}. Both pairs of output MOSFETs will switch in a locked, complementary fashion.

With a 50% duty cycle the average voltage of outputs A_{OUT} and B_{OUT} will be the same, which is half of V_S so that the average differential voltage over each period applied to the load will therefore be zero.

Four-quadrant operation allows for smooth transitions through zero current for low-speed applications. However, power dissipation is slightly higher than in two-quadrant operation since all four output MOSFETs must switch every cycle.

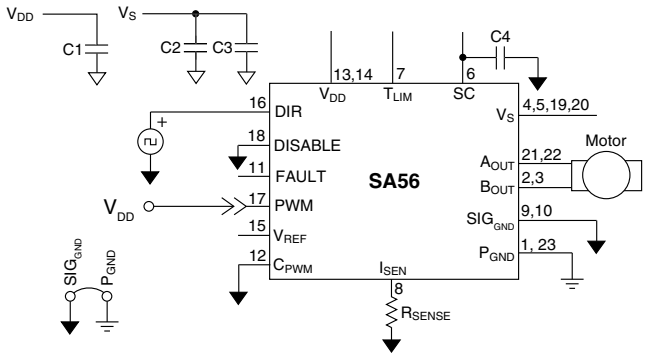


FIGURE 4. 4-QUADRANT – DIGITAL MODE

BRAKING – DIGITAL MODE

Under digital control, the SA56 can rapidly decelerate the motor by shunting the winding currents through the output MOSFETs. Logic LOW on the PWM input both A and B outputs high. The motor winding current circulates through the on resistance of the MOSFETs quickly slowing the motor.

The winding current can be monitored with the I_{SEN} pin during the braking of the motor. However, the current during braking circulates in the normal forward direction through one output MOSFET and is in the reverse in the other MOSFET. The current sense feature can measure only forward currents. The logic input on the DIR pin dictates which output MOSFET is used for sensing the forward current during braking.

PROTECTION CIRCUITS

The most severe condition for any power device is a direct, hard-wired ("screwdriver") short from an output to ground. While the short-circuit protection will latch the output MOSFETs within 500 ns (typical), the die and package may be required to dissipate up to 500 Watts of power until the protection circuits are activated.

This energy can be destructive, particularly at higher operating voltages, so sound thermal design is critical if fault tolerance is to be established in the design. The V_S and P_{GND} pins may become very hot during this period of high current.

Thermal and short-circuit protection are included in the SA56 to prevent damage in the event that faults occur as described below:

Short-circuit protection – The short-circuit protection circuits will sense a direct short from either output (A_{OUT} or B_{OUT}) to P_{GND} or V_S – as well as across the load. If the high-current protection circuit engages, it will place all four MOSFETs in the tristate state (high-impedance output). The SC output, pin 6, will go HIGH though not latch, thereby denoting that this protection feature has been triggered.

Over-current protection – When the current on the high side goes above 10 amperes peak, the over-current circuit tristates so that the four MOSFETs go into a latched fault condition.

Thermal protection – The thermal protection circuits will engage if the temperature of any of the four MOSFETs reaches approximately 160°C. If this occurs, the FAULT output pin will go HIGH. If the thermal protection circuit engages, it will place all four MOSFETs in the tristate state (high-impedance output). The T_{LIM} output which is normally LOW will go HIGH, though not latch, thereby denoting which of the protection features has been triggered.

PROGRAMMABLE CURRENT LIMIT

The I_{SEN} pin sources a current proportional to the forward output current of the active P channel output MOSFET. The proportionality is approximately 200 microamperes per ampere of output current. Note that the I_{SEN} output is blocked during the switching transitions when current spikes are likely to be significant.

To create a programmable current limit, connect a resistor from I_{SEN} to SIG_{GND}. If the voltage across this resistor exceeds an internally-generated 2.75V threshold, all four output MOSFETs will be turned off for the remainder of the switching cycle. A 2.7k-Ohm resistor will set the current limit at approximately 5 amperes.

The I_{SEN} output can also be used for maintaining a current control loop in torque motor applications.

CURRENT SENSE LINEARITY CALCULATION

The current sense linearity is specified in the table on page 2 and is calculated using the method described below:

a) Define a straight line (y = mx + b) joining the two end data points where, m is the slope and b is the offset or zero crossover. Calculate the slope m and offset c using the extreme data points. Assume I_{SENSE} in the y axis and I_{LOAD} in the x axis.

b) Calculate linear I_{SEN} (or ideal I_{SENSE} value, IS_{IDEAL}) using the straight line equation derived in step (a) for the I_{LOAD} data points.

c) Determine deviation from linear I_{SEN} (step (b) and actual measured I_{SENSE} value (IS_{ACTUAL}) as shown below:

$$\text{Linearity Error (\%)} = \frac{IS_{IDEAL} - IS_{ACTUAL}}{IS_{IDEAL}} \times 100$$

This data sheet has been carefully checked and is believed to be reliable, however, no responsibility is assumed for possible inaccuracies or omissions. All specifications are subject to change without notice.