

NTLJD3181PZ

Power MOSFET

-20 V, -4.0 A, μ Cool™ Dual P-Channel, ESD, 2x2 mm WDFN Package

Features

- WDFN 2x2 mm Package with Exposed Drain Pads for Excellent Thermal Conduction
- Lowest $R_{DS(on)}$ Solution in 2x2 mm Package
- Footprint Same as SC-88 Package
- Low Profile (< 0.8 mm) for Easy Fit in Thin Environments
- ESD Protected
- This is a Pb-Free Device

Applications

- Optimized for Battery and Load Management Applications in Portable Equipment
- Li-Ion Battery Charging and Protection Circuits
- High Side Load Switch

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

| Parameter | Symbol | Value | Unit | |
|---|------------------------|--------------------------|------|------------------|
| Drain-to-Source Voltage | V_{DSS} | -20 | V | |
| Gate-to-Source Voltage | V_{GS} | ± 8.0 | V | |
| Continuous Drain Current (Note 1) | Steady State | $T_A = 25^\circ\text{C}$ | -3.2 | A |
| | | $T_A = 85^\circ\text{C}$ | -2.3 | |
| | $t \leq 5 \text{ s}$ | $T_A = 25^\circ\text{C}$ | -4.0 | |
| Power Dissipation (Note 1) | Steady State | $T_A = 25^\circ\text{C}$ | 1.5 | W |
| | | $t \leq 5 \text{ s}$ | 2.3 | |
| Continuous Drain Current (Note 2) | Steady State | $T_A = 25^\circ\text{C}$ | -2.2 | A |
| | | $T_A = 85^\circ\text{C}$ | -1.6 | |
| Power Dissipation (Note 2) | Steady State | $T_A = 25^\circ\text{C}$ | 0.71 | W |
| Pulsed Drain Current | $t_p = 10 \mu\text{s}$ | I_{DM} | -16 | A |
| Operating Junction and Storage Temperature | T_J, T_{STG} | -55 to 150 | | $^\circ\text{C}$ |
| Source Current (Body Diode) (Note 2) | I_S | -1.0 | | A |
| Lead Temperature for Soldering Purposes (1/8" from case for 10 s) | T_L | 260 | | $^\circ\text{C}$ |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

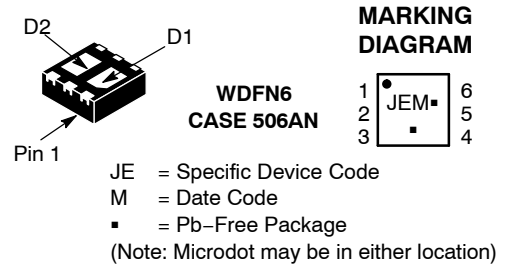
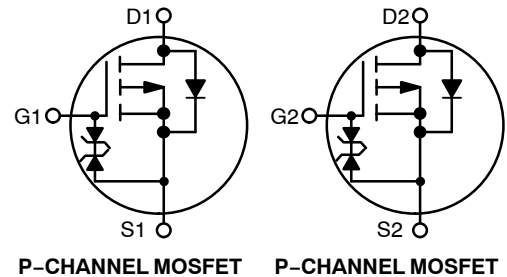
1. Surface Mounted on FR4 Board using 1 in sq pad size (Cu area = 1.127 in sq [2 oz] including traces).
2. Surface Mounted on FR4 Board using the minimum recommended pad size of 30 mm², 2 oz Cu.



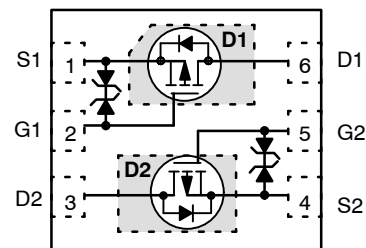
ON Semiconductor®

<http://onsemi.com>

| $V_{(BR)DSS}$ | $R_{DS(on)}$ MAX | I_D MAX (Note 1) |
|---------------|-------------------------|--------------------|
| -20 V | 100 m Ω @ -4.5 V | -4.0 A |
| | 144 m Ω @ -2.5 V | |
| | 200 m Ω @ -1.8 V | |



PIN CONNECTIONS



ORDERING INFORMATION

| Device | Package | Shipping† |
|----------------|-----------------|------------------|
| NTLJD3181PZTAG | WDFN6 (Pb-Free) | 3000/Tape & Reel |
| NTLJD3181PZTBG | WDFN6 (Pb-Free) | 3000/Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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THERMAL RESISTANCE RATINGS

| Parameter | Symbol | Max | Unit |
|-----------|--------|-----|------|
|-----------|--------|-----|------|

SINGLE OPERATION (SELF-HEATED)

| | | | |
|---|-----------------|-----|------|
| Junction-to-Ambient – Steady State (Note 3) | $R_{\theta JA}$ | 83 | °C/W |
| Junction-to-Ambient – Steady State Min Pad (Note 4) | $R_{\theta JA}$ | 177 | |
| Junction-to-Ambient – $t \leq 5$ s (Note 3) | $R_{\theta JA}$ | 54 | |

DUAL OPERATION (EQUALLY HEATED)

| | | | |
|---|-----------------|-----|------|
| Junction-to-Ambient – Steady State (Note 3) | $R_{\theta JA}$ | 58 | °C/W |
| Junction-to-Ambient – Steady State Min Pad (Note 4) | $R_{\theta JA}$ | 133 | |
| Junction-to-Ambient – $t \leq 5$ s (Note 3) | $R_{\theta JA}$ | 40 | |

3. Surface Mounted on FR4 Board using 1 in sq pad size (Cu area = 1.127 in sq [2 oz] including traces).
4. Surface Mounted on FR4 Board using the minimum recommended pad size (30 mm², 2 oz Cu).

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MOSFET ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|-----------|--------|-----------------|-----|-----|-----|------|
|-----------|--------|-----------------|-----|-----|-----|------|

OFF CHARACTERISTICS

| | | | | | | |
|---|-------------------|---|--------------------------|----|----------|----------------------------|
| Drain-to-Source Breakdown Voltage | $V_{(BR)DSS}$ | $V_{GS} = 0\text{ V}, I_D = -250\ \mu\text{A}$ | -20 | | | V |
| Drain-to-Source Breakdown Voltage Temperature Coefficient | $V_{(BR)DSS}/T_J$ | $I_D = -250\ \mu\text{A}$, Ref to 25°C | | 13 | | $\text{mV}/^\circ\text{C}$ |
| Zero Gate Voltage Drain Current | I_{DSS} | $V_{DS} = -16\text{ V}, V_{GS} = 0\text{ V}$ | $T_J = 25^\circ\text{C}$ | | -1.0 | μA |
| | | | $T_J = 85^\circ\text{C}$ | | -10 | |
| Gate-to-Source Leakage Current | I_{GSS} | $V_{DS} = 0\text{ V}, V_{GS} = \pm 8.0\text{ V}$ | | | ± 10 | μA |

ON CHARACTERISTICS (Note 5)

| | | | | | | |
|--|------------------|---|------|-----|------|----------------------------|
| Gate Threshold Voltage | $V_{GS(TH)}$ | $V_{GS} = V_{DS}, I_D = -250\ \mu\text{A}$ | -0.4 | | -1.0 | V |
| Gate Threshold Temperature Coefficient | $V_{GS(TH)}/T_J$ | | | 2.0 | | $\text{mV}/^\circ\text{C}$ |
| Drain-to-Source On-Resistance | $R_{DS(on)}$ | $V_{GS} = -4.5\text{ V}, I_D = -2.0\text{ A}$ | | 68 | 100 | $\text{m}\Omega$ |
| | | $V_{GS} = -2.5\text{ V}, I_D = -2.0\text{ A}$ | | 90 | 144 | |
| | | $V_{GS} = -1.8\text{ V}, I_D = -1.7\text{ A}$ | | 125 | 200 | |
| Forward Transconductance | g_{FS} | $V_{DS} = -5.0\text{ V}, I_D = -2.0\text{ A}$ | | 6.5 | | S |

CHARGES, CAPACITANCES AND GATE RESISTANCE

| | | | | | | |
|------------------------------|--------------|--|--|------|-----|-------------|
| Input Capacitance | C_{ISS} | $V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}, V_{DS} = -10\text{ V}$ | | 450 | | pF |
| Output Capacitance | C_{OSS} | | | 90 | | |
| Reverse Transfer Capacitance | C_{RSS} | | | 62 | | |
| Total Gate Charge | $Q_{G(TOT)}$ | $V_{GS} = -4.5\text{ V}, V_{DS} = -10\text{ V}, I_D = -3.8\text{ A}$ | | 5.2 | 7.8 | nC |
| Threshold Gate Charge | $Q_{G(TH)}$ | | | 0.3 | | |
| Gate-to-Source Charge | Q_{GS} | | | 0.84 | | |
| Gate-to-Drain Charge | Q_{GD} | | | 1.5 | | |

SWITCHING CHARACTERISTICS (Note 6)

| | | | | | | |
|---------------------|--------------|--|--|------|--|-------------|
| Turn-On Delay Time | $t_{d(ON)}$ | $V_{GS} = -4.5\text{ V}, V_{DD} = -5.0\text{ V}, I_D = -2.0\text{ A}, R_G = 2.0\ \Omega$ | | 6.6 | | ns |
| Rise Time | t_r | | | 9.0 | | |
| Turn-Off Delay Time | $t_{d(OFF)}$ | | | 14 | | |
| Fall Time | t_f | | | 12.5 | | |

DRAIN-SOURCE DIODE CHARACTERISTICS

| | | | | | | | |
|--------------------------|----------|--|---------------------------|----|-------|-------------|---|
| Forward Recovery Voltage | V_{SD} | $V_{GS} = 0\text{ V}, I_S = -1.0\text{ A}$ | $T_J = 25^\circ\text{C}$ | | -0.73 | -1.0 | V |
| | | | $T_J = 125^\circ\text{C}$ | | -0.62 | | |
| Reverse Recovery Time | t_{RR} | $V_{GS} = 0\text{ V}, d_{ISD}/d_t = 100\text{ A}/\mu\text{s}, I_S = -1.0\text{ A}$ | | 23 | | ns | |
| Charge Time | t_a | | | 13 | | | |
| Discharge Time | t_b | | | 10 | | | |
| Reverse Recovery Time | Q_{RR} | | | 10 | | nC | |

5. Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2\%$.

6. Switching characteristics are independent of operating junction temperatures.

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TYPICAL PERFORMANCE CURVES ($T_J = 25^\circ\text{C}$ unless otherwise noted)

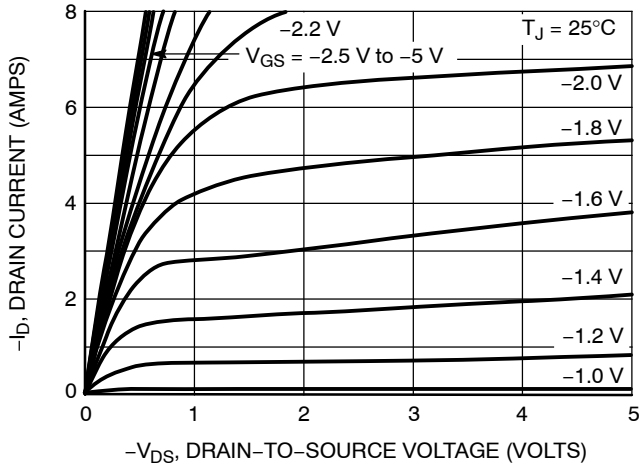


Figure 1. On-Region Characteristics

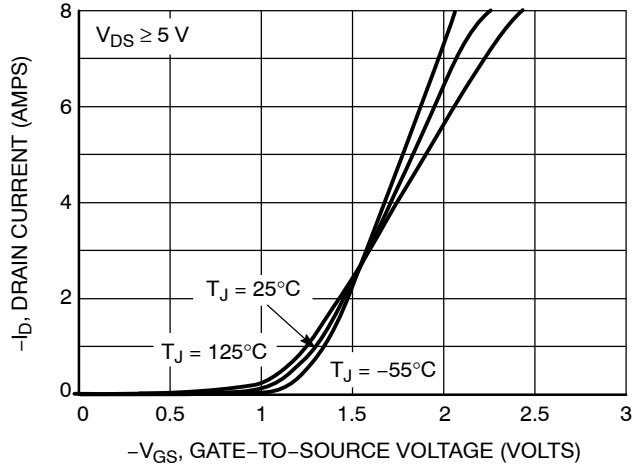


Figure 2. Transfer Characteristics

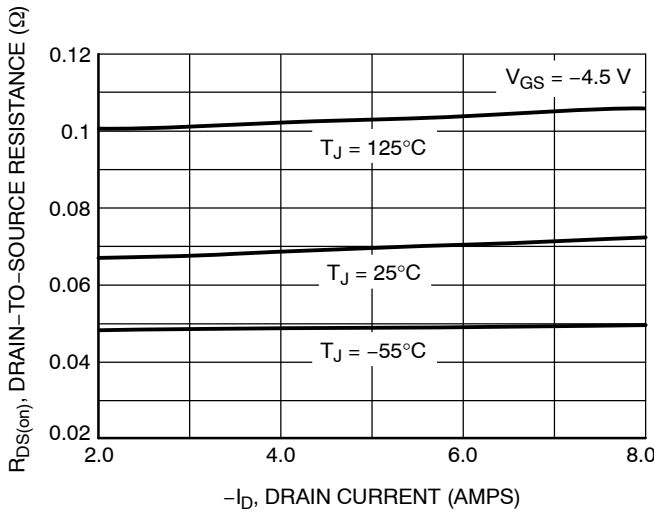


Figure 3. On-Resistance versus Drain Current

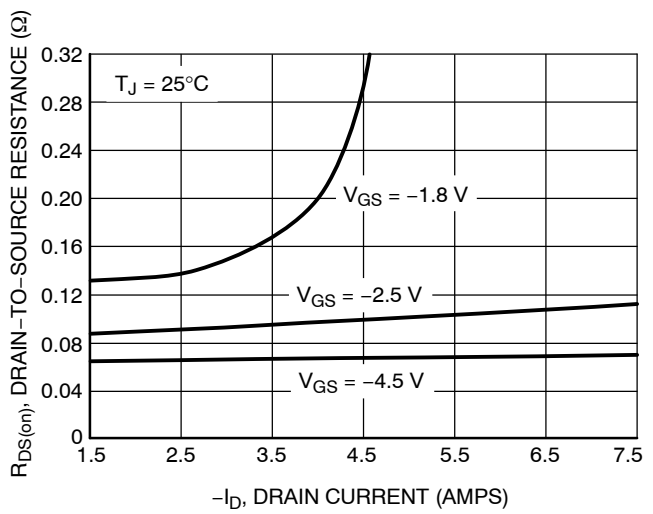


Figure 4. On-Resistance versus Drain Current and Gate Voltage

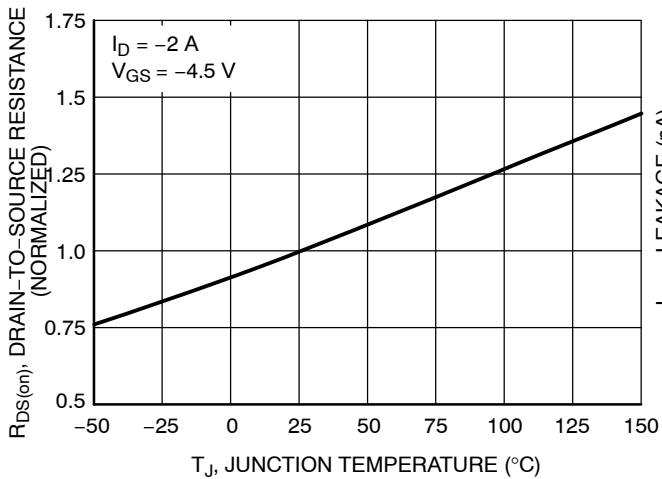


Figure 5. On-Resistance Variation with Temperature

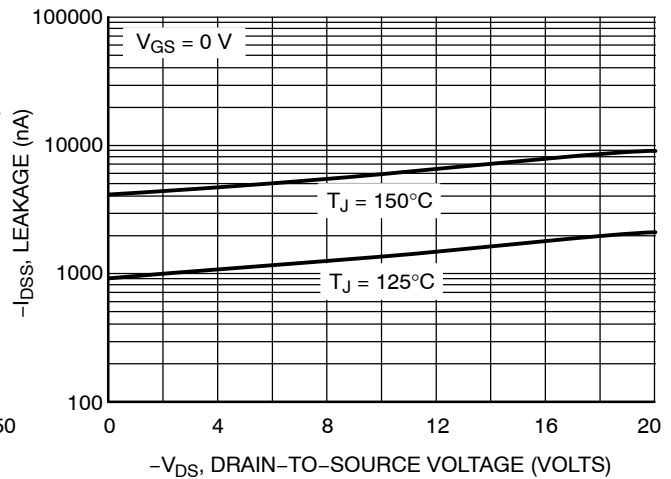


Figure 6. Drain-to-Source Leakage Current versus Voltage

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TYPICAL PERFORMANCE CURVES ($T_J = 25^\circ\text{C}$ unless otherwise noted)

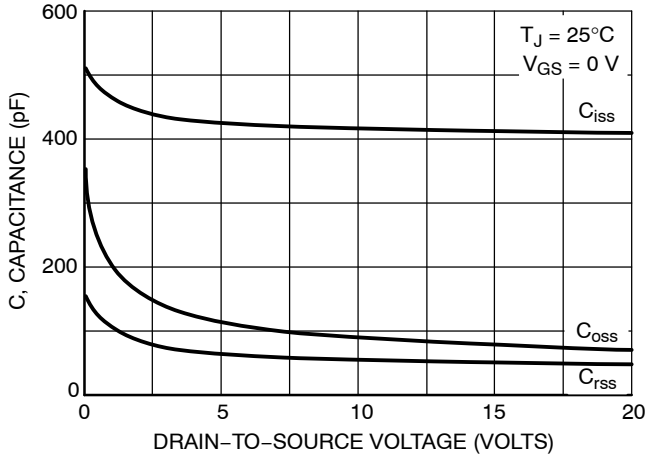


Figure 7. Capacitance Variation

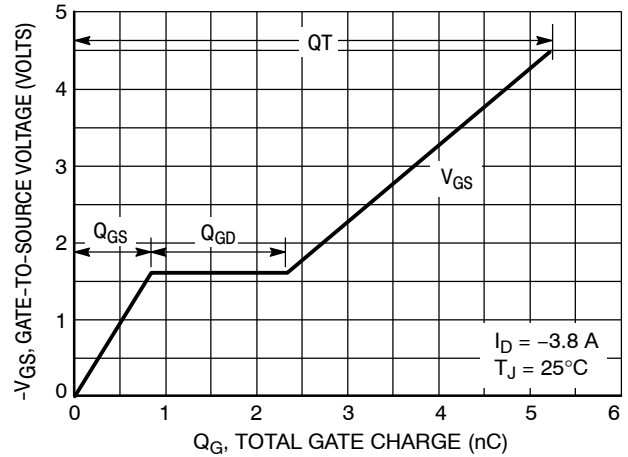


Figure 8. Gate-To-Source and Drain-To-Source Voltage versus Total Charge

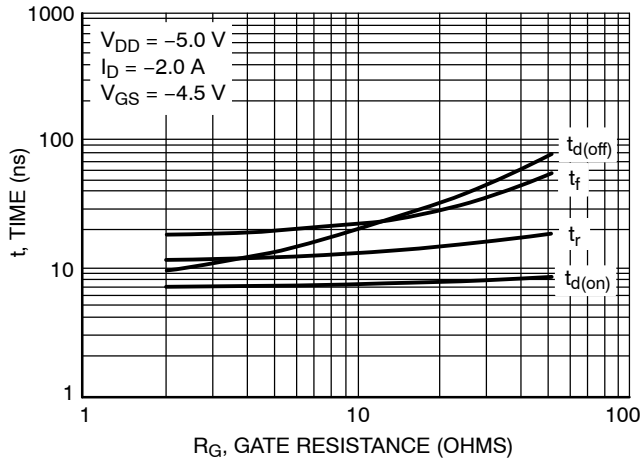


Figure 9. Resistive Switching Time Variation versus Gate Resistance

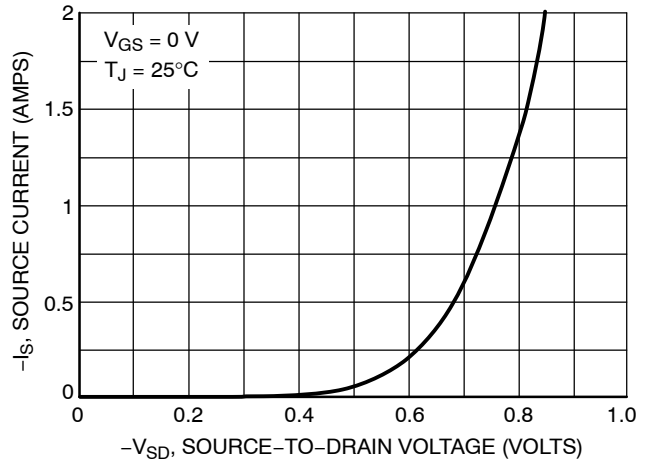


Figure 10. Diode Forward Voltage versus Current

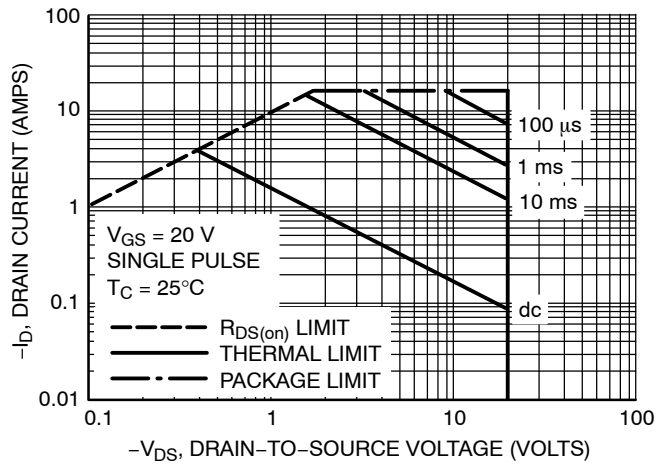


Figure 11. Maximum Rated Forward Biased Safe Operating Area

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TYPICAL PERFORMANCE CURVES ($T_J = 25^\circ\text{C}$ unless otherwise noted)

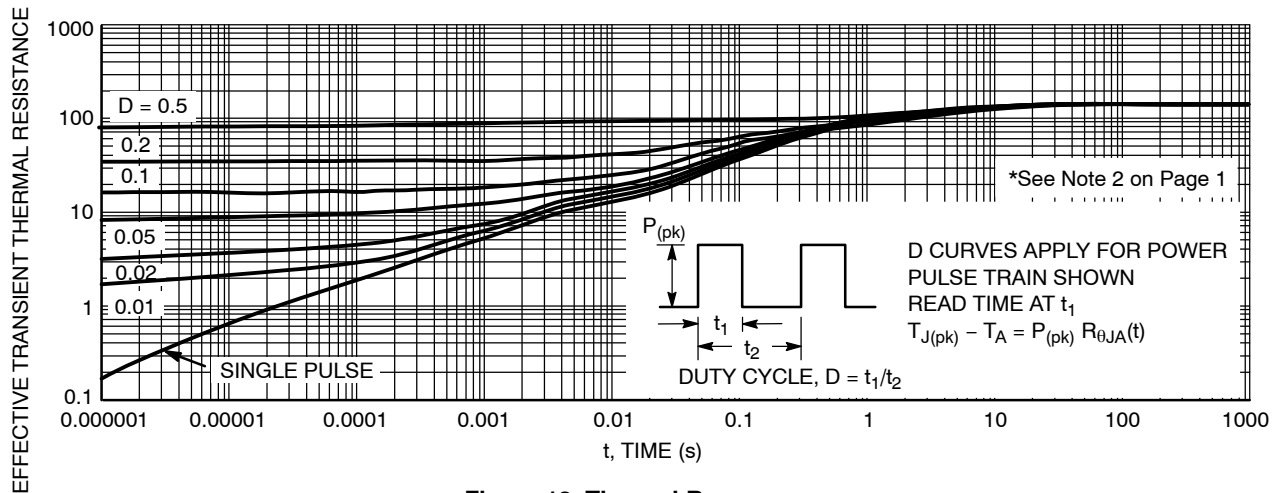
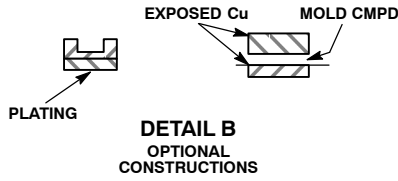
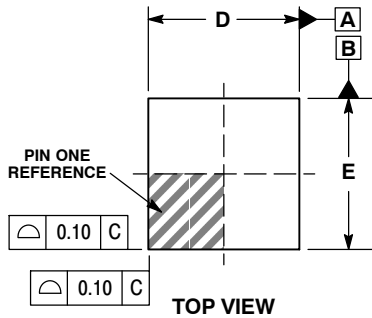


Figure 12. Thermal Response

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PACKAGE DIMENSIONS

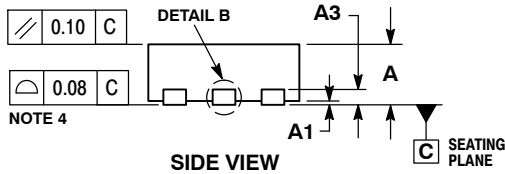
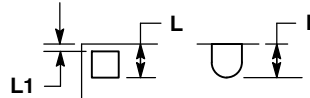
WDFN6, 2x2
CASE 506AN-01
ISSUE D



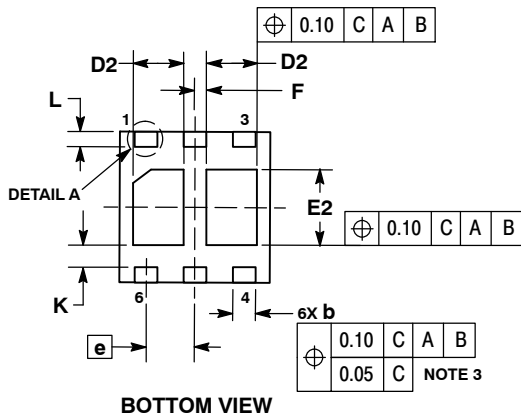
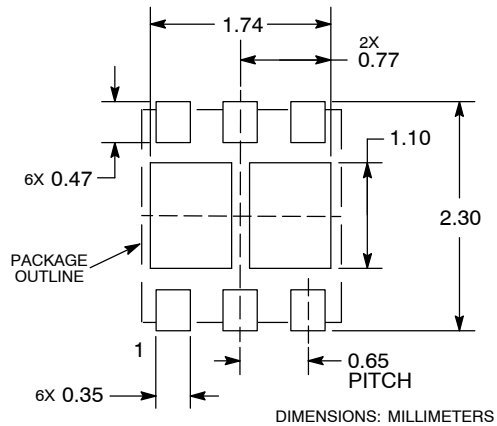
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

| DIM | MILLIMETERS | |
|-----|-------------|------|
| | MIN | MAX |
| A | 0.70 | 0.80 |
| A1 | 0.00 | 0.05 |
| A3 | 0.20 REF | |
| b | 0.25 | 0.35 |
| D | 2.00 BSC | |
| D2 | 0.57 | 0.67 |
| E | 2.00 BSC | |
| E2 | 0.90 | 1.10 |
| e | 0.65 BSC | |
| F | 0.15 BSC | |
| K | 0.25 REF | |
| L | 0.20 | 0.30 |
| L1 | --- | 0.10 |



SOLDERMASK DEFINED MOUNTING FOOTPRINT



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