Freescale Semiconductor
Data Sheet: Advance Information

MCF52235DS
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MCF52235 ColdFire® Microcontroller Data Sheet

Supports MCF52235, MCF52234, MCF52233, MCF52231, & MCF52230

By: Microcontroller Division

The MCF52235 is a member of the ColdFire® family of reduced instruction set computing (RISC) microprocessors. This hardware specification provides an overview of the 32-bit MCF52235 microcontroller, focusing on its highly integrated and diverse feature set.

This 32-bit device is based on the Version 2 ColdFire core operating at a frequency up to 60 MHz, offering high performance and low power consumption. On-chip memories connected tightly to the processor core include 256 Kbytes of Flash and 32 Kbytes of static random access memory (SRAM). On-chip modules include:

- V2 ColdFire core providing 56 Dhrystone 2.1 MIPS @ 60 MHz executing out of on-chip Flash memory using enhanced multiply accumulate (EMAC) and hardware divider.
- Enhanced Multiply Accumulate Unit (EMAC) and hardware divide module
- Cryptographic Acceleration Unit (CAU) coprocessor
- Fast Ethernet Controller (FEC)
- On-chip Ethernet Transceiver (ePHY)

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- FlexCAN controller area network (CAN) module
- Three universal asynchronous/synchronous receiver/transmitters (UARTs)
- Inter-integrated circuit (I^2C™) bus controller
- Queued serial peripheral interface (QSPI) module
- Eight-channel 12-bit fast analog-to-digital converter (ADC)
- Four channel direct memory access (DMA) controller
- Four 32-bit input capture/output compare timers with DMA support (DTIM)
- Four-channel general-purpose timer (GPT) capable of input capture/output compare, pulse width modulation (PWM) and pulse accumulation
- Eight/Four-channel 8/16-bit pulse width modulation timers (two adjacent 8-bit PWMs can be concatenated to form a single 16-bit timer)
- Two 16-bit periodic interrupt timers (PITs)
- Real-time clock (RTC) module
- Programmable software watchdog timer
- Two interrupt controllers providing every peripheral with a unique selectable-priority interrupt vector plus seven external interrupts with fixed levels/priorities
- Clock module with support for crystal or external oscillator and integrated phase locked loop (PLL)
- Test access/debug port (JTAG, BDM)

1 MCF52235 Family Configurations

Table 1. MCF52235 Family Configurations

Module	52230	52231	52233	52234	52235
ColdFire Version 2 Core with MAC (Multiply-Accumulate Unit)	x	x	x	x	x
System Clock	60 MHz				
Performance (Dhrystone 2.1 MIPS)	56				
Flash / Static RAM (SRAM)	128/32 Kbytes		256/32 Kbytes		
Interrupt Controllers (INTC0/INTC1)	x	x	x	x	x
Fast Analog-to-Digital Converter (ADC)	x	x	x	x	x
Random Number Generator and Crypto Acceleration Unit (CAU)	-	-	-	-	x
FlexCAN 2.0B Module	-	x	-	x	x
Fast Ethernet Controller (FEC) with on-chip interface (ePHY)	x	x	x	x	x
Four-channel Direct-Memory Access (DMA)	x	x	x	x	x

Table 1. MCF52235 Family Configurations (continued)

Module	52230	52231	52233	52234	52235
Software Watchdog Timer (WDT)	x	x	x	x	x
Programmable Interrupt Timer	2	2	2	2	2
Four-Channel General Purpose Timer	x	x	x	x	x
32-bit DMA Timers	4	4	4	4	4
QSPI	x	x	x	x	x
UART(s)	3	3	3	3	3
I^2C	x	x	x	x	x
Eight/Four-channel 8/16-bit PWM Timer	x	x	x	x	x
General Purpose I/O Module (GPIO)	x	x	x	x	x
Chip Configuration and Reset Controller Module	x	x	x	x	x
Background Debug Mode (BDM)	x	x	x	x	x
JTAG - IEEE 1149.1 Test Access Port[1]	x	x	x	x	x
Package	80-pin LQFP 112-pin LQFP	80-pin LQFP 112-pin LQFP	80-pin LQFP 112-pin LQFP	80-pin LQFP 112-pin LQFP 121 MAPBGA	112-pin LQFP 121 MAPBGA

NOTES:
1 The full debug/trace interface is available only on the 112- and 121-pin packages. A reduced debug interface is bonded on the 80-pin package.

1.1 Block Diagram

The MCF52235 (or its variants) come in 80- and 112-pin low-profile quad flat pack packages (LQFP) and a 121 MAPBGA, and operates in single-chip mode only. Figure 1 shows a top-level block diagram of the MCF52235.

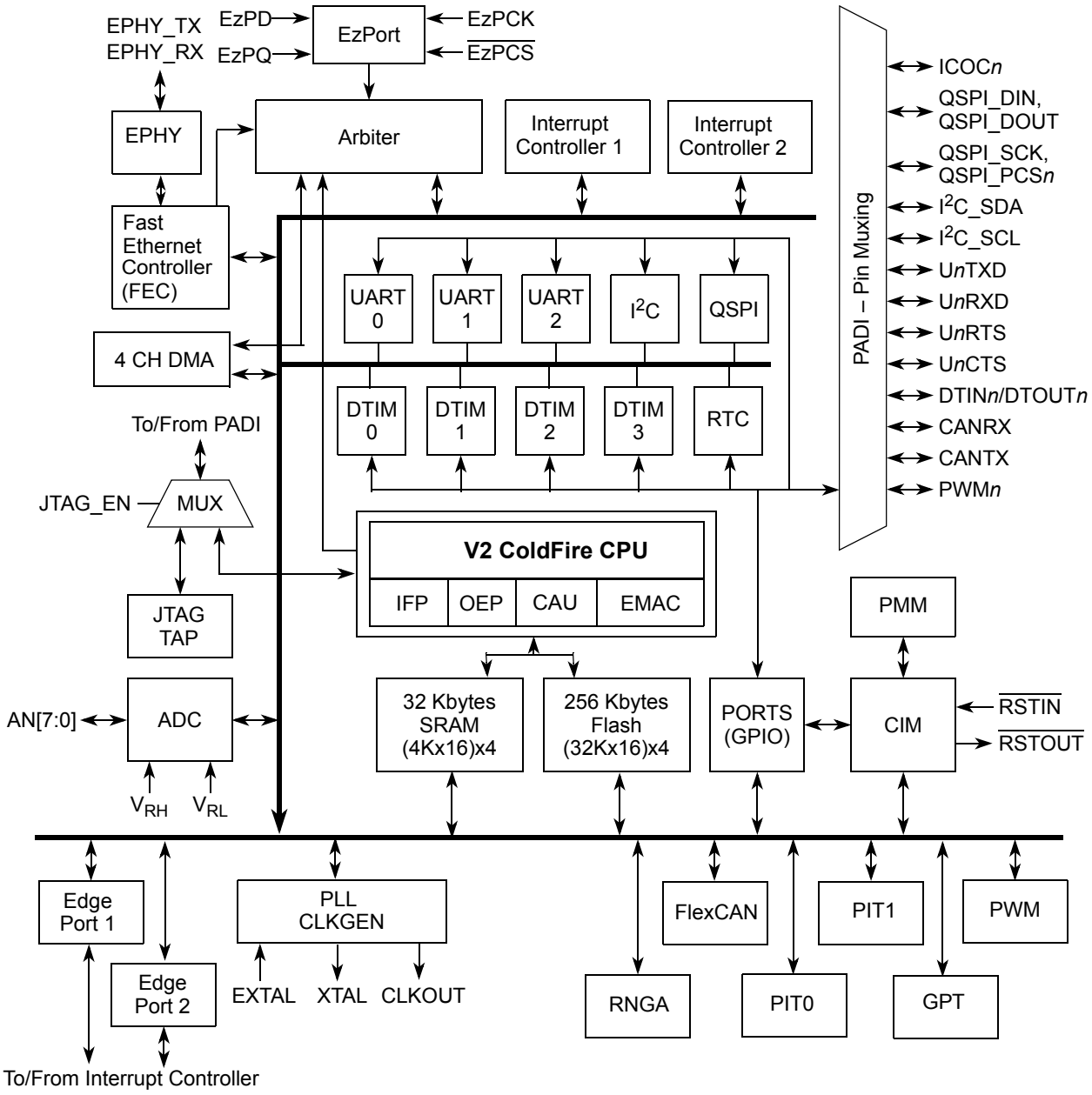

Figure 1. MCF52235 Block Diagram

1.2 Features

This document contains information on a new product under development. Freescale reserves the right to change or discontinue this product without notice. Specifications and information herein are subject to change without notice.

1.2.1 Feature Overview

- Version 2 ColdFire variable-length RISC processor core
  - Static operation
  - 32-bit address and data path on-chip
  - Up to 60MHz processor core frequency
  - Sixteen general-purpose 32-bit data and address registers
  - Implements ColdFire ISA_A+ with extensions to support the user stack pointer register, and 4 new instructions for improved bit processing
  - Enhanced Multiply-Accumulate (EMAC) unit with four 48-bit accumulators to support 32-bit signal processing algorithms
  - Cryptography Acceleration Unit (CAU)
    - Tightly-coupled coprocessor to accelerate software-based encryption and message digest functions
    - FIPS-140 compliant random number generator
    - Support for DES, 3DES, AES, MD5, and SHA-1 algorithms
  - Illegal instruction decode that allows for 68K emulation support
- System debug support
  - Real time trace for determining dynamic execution path
  - Background debug mode (BDM) for in-circuit debugging
  - Real time debug support, with four user-visible hardware breakpoint registers (PC and address with optional data) that can be configured into a 1- or 2-level trigger
- On-chip memories
  - 32 Kbyte dual-ported SRAM on CPU internal bus, accessible by core and non-core bus masters (e.g., DMA) with standby power supply support
  - 256 Kbytes of interleaved Flash memory supporting 2-1-1-1 accesses
- Power management
  - Fully static operation with processor sleep and whole chip stop modes
  - Very rapid response to interrupts from the low-power sleep mode (wake-up feature)
  - Software visible clock enable/disable for each peripheral
- Fast Ethernet Controller (FEC)
  - 10/100 BaseT/TX capability, half duplex or full duplex
  - On-chip transmit and receive FIFOs
  - Built-in dedicated DMA controller
  - Memory-based flexible descriptor rings

- On-chip Ethernet Transceiver (ePHY)
  - Digital adaptive equalization
  - Supports auto-negotiation
  - Baseline wander correction
  - Full-/Half-duplex support in all modes
  - Loopback modes
  - Supports MDIO preamble suppression
  - Jumbo packet
- FlexCAN 2.0B Module
  - Based on and includes all existing features of the Freescale TOUCAN module
  - Full implementation of the CAN protocol specification version 2.0B
    - Standard Data and Remote Frames (up to 109 bits long)
    - Extended Data and Remote Frames (up to 127 bits long)
    - 0-8 bytes data length
    - Programmable bit rate up to 1 Mbit/sec
  - Flexible Message Buffers (MBs), totalling up to 16 message buffers of 0–8 byte data length each, configurable as Rx or Tx, all supporting standard and extended messages
  - Unused Message Buffer space can be used as general purpose RAM space
  - Listen only mode capability
  - Content-related addressing
  - No read/write semaphores required
  - Three programmable mask registers: global (for MBs 0-13), special for MB14 and special for MB15
  - Programmable transmit-first scheme: lowest ID or lowest buffer number
  - “Time stamp” based on 16-bit free-running timer
  - Global network time, synchronized by a specific message
  - Programmable I/O modes
  - Maskable interrupts
- Three Universal Asynchronous/synchronous Receiver Transmitters (UARTs)
  - 16-bit divider for clock generation
  - Interrupt control logic
  - Maskable interrupts
  - DMA support
  - Data formats can be 5, 6, 7 or 8 bits with even, odd or no parity
  - Up to 2 stop bits in 1/16 increments
  - Error-detection capabilities

  - Modem support includes request-to-send ($\overline{\text{URTS}}$) and clear-to-send ($\overline{\text{UCTS}}$) lines for two UARTs
  - Transmit and receive FIFO buffers
- I^2C Module
  - Interchip bus interface for EEPROMs, LCD controllers, A/D converters, and keypads
  - Fully compatible with industry-standard I^2C bus
  - Master or slave modes support multiple masters
  - Automatic interrupt generation with programmable level
- Queued Serial Peripheral Interface (QSPI)
  - Full-duplex, three-wire synchronous transfers
  - Up to four chip selects available
  - Master mode operation only
  - Programmable master bit rates
  - Up to 16 pre-programmed transfers
- Fast Analog-to-Digital Converter (ADC)
  - 8 analog input channels
  - 12-bit resolution
  - Minimum 2.25 μS conversion time
  - Simultaneous sampling of two channels for motor control applications
  - Single-scan or continuous operation
  - Optional interrupts on conversion complete, zero crossing (sign change), or under/over low/high limit
  - Unused analog channels can be used as digital I/O
- Four 32-bit DMA Timers
  - 16.7-ns resolution at 60 MHz
  - Programmable sources for clock input, including an external clock option
  - Programmable prescaler
  - Input-capture capability with programmable trigger edge on input pin
  - Output-compare with programmable mode for the output pin
  - Free run and restart modes
  - Maskable interrupts on input capture or reference-compare
  - DMA trigger capability on input capture or reference-compare
- Four-channel general purpose timers
  - 16-bit architecture
  - Programmable prescaler
  - Output pulse widths variable from microseconds to seconds

  - Single 16-bit input pulse accumulator
  - Toggle-on-overflow feature for pulse-width modulator (PWM) generation
  - One dual-mode pulse accumulation channel
- Pulse-width modulation timer
  - Operates as eight channels with 8-bit resolution or four channels with 16-bit resolution
  - Programmable period and duty cycle
  - Programmable enable/disable for each channel
  - Software selectable polarity for each channel
  - Period and duty cycle are double buffered. Change takes effect when the end of the current period is reached (PWM counter reaches zero) or when the channel is disabled.
  - Programmable center or left aligned outputs on individual channels
  - Four clock sources (A, B, SA, and SB) provide for a wide range of frequencies
  - Emergency shutdown
- Two Periodic Interrupt Timers (PITs)
  - 16-bit counter
  - Selectable as free running or count down
- Real-Time Clock (RTC)
  - Maintains system time-of-day clock
  - Provides stopwatch and alarm interrupt functions
- Software Watchdog Timer
  - 32-bit counter
  - Low power mode support
- Clock Generation Features
  - 25 MHz crystal input
  - On-chip PLL can generate core frequencies up to maximum 60MHz operating frequency
  - Provides clock for integrated ePHY
- Dual Interrupt Controllers (INTC0/INTC1)
  - Support for multiple interrupt sources organized as follows:
    - Fully-programmable interrupt sources for each peripheral
    - 7 fixed-level interrupt sources
    - Seven external interrupt signals
  - Unique vector number for each interrupt source
  - Ability to mask any individual interrupt source or all interrupt sources (global mask-all)
  - Support for hardware and software interrupt acknowledge (IACK) cycles
  - Combinatorial path to provide wake-up from low power modes

- DMA Controller
  - Four fully programmable channels
  - Dual-address transfer support with 8-, 16- and 32-bit data capability along with support for 16-byte (4 X 32-bit) burst transfers
  - Source/destination address pointers that can increment or remain constant
  - 24-bit byte transfer counter per channel
  - Auto-alignment transfers supported for efficient block movement
  - Bursting and cycle steal support
  - support for channel-to-channel linking
  - Software-programmable DMA channel selections in the UARTs (3) and 32-bit timers (4)
- Reset
  - Separate reset in and reset out signals
  - Seven sources of reset:
    - Power-on reset (POR)
    - External
    - Software
    - Watchdog
    - Loss of clock
    - Loss of lock
    - Low-voltage detection (LVD)
  - Status flag indication of source of last reset
- Chip Integration Module (CIM)
  - System configuration during reset
  - Selects one of six clock modes
  - Configures output pad drive strength
  - Unique part identification number and part revision number
- General Purpose I/O interface
  - Up to 73 bits of general purpose I/O
  - Bit manipulation supported via set/clear functions
  - Unused peripheral pins may be used as extra GPIO
- JTAG support for system level board testing

1.2.2 V2 Core Overview

The Version 2 ColdFire processor core is comprised of two separate pipelines that are decoupled by an instruction buffer. The two-stage Instruction Fetch Pipeline (IFP) is responsible for instruction-address generation and instruction fetch. The instruction buffer is a first-in-first-out (FIFO) buffer that holds

prefetched instructions awaiting execution in the Operand Execution Pipeline (OEP). The OEP includes two pipeline stages. The first stage decodes instructions and selects operands (DSOC); the second stage (AGEX) performs instruction execution and calculates operand effective addresses, if needed.

The V2 core implements the ColdFire Instruction Set Architecture Revision A+ (see the ColdFire Family Programmer's Reference Manual for instruction set details) which includes support for a separate user stack pointer register and four new instructions to assist in bit processing. Additionally, the MCF52235 core includes the enhanced multiply-accumulate unit (EMAC) for improved signal processing capabilities. The MAC implements a 4-stage arithmetic pipeline, optimized for 32 x 32 bit operations, with support for four 48-bit accumulators. Supported operands include 16- and 32-bit signed and unsigned integers as well as signed fractional operands and a complete set of instructions to process these data types. The EMAC provides superb support for execution of DSP operations within the context of a single processor at a minimal hardware cost.

1.2.3 Debug Module

The ColdFire processor core debug interface is provided to support system debugging in conjunction with low-cost debug and emulator development tools. Through a standard debug interface users can access debug information, and on 112- and 121-lead packages real-time tracing capability is provided. This allows the processor and system to be debugged at full speed without the need for costly in-circuit emulators. The debug interface is a superset of the BDM interface provided on Freescale's 683xx family of parts. The MCF52235 supports Revision B+ of the ColdFire debug architecture (DEBUG_B+).

The on-chip breakpoint resources include a total of nine programmable 32-bit registers: two address registers, two data registers (one data register and one data mask register), four 32-bit PC registers and one PC mask register. These registers can be accessed through the dedicated debug serial communication channel or from the processor's supervisor mode programming model. The breakpoint registers can be configured to generate triggers by combining the address, data, and PC conditions in a variety of single- or dual-level definitions. The trigger event can be programmed to generate a processor halt or initiate a debug interrupt exception.

The MCF52235's interrupt servicing options during emulator mode allow real-time critical interrupt service routines to be serviced while processing a debug interrupt event, thereby ensuring that the system continues to operate even during debugging.

To support program trace, the V2 debug module provides processor status (PST[3:0]) and debug data (DDATA[3:0]) ports. These buses and the PSTCLK output provide execution status, captured operand data, and branch target addresses defining processor activity at the CPU's clock rate. The MCF52235 includes a new debug signal, ALLPST. This signal is the logical 'AND' of the processor status (PST[3:0]) signals and is useful for detecting when the processor is in a halted state (PST[3:0] = 1111).

The full debug/trace interface is available only on the 112- and 121-pin packages. However, every product features the dedicated debug serial communication channel (DSI, DSO, DSCLK) and the ALLPST signal.

1.2.4 JTAG

The MCF52235 supports circuit board test strategies based on the Test Technology Committee of IEEE and the Joint Test Action Group (JTAG). The test logic includes a test access port (TAP) consisting of a

16-state controller, an instruction register, and three test registers (a 1-bit bypass register, a 256-bit boundary-scan register, and a 32-bit ID register). The boundary scan register links the device's pins into one shift register. Test logic, implemented using static logic design, is independent of the device system logic.

The MCF52235 implementation can do the following:

- Perform boundary-scan operations to test circuit board electrical continuity
- Sample MCF52235 system pins during operation and transparently shift out the result in the boundary scan register
- Bypass the MCF52235 for a given circuit board test by effectively reducing the boundary-scan register to a single bit
- Disable the output drive to pins during circuit-board testing
- Drive output pins to stable levels

1.2.5 On-Chip Memories

1.2.5.1 SRAM

The SRAM module provides a general-purpose 32-Kbyte memory block that the ColdFire core can access in a single cycle. The location of the memory block can be set to any 32-Kbyte boundary within the 4-Gbyte address space. This memory is ideal for storing critical code or data structures and for use as the system stack. Because the SRAM module is physically connected to the processor's high-speed local bus, it can quickly service core-initiated accesses or memory-referencing commands from the debug module.

The SRAM module is also accessible by the DMA. The dual-ported nature of the SRAM makes it ideal for implementing applications with double-buffer schemes, where the processor and a DMA device operate in alternate regions of the SRAM to maximize system performance.

1.2.5.2 Flash

The ColdFire Flash Module (CFM) is a non-volatile memory (NVM) module that connects to the processor's high-speed local bus. The CFM is constructed with four banks of 32K x 16-bit Flash arrays to generate 256 Kbytes of 32-bit Flash memory. These arrays serve as electrically erasable and programmable, non-volatile program and data memory. The Flash memory is ideal for program and data storage for single-chip applications, allowing for field reprogramming without requiring an external high voltage source. The CFM interfaces to the ColdFire core through an optimized read-only memory controller which supports address speculation and interleaved accesses from the 2-cycle Flash arrays for improved performance. For operation at reduced core frequencies, the access time can be decreased (under program control) to a single-cycle access. A backdoor mapping of the Flash memory is used for all program, erase, and verify operations, as well as providing a read datapath for the DMA. Flash memory may also be programmed via the EzPort, which is a serial Flash programming interface that allows the Flash to be read, erased and programmed by an external controller in a format compatible with most SPI bus Flash memory chips. This allows easy device programming via Automated Test Equipment or bulk programming tools.

1.2.6 Power Management

The MCF52235 incorporates several low power modes of operation which are entered under program control and exited by several external trigger events. An integrated power-on reset (POR) circuit monitors the input supply and forces an MCU reset as the supply voltage rises. The low voltage detector (LVD) monitors the supply voltage and is configurable to force a reset or interrupt condition if it falls below the LVD trip point.

1.2.7 Fast Ethernet Controller (FEC)

The integrated Fast Ethernet Controller (FEC) performs the full set of IEEE® 802.3/Ethernet CSMA/CD media access control and channel interface functions. The FEC connects through the on-chip transceiver (ePHY) which provides the physical layer interface.

1.2.8 Ethernet Physical Interface (ePHY)

The ePHY is an IEEE 802.3 compliant 10/100 Ethernet physical transceiver. The ePHY can be configured to support 10BASE-T or 100BASE-TX applications. The ePHY is configurable via internal registers.

There are five basic modes of operation for the ePHY:

- Power down/initialization
- Auto-negotiate
- 10BASE-T
- 100BASE-TX
- Low-power

1.2.9 Cryptography Acceleration Unit

The MCF52235 device incorporates two hardware accelerators for cryptographic functions. First, the CAU is a coprocessor tightly-coupled to the V2 ColdFire core that implements a set of specialized operations to increase the throughput of software-based encryption and message digest functions, specifically the DES, 3DES, AES, MD5 and SHA-1 algorithms. Second, a random number generator provides FIPS-140 compliant 32-bit values to security processing routines. Both modules supply critical acceleration to software-based cryptographic algorithms at a minimal hardware cost.

1.2.10 FlexCAN

The FlexCAN module is a communication controller implementing version 2.0 of the CAN protocol parts A and B. The CAN protocol can be used as an industrial control serial data bus, meeting the specific requirements of reliable operation in a harsh EMI environment with high bandwidth. This instantiation of FlexCAN has 16 message buffers.

1.2.11 UARTs

The MCF52235 has three full-duplex UARTs that function independently. The three UARTs can be clocked by the system bus clock, eliminating the need for an external clock source. On smaller packages, the third UART is multiplexed with other digital I/O functions.

1.2.12 I^2C Bus

The I^2C bus is a two-wire, bidirectional serial bus that provides a simple, efficient method of data exchange and minimizes the interconnection between devices. This bus is suitable for applications requiring occasional communications over a short distance between many devices on a circuit board.

1.2.13 QSPI

The queued serial peripheral interface (QSPI) provides a synchronous serial peripheral interface with queued transfer capability. It allows up to 16 transfers to be queued at once, minimizing the need for CPU intervention between transfers.

1.2.14 ADC

The Fast ADC consists of an eight-channel input select multiplexer and two independent sample and hold (S/H) circuits feeding separate 12-bit ADCs. The two separate converters store their results in accessible buffers for further processing.

The ADC can be configured to perform a single scan and halt, perform a scan whenever triggered, or perform a programmed scan sequence repeatedly until manually stopped.

The ADC can be configured for either *sequential* or *simultaneous* conversion. When configured for sequential conversions, up to eight channels can be sampled and stored in any order specified by the channel list register. Both ADCs may be required during a scan, depending on the inputs to be sampled.

During a simultaneous conversion, both S/H circuits are used to capture two different channels at the same time. This configuration requires that a single channel may not be sampled by both S/H circuits simultaneously.

Optional interrupts can be generated at the end of the scan sequence if a channel is out of range (measures below the low threshold limit or above the high threshold limit set in the limit registers) or at several different zero crossing conditions.

1.2.15 DMA Timers (DTIM0–DTIM3)

There are four independent, DMA transfer capable 32-bit timers (DTIM0, DTIM1, DTIM2, and DTIM3) on the MCF52235. Each module incorporates a 32-bit timer with a separate register set for configuration and control. The timers can be configured to operate from the system clock or from an external clock source using one of the DTINx signals. If the system clock is selected, it can be divided by 16 or 1. The input clock is further divided by a user-programmable 8-bit prescaler which clocks the actual timer counter register (TCRn). Each of these timers can be configured for input capture or reference (output) compare mode. Timer events may optionally cause interrupt requests or DMA transfers.

1.2.16 General Purpose Timer (GPT)

The general purpose timer (GPT) is a four-channel timer module consisting of a 16-bit programmable counter driven by a 7-stage programmable prescaler. Each of the four channels can be configured for input capture or output compare. Additionally, one of the channels, channel 3, can be configured as a pulse accumulator.

A timer overflow function allows software to extend the timing capability of the system beyond the 16-bit range of the counter. The input capture and output compare functions allow simultaneous input waveform measurements and output waveform generation. The input capture function can capture the time of a selected transition edge. The output compare function can generate output waveforms and timer software delays. The 16-bit pulse accumulator can operate as a simple event counter or a gated time accumulator.

1.2.17 Periodic Interrupt Timers (PIT0 and PIT1)

The two periodic interrupt timers (PIT0 and PIT1) are 16-bit timers that provide interrupts at regular intervals with minimal processor intervention. Each timer can either count down from the value written in its PIT modulus register, or it can be a free-running down-counter.

1.2.18 Pulse Width Modulation Timers

The MCF52235 has an 8-channel, 8-bit PWM timer. Each channel has a programmable period and duty cycle as well as a dedicated counter. Each of the modulators can create independent continuous waveforms with software-selectable duty rates from 0% to 100%. The PWM outputs have programmable polarity, and can be programmed as left aligned outputs or center aligned outputs. For higher period and duty cycle resolution, each pair of adjacent channels ([7:6], [5:4], [3:2], and [1:0]) can be concatenated to form a single 16-bit channel. The module can thus be configured to support 8/0, 6/1, 4/2, 2/3, or 0/4 8-/16-bit channels.

1.2.19 Real-Time Clock (RTC)

The Real-Time Clock (RTC) module maintains the system (time-of-day) clock and provides stopwatch, alarm, and interrupt functions. It includes full clock features: seconds, minutes, hours, days and supports a host of time-of-day interrupt functions along with an alarm interrupt.

1.2.20 Software Watchdog Timer

The watchdog timer is a 16-bit timer that facilitates recovery from runaway code. The watchdog counter is a free-running down-counter that generates a reset on underflow. To prevent a reset, software must periodically restart the countdown.

1.2.21 Phase Locked Loop (PLL)

The clock module supports an external crystal oscillator and includes a phase-locked loop (PLL), reduced frequency divider (RFD), low-power divider status/control registers, and control logic. In order to improve

noise immunity the PLL has its' own power supply inputs: VDDPLL and VSSPLL. All other circuits are powered by the normal supply pins, VDD and VSS.

1.2.22 Interrupt Controller (INTC0/INTC1)

There are two interrupt controllers on the MCF52235. These interrupt controllers are organized as seven levels with up to nine interrupt sources per level. Each interrupt source has a unique interrupt vector, and provide each peripheral with all necessary interrupts. Each internal interrupt has a programmable level [1-7] and priority within the level. The seven external interrupts have fixed levels/priorities.

1.2.23 DMA Controller

The Direct Memory Access (DMA) Controller Module provides an efficient way to move blocks of data with minimal processor interaction. The DMA module provides four channels (DMA0-DMA3) that allow byte, word, longword or 16-byte burst line transfers. These transfers are triggered by software explicitly setting a DCRn[START] bit or by the assertion of a DMA request from any number of on-chip peripherals. The DMA controller supports dual address transfers to on-chip devices.

1.2.24 Reset

The reset controller determines the source of reset, asserts the appropriate reset signals to the system, and keeps track of what caused the last reset. There are six sources of reset:

- External reset input
- Power-on reset (POR)
- Watchdog timer
- Phase locked-loop (PLL) loss of lock
- PLL loss of clock
- Software

Registers provide status flags indicating the last source of reset and a control bit for software assertion of the $\overline{\text{RSTO}}$ pin.

1.2.25 GPIO

All of the pins associated with the external bus interface may be used for several different functions. When not used this, all of the pins may be used as general-purpose digital I/O pins. In some cases, the pin function is set by the operating mode, and the alternate pin functions are not supported.

The digital I/O pins on the MCF52235 are grouped into 8-bit ports. Some ports do not use all eight bits. Each port has registers that configure, monitor, and control the port pins.

1.3 Part Numbers and Packaging

Table 2. Part Number Summary

Part Number	Flash / SRAM	Key Features	Package	Speed
MCF52230	128 Kbytes / 32 Kbytes	3 UARTs, I^2C, QSPI, A/D, FEC ePHY, DMA, 16-/32-bit PWM Timers	80-pin TQFP 112-pin LQFP	60 MHz
MCF52231	128 Kbytes / 32 Kbytes	3 UARTs, I^2C, QSPI, A/D, FEC ePHY, DMA, 16-/32-bit PWM Timers, CAN	80-pin TQFP 112-pin LQFP	60 MHz
MCF52233	256 Kbytes / 32 Kbytes	3 UARTs, I^2C, QSPI, A/D, FEC ePHY, DMA, 16-/32-bit PWM Timers	80-pin TQFP 112-pin LQFP	60 MHz
MDCF52234	256 Kbytes / 32 Kbytes	3 UARTs, I^2C, QSPI, A/D, FEC, ePHY, DMA, 16-/32-bit PWM Timers, CAN	80-pin TQFP 112-pin LQFP 121 MAPBGA	60 MHz
MCF52235	256 Kbytes / 32 Kbytes	3 UARTs, I^2C, QSPI, A/D, CAU, FEC, DMA, ePHY, 16-/32-bit PWM Timers, CAN	112-pin LQFP 121 MAPBGA	60 MHz

1.4 Package Pinouts

Figure 2 shows the pinout configuration for the 80-Lead TQFP.

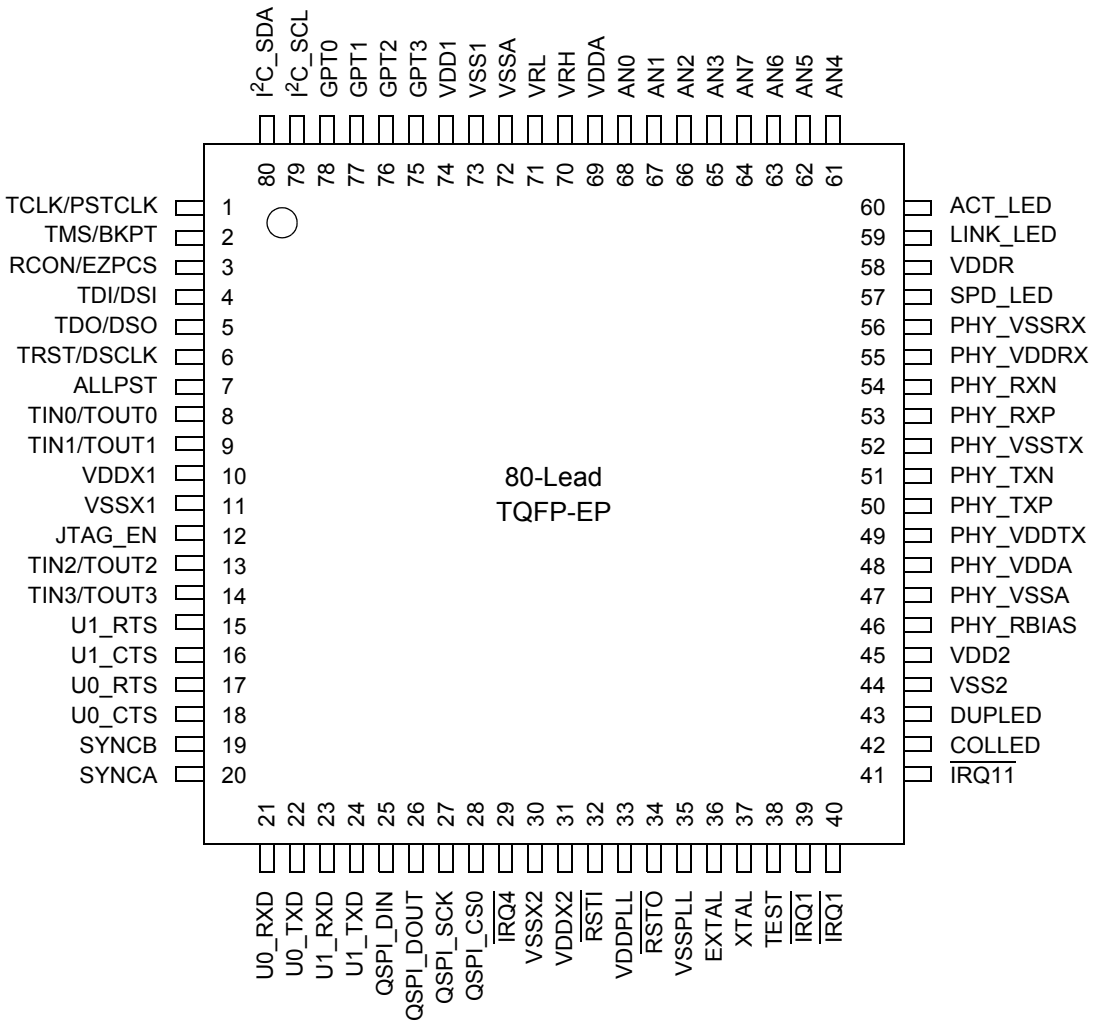

Figure 2. 80-Lead TQFP Pin Assignments

Figure 3 shows the pinout configuration for the 112-Lead LQFP.

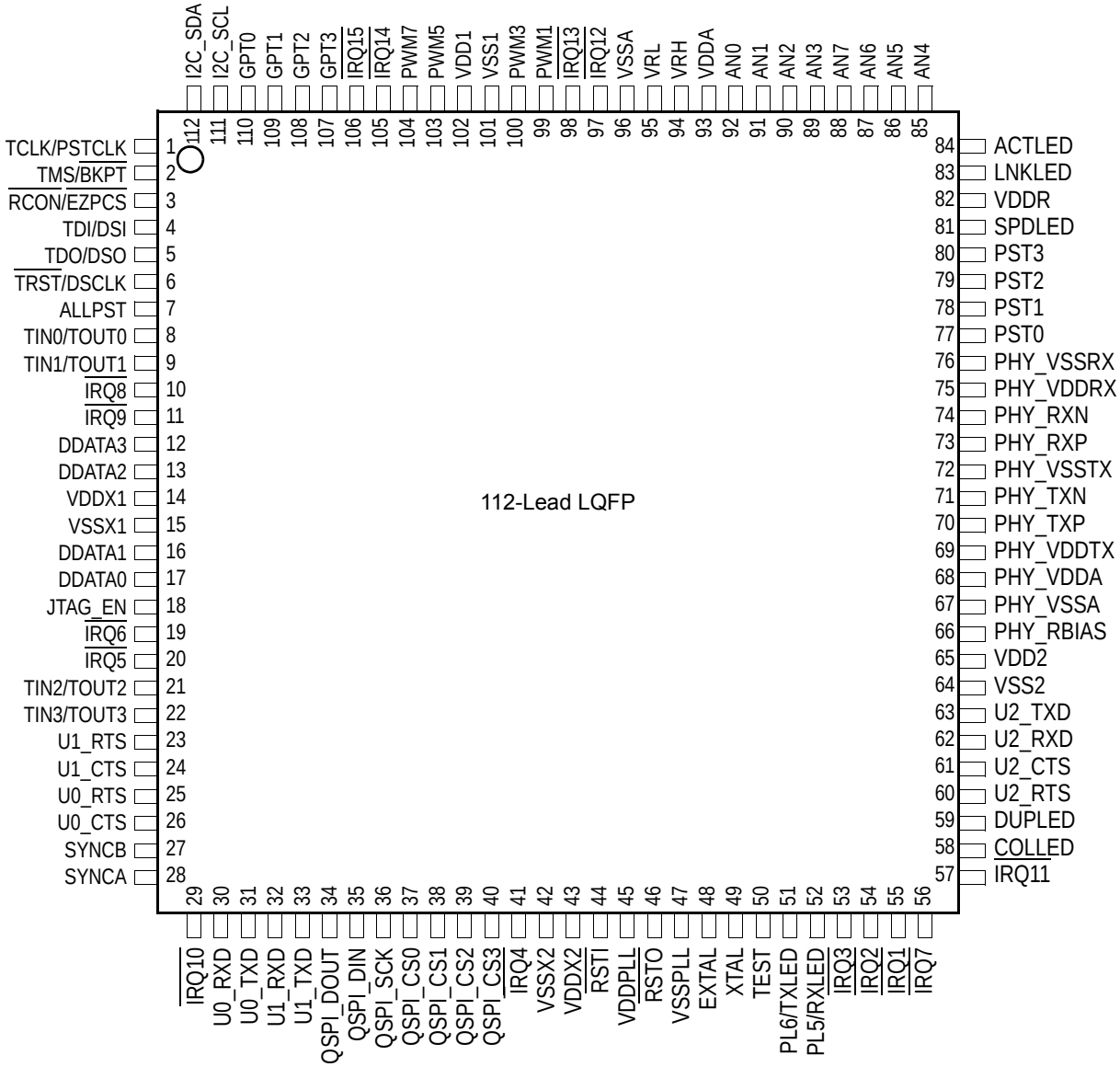

Figure 3. 112-Lead LQFP Pin Assignments

Table 3. Pin Functions by Primary and Alternate Purpose

Pin Group	Primary Function	Secondary Function	Tertiary Function	Quaternary Function	Drive Strength / Control[1]	Wired OR Control	Pull-up / Pull-down[2]	Pin on121 MAPBGA	Pin on 112 LQFP	Pin on 80 LQFP	Notes
ADC	AN7	—	—	PAN[0]	Low	—	—	—	88	64	
	AN6	—	—	PAN[1]	Low	—	—	—	87	63	
	AN5	—	—	PAN[2]	Low	—	—	—	86	62	
	AN4	—	—	PAN[3]	Low	—	—	—	85	61	
	AN3	—	—	PAN[4]	Low	—	—	—	89	65	
	AN2	—	—	PAN[5]	Low	—	—	—	90	66	
	AN1	—	—	PAN[6]	Low	—	—	—	91	67	
	AN0	—	—	PAN[7]	Low	—	—	—	92	68	
	SYNCA	CANTX[3]	FEC_MDIO	PAS[3]	PDSR[39]	—	—	—	28	20	
	SYNCB	CANRX[3]	FEC_MDC	PAS[2]	PDSR[39]	—	—	—	27	19	
	VDDA	—	—	—	N/A	N/A	—	—	93	69	
	VSSA	—	—	—	N/A	N/A	—	—	96	72	
	VRH	—	—	—	N/A	N/A	—	—	94	70	
	VRL	—	—	—	N/A	N/A	—	—	95	71	
Clock Generation	EXTAL	—	—	—	N/A	N/A	—	—	48	36	
	XTAL	—	—	—	N/A	N/A	—	—	49	37	
	VDDPLL	—	—	—	N/A	N/A	—	—	45	33	
	VSSPLL	—	—	—	N/A	N/A	—	—	47	35	
Debug Data	ALLPST	—	—	—	High	—	—	—	7	7	
	DDATA[3:0]	—	—	PDD[7:4]	High	—	—	—	12,13, 16,17	—	
	PST[3:0]	—	—	PDD[3:0]	High	—	—	—	80,79, 78,77	—	

Pin Group	Primary Function	Secondary Function	Tertiary Function	Quaternary Function	Drive Strength / Control[1]	Wired OR Control	Pull-up / Pull-down[2]	Pin on121 MAPBGA	Pin on 112 LQFP	Pin on 80 LQFP	Notes
Ethernet LEDs	ACTLED	—	—	PSD[0]	PDSR[32]	PWOR[8]	—	—	84	60	
	COLLED	—	—	PSD[4]	PDSR[36]	PWOR[12]	—	—	58	42	
	DUPLED	—	—	PSD[3]	PDSR[35]	PWOR[11]	—	—	59	43	
	LNKLED	—	—	PSD[1]	PDSR[33]	PWOR[9]	—	—	83	59	
	SPDLED	—	—	PSD[2]	PDSR[34]	PWOR[10]	—	—	81	57	
	RXLED	—	—	PSD[5]	PDSR[37]	PWOR[13]	—	—	52	—	
	TXLED	—	—	PSD[6]	PDSR[38]	PWOR[14]	—	—	51	—	
Ethernet PHY	PHY_RBIAS	—	—	—	—	—		—	66	46	
	PHY_RXN	—	—	—	—	—		—	74	54	
	PHY_RXP	—	—	—	—	—		—	73	53	
	PHY_TXN	—	—	—	—	—		—	71	51	
	PHY_TXP	—	—	—	—	—		—	70	50	
	PHY_VDDA	—	—	—		N/A		—	68	48	
	PHY_VDDRX	—	—	—		N/A		—	75	55	
	PHY_VDDTX	—	—	—		N/A		—	69	49	
	PHY_VSSA	—	—	—		N/A		—	67	47	
	PHY_VSSRX	—	—	—		N/A		—	76	56	
	PHY_VSSTX	—	—	—		N/A		—	72	52	
I^2C	SCL	CANTX[3]	TXD2	PAS[1]	PDSR[0]	—	pull-up[4]	—	111	79	
	SDA	CANRX[3]	RXD2	PAS[0]	PDSR[0]	—	pull-up[4]	—	112	80	

Pin Group	Primary Function	Secondary Function	Tertiary Function	Quaternary Function	Drive Strength / Control[1]	Wired OR Control	Pull-up / Pull-down[2]	Pin on121 MAPBGA	Pin on 112 LQFP	Pin on 80 LQFP	Notes
Interrupts	$\overline{\text{IRQ15}}$	—	—	PGP[7]	PSDR[47]	—	pull-up[4]	—	106	—	
	$\overline{\text{IRQ14}}$	—	—	PGP[6]	PSDR[46]	—	pull-up[4]	—	105	—	
	$\overline{\text{IRQ13}}$	—	—	PGP[5]	PSDR[45]	—	pull-up[4]	—	98	—	
	$\overline{\text{IRQ12}}$	—	—	PGP[4]	PSDR[44]	—	pull-up[4]	—	97	—	
	$\overline{\text{IRQ11}}$	—	—	PGP[3]	PSDR[43]	—	pull-up[4]	—	57	—	
	$\overline{\text{IRQ10}}$	—	—	PGP[2]	PSDR[42]	—	pull-up[4]	—	29	—	
	$\overline{\text{IRQ9}}$	—	—	PGP[1]	PSDR[41]	—	pull-up[4]	—	11	—	
	$\overline{\text{IRQ8}}$	—	—	PGP[0]	PSDR[40]	—	pull-up[4]	—	10	—	
	$\overline{\text{IRQ7}}$	—	—	PNQ[7]	Low	—	pull-up[4]	—	56	40	
	$\overline{\text{IRQ6}}$	—	FEC_RXER	PNQ[6]	Low	—	pull-up[4]	—	19	—	
	$\overline{\text{IRQ5}}$	—	FEC_RXD[1]	PNQ[5]	Low	—	pull-up[4]	—	20	—	
	$\overline{\text{IRQ4}}$	—	—	PNQ[4]	Low	—	pull-up[4]	—	41	29	
	$\overline{\text{IRQ3}}$	—	FEC_RXD[2]	PNQ[3]	Low	—	pull-up[4]	—	53	—	
	$\overline{\text{IRQ2}}$	—	FEC_RXD[3]	PNQ[2]	Low	—	pull-up[4]	—	54	—	
	$\overline{\text{IRQ1}}$	SYNCA	PWM1	PNQ[1]	High	—	pull-up[4]	—	55	39	
JTAG/BDM	JTAG_EN	—	—	—	N/A	N/A	pull-down	—	18	12	
	TCLK/ PSTCLK	CLKOUT	—	—	High	—	pull-up[5]	—	1	1	
	TDI/DSI	—	—	—	N/A	N/A	pull-up[5]	—	4	4	
	TDO/DSO	—	—	—	High	N/A	—	—	5	5	
	TMS /$\overline{\text{BKPT}}$	—	—	—	N/A	N/A	pull-up[5]	—	2	2	
	$\overline{\text{TRST}}$ /DSCLK	—	—	—	N/A	N/A	pull-up[5]	—	6	6	
Mode Selection	$\overline{\text{RCON}}$/ EZPCS	—	—	—	N/A	N/A	pull-up	—	3	3	

Pin Group	Primary Function	Secondary Function	Tertiary Function	Quaternary Function	Drive Strength / Control[1]	Wired OR Control	Pull-up / Pull-down[2]	Pin on121 MAPBGA	Pin on 112 LQFP	Pin on 80 LQFP	Notes
PWM	PWM7	—	—	PTD[3]	PDSR[31]	—	—	—	104	—	
	PWM5	—	—	PTD[2]	PDSR[30]	—	—	—	103	—	
	PWM3	—	—	PTD[1]	PDSR[29]	—	—	—	100	—	
	PWM1	—	—	PTD[0]	PDSR[28]	—	—	—	99	—	
QSPI	QSPI_DIN/ EZPD	CANRX[3]	RXD1	PQS[1]	PDSR[2]	PWOR[4]	—	—	35	25	
	QSPI_DOUT/ EZPQ	CANTX[3]	TXD1	PQS[0]	PDSR[1]	PWOR[5]	—	—	34	26	
	QSPI_SCK/ EZPCK	SCL	$\overline{\text{RTS1}}$	PQS[2]	PDSR[3]	PWOR[6]	pull-up[6]	—	36	27	
	QSPI_CS3	SYNCA	SYNCB	PQS[6]	PDSR[7]	—	—	—	40	—	
	QSPI_CS2	—	—	PQS[5]	PDSR[6]	—	—	—	39	—	
	QSPI_CS1	—	—	PQS[4]	PDSR[5]	—	—	—	38	—	
	QSPI_CS0	SDA	$\overline{\text{CTS1}}$	PQS[3]	PDSR[4]	PWOR[7]	pull-up[6]	—	37	58	
Reset[7]	$\overline{\text{RSTI}}$	—	—	—	N/A	N/A	pull-up[7]	—	44	32	
	$\overline{\text{RSTO}}$	—	—	—	high	—	—	—	46	34	
Test	TEST	—	—	—	N/A	N/A	pull-down	—	50	38	
Timers, 16-bit	GPT3	FEC_TXD[3]	PWM7	PTA[3]	PDSR[23]	PWOR[23]	pull-up[8]	—	107	75	
	GPT2	FEC_TXD[2]	PWM5	PTA[2]	PDSR[22]	PWOR[22]	pull-up[8]	—	108	76	
	GPT1	FEC_TXD[1]	PWM3	PTA[1]	PDSR[21]	PWOR[21]	pull-up[8]	—	109	77	
	GPT0	FEC_TXER	PWM1	PTA[0]	PDSR[20]	PWOR[20]	pull-up[8]	—	110	78	
Timers, 32-bit	TIN3	TOUT3	PWM6	PTC[3]	PDSR[19]	PWOR[19]	—	—	22	14	
	TIN2	TOUT2	PWM4	PTC[2]	PDSR[18]	PWOR[18]	—	—	21	13	
	TIN1	TOUT1	PWM2	PTC[1]	PDSR[17]	PWOR[17]	—	—	9	9	
	TIN0	TOUT0	PWM0	PTC[0]	PDSR[16]	PWOR[16]	—	—	8	8	

Pin Group	Primary Function	Secondary Function	Tertiary Function	Quaternary Function	Drive Strength / Control[1]	Wired OR Control	Pull-up / Pull-down[2]	Pin on121 MAPBGA	Pin on 112 LQFP	Pin on 80 LQFP	Notes
UART 0	CTS0	CANRX[3]	FEC_RXCLK	PUA[3]	PDSR[11]	—	—	—	26	18	
	RTS0	CANTX[3]	FEC_RXDV	PUA[2]	PDSR[10]	—	—	—	25	17	
	RXD0	—	FEC_RXD[0]	PUA[1]	PDSR[9]	PWOR[0]	—	—	30	21	
	TXD0	—	FEC_CRS	PUA[0]	PDSR[8]	PWOR[1]	—	—	31	22	
UART 1	CTS1	SYNCA	RXD2	PUB[3]	PDSR[15]	—	—	—	24	16	
	RTS1	SYNCB	TXD2	PUB[2]	PDSR[14]	—	—	—	23	15	
	RXD1	—	FEC_TXD[0]	PUB[1]	PDSR[13]	PWOR[2]	—	—	32	23	
	TXD1	—	FEC_COL	PUB[0]	PDSR[12]	PWOR[3]	—	—	33	24	
UART 2	CTS2	—	—	PUC[3]	PDSR[27]	—	—	—	61	—	
	RTS2	—	—	PUC[2]	PDSR[26]	—	—	—	60	—	
	RXD2	—	—	PUC[1]	PDSR[25]	—	—	—	62	—	
	TXD2	—	—	PUC[30]	PDSR[24]	—	—	—	63	—	
FlexCAN	CANRX		FEC_MDIO	PAS[3]	PDSR[39]	—	—	—	—	—	See Note[3]
	CANTX		FEC_MDC	PAS[2]	PDSR[39]	—	—	—	—	—	See Note[3]
VDD[9]	VDD	—	—	—	N/A	N/A	—		14,43,65, 82,102	10,31,45, 58,74	
VSS	VSS	—	—	—	N/A	N/A	—		15,42, 64,101	11,30, 44,73	

NOTES:
1 The PDSR and PSSR registers are described in the MCF52235 Reference Manual. All programmable signals default to 2mA drive in normal (single-chip) mode.
2 All signals have a pull-up in GPIO mode.
3 The multiplexed CANTX and CANRX signals do not have dedicated pins, but are available as muxed replacements for other signals.
4 For primary and GPIO functions only.
5 Only when JTAG mode is enabled.
6 For secondary and GPIO functions only.
7 RSTI has an internal pull-up resistor, however the use of an external resistor is very strongly recommended
8 For GPIO function. Primary Function has pull-up control within the GPT module
9 This list for power and ground does not include those dedicated power/ground pins included elsewhere, e.g. in the ethernet PHY.

1.5 Reset Signals

Table 4 describes signals that are used to either reset the chip or as a reset indication.

Table 4. Reset Signals

Signal Name	Abbreviation	Function	I/O
Reset In	$\overline{\text{RSTI}}$	Primary reset input to the device. Asserting $\overline{\text{RSTI}}$ immediately resets the CPU and peripherals.	I
Reset Out	$\overline{\text{RSTO}}$	Driven low for 512 CPU clocks after the reset source has deasserted.	O

1.6 PLL and Clock Signals

Table 5 describes signals that are used to support the on-chip clock generation circuitry.

Table 5. PLL and Clock Signals

Signal Name	Abbreviation	Function	I/O
External Clock In	EXTAL	Crystal oscillator or external clock input.	I
Crystal	XTAL	Crystal oscillator output.	O
Clock Out	CLKOUT	This output signal reflects the internal system clock.	O

1.7 Mode Selection

Table 6 describes signals used in mode selection, Table 6 describes particular clocking modes.

Table 6. Mode Selection Signals

Signal Name	Abbreviation	Function	I/O
Reset Configuration	$\overline{\text{RCON}}$	The Serial Flash Programming mode is entered by asserting the $\overline{\text{RCON}}$ pin (with the TEST pin negated) as the chip comes out of reset. During this mode, the EzPort has access to the Flash memory which can be programmed from an external device.	
Test	TEST	Reserved for factory testing only and in normal modes of operation should be connected to VSS to prevent unintentional activation of test functions.	I

1.8 External Interrupt Signals

Table 7 describes the external interrupt signals.

Table 7. External Interrupt Signals

Signal Name	Abbreviation	Function	I/O
External Interrupts	$\overline{\text{IRQ}}$[15:1]	External interrupt sources.	I

1.9 Queued Serial Peripheral Interface (QSPI)

Table 8 describes QSPI signals.

Table 8. Queued Serial Peripheral Interface (QSPI) Signals

Signal Name	Abbreviation	Function	I/O
QSPI Synchronous Serial Output	QSPI_DOUT	Provides the serial data from the QSPI and can be programmed to be driven on the rising or falling edge of QSPI_CLK.	O
QSPI Synchronous Serial Data Input	QSPI_DIN	Provides the serial data to the QSPI and can be programmed to be sampled on the rising or falling edge of QSPI_CLK.	I
QSPI Serial Clock	QSPI_CLK	Provides the serial clock from the QSPI. The polarity and phase of QSPI_CLK are programmable.	O
Synchronous Peripheral Chip Selects	QSPI_CS[3:0]	QSPI peripheral chip selects that can be programmed to be active high or low.	O

1.10 Fast Ethernet Controller ePHY Signals

Table 9 describes the Fast Ethernet Controller (FEC) Signals.

Table 9. Fast Ethernet Controller (FEC) Signals

Signal Name	Abbreviation	Function	I/O
Twisted Pair Input +	RXP	Differential Ethernet twisted-pair input pin. This pin is high-impedance out of reset.	I
Twisted Pair Input -	RXN	Differential Ethernet twisted-pair input pin. This pin is high-impedance out of reset.	I
Twisted Pair Output +	TXN	Differential Ethernet twisted-pair output pin. This pin is high-impedance out of reset.	O
Twisted Pair Output -	TXP	Differential Ethernet twisted-pair output pin. This pin is high-impedance out of reset.	O
Bias Control Resistor	RBIAS	Connect a 12.4 kΩ (1.0%) external resistor, RBIAS, between the PHY_RBIAS pin and analog ground. Place this resistor as near to the chip pin as possible. Stray capacitance must be kept to less than 10 pF (>50 pF will cause instability). No high-speed signals can be permitted in the region of RBIAS.	I
Activity LED	ACT_LED	Indicates when the ePHY is transmitting or receiving	O
Link LED	LINK_LED	Indicates when the ePHY has a valid link	O
Speed LED	SPD_LED	Indicates the speed of the ePHY connection	O
Duplex LED	DUPLED	Indicates the duplex (full or half) of the ePHY connection	O
Collision LED	COLLED	Indicates if the ePHY detects a collision	O
Transmit LED	TXLED	Indicates if the ePHY is transmitting	O
Receive LED	RXLED	Indicates if the ePHY is receiving	O

1.11 I^2C I/O Signals

Table 10 describes the I^2C serial interface module signals.

Table 10. I^2C I/O Signals

Signal Name	Abbreviation	Function	I/O
Serial Clock	SCL	Open-drain clock signal for the for the I^2C interface. Either it is driven by the I^2C module when the bus is in master mode or it becomes the clock input when the I^2C is in slave mode.	I/O
Serial Data	SDA	Open-drain signal that serves as the data input/output for the I^2C interface.	I/O

1.12 UART Module Signals

Table 11 describes the UART module signals.

Table 11. UART Module Signals

Signal Name	Abbreviation	Function	I/O
Transmit Serial Data Output	UTXD*n*	Transmitter serial data outputs for the UART modules. The output is held high (mark condition) when the transmitter is disabled, idle, or in the local loopback mode. Data is shifted out, LSB first, on this pin at the falling edge of the serial clock source.	O
Receive Serial Data Input	URXD*n*	Receiver serial data inputs for the UART modules. Data is received on this pin LSB first. When the UART clock is stopped for power-down mode, any transition on this pin restarts it.	I
Clear-to-Send	$\overline{\text{UCTS}}n$	Indicate to the UART modules that they can begin data transmission.	I
Request-to-Send	$\overline{\text{URTS}}n$	Automatic request-to-send outputs from the UART modules. This signal can also be configured to be asserted and negated as a function of the RxFIFO level.	O

1.13 DMA Timer Signals

Table 12 describes the signals of the four DMA timer modules.

Table 12. DMA Timer Signals

Signal Name	Abbreviation	Function	I/O
DMA Timer Input	DTIN	Event input to the DMA timer modules.	I
DMA Timer Output	DTOUT	Programmable output from the DMA timer modules.	O

1.14 ADC Signals

Table 13 describes the signals of the Analog-to-Digital Converter.

Table 13. ADC Signals

Signal Name	Abbreviation	Function	I/O
Analog Inputs	AN[7:0]	Inputs to the A-to-D converter.	I
Analog Reference	V_{RH}	Reference voltage high and low inputs.	I
	V_{RL}		I
Analog Supply	V_{DDA}	Isolate the ADC circuitry from power supply noise	—
	V_{SSA}		—

1.15 General Purpose Timer Signals

Table 14 describes the General Purpose Timer Signals.

Table 14. GPT Signals

Signal Name	Abbreviation	Function	I/O
General Purpose Timer Input/Output	GPT[3:0]	Inputs to or outputs from the general purpose timer module	I/O

1.16 Pulse Width Modulator Signals

Table 15 describes the PWM signals.

Table 15. PWM Signals

Signal Name	Abbreviation	Function	I/O
PWM Output Channels	PWM[7:0]	Pulse width modulated output for PWM channels	O

1.17 Debug Support Signals

These signals are used as the interface to the on-chip JTAG controller and also to interface to the BDM logic.

Table 16. Debug Support Signals

Signal Name	Abbreviation	Function	I/O
JTAG Enable	JTAG_EN	Select between debug module and JTAG signals at reset	I
Test Reset	$\overline{\text{TRST}}$	This active-low signal is used to initialize the JTAG logic asynchronously.	I
Test Clock	TCLK	Used to synchronize the JTAG logic.	I
Test Mode Select	TMS	Used to sequence the JTAG state machine. TMS is sampled on the rising edge of TCLK.	I

Table 16. Debug Support Signals (continued)

Signal Name	Abbreviation	Function	I/O
Test Data Input	TDI	Serial input for test instructions and data. TDI is sampled on the rising edge of TCLK.	I
Test Data Output	TDO	Serial output for test instructions and data. TDO is tri-stateable and is actively driven in the shift-IR and shift-DR controller states. TDO changes on the falling edge of TCLK.	O
Development Serial Clock	DSCLK	Development Serial Clock-Internally synchronized input. (The logic level on DSCLK is validated if it has the same value on two consecutive rising bus clock edges.) Clocks the serial communication port to the debug module during packet transfers. Maximum frequency is PSTCLK/5. At the synchronized rising edge of DSCLK, the data input on DSI is sampled and DSO changes state.	I
Breakpoint	$\overline{\text{BKPT}}$	Breakpoint - Input used to request a manual breakpoint. Assertion of $\overline{\text{BKPT}}$ puts the processor into a halted state after the current instruction completes. Halt status is reflected on processor status signals () as the value 0xF.	I
Development Serial Input	DSI	Development Serial Input -Internally synchronized input that provides data input for the serial communication port to the debug module, once the DSCLK has been seen as high (logic 1).	I
Development Serial Output	DSO	Development Serial Output -Provides serial output communication for debug module responses. DSO is registered internally. The output is delayed from the validation of DSCLK high.	O
Debug Data	DDATA[3:0]	Display captured processor data and breakpoint status. The CLKOUT signal can be used by the development system to know when to sample DDATA[3:0].	O
Processor Status Clock	PSTCLK	Processor Status Clock - Delayed version of the processor clock. Its rising edge appears in the center of valid PST and DDATA output. PSTCLK indicates when the development system should sample PST and DDATA values. If real-time trace is not used, setting CSR[PCD] keeps PSTCLK, and PST and DDATA outputs from toggling without disabling triggers. Non-quiescent operation can be reenabled by clearing CSR[PCD], although the external development systems must resynchronize with the PST and DDATA outputs. PSTCLK starts clocking only when the first non-zero PST value (0xC, 0xD, or 0xF) occurs during system reset exception processing.	O
Processor Status Outputs	PST[3:0]	Indicate core status. Debug mode timing is synchronous with the processor clock; status is unrelated to the current bus transfer. The CLKOUT signal can be used by the development system to know when to sample PST[3:0].	O
All Processor Status Outputs	ALLPST	Logical “AND” of PST[3.0]	O

1.18 EzPort Signal Descriptions

Table 17 contains a list of EzPort external signals

Table 17. EzPort Signal Descriptions

Signal Name	Abbreviation	Function	I/O
EzPort Clock	EZPCK	Shift clock for EzPort transfers	I
EzPort Chip Select	$\overline{\text{EZPCS}}$	Chip select for signalling the start and end of serial transfers	I
EzPort Serial Data In	EZPD	EZPD is sampled on the rising edge of EZPCK	I
EzPort Serial Data Out	EZPQ	EZPQ transitions on the falling edge of EZPCK	O

1.19 Power and Ground Pins

The pins described in Table 18 provide system power and ground to the chip. Multiple pins are provided for adequate current capability. All power supply pins must have adequate bypass capacitance for high-frequency noise suppression.

Table 18. Power and Ground Pins

Signal Name	Abbreviation	Function	I/O
PLL Analog Supply	VDDPLL, VSSPLL	Dedicated power supply signals to isolate the sensitive PLL analog circuitry from the normal levels of noise present on the digital power supply.	I
Positive Supply	VDD	These pins supply positive power to the core logic.	I
Ground	VSS	This pin is the negative supply (ground) to the chip.	

Some of the V_{DD} and V_{SS} pins on the device are only to be used for noise bypass. Figure 4 shows a typical connection diagram. Pay particular attention to those pins which show only capacitor connections. Do not connect power supply voltage directly to these pins.

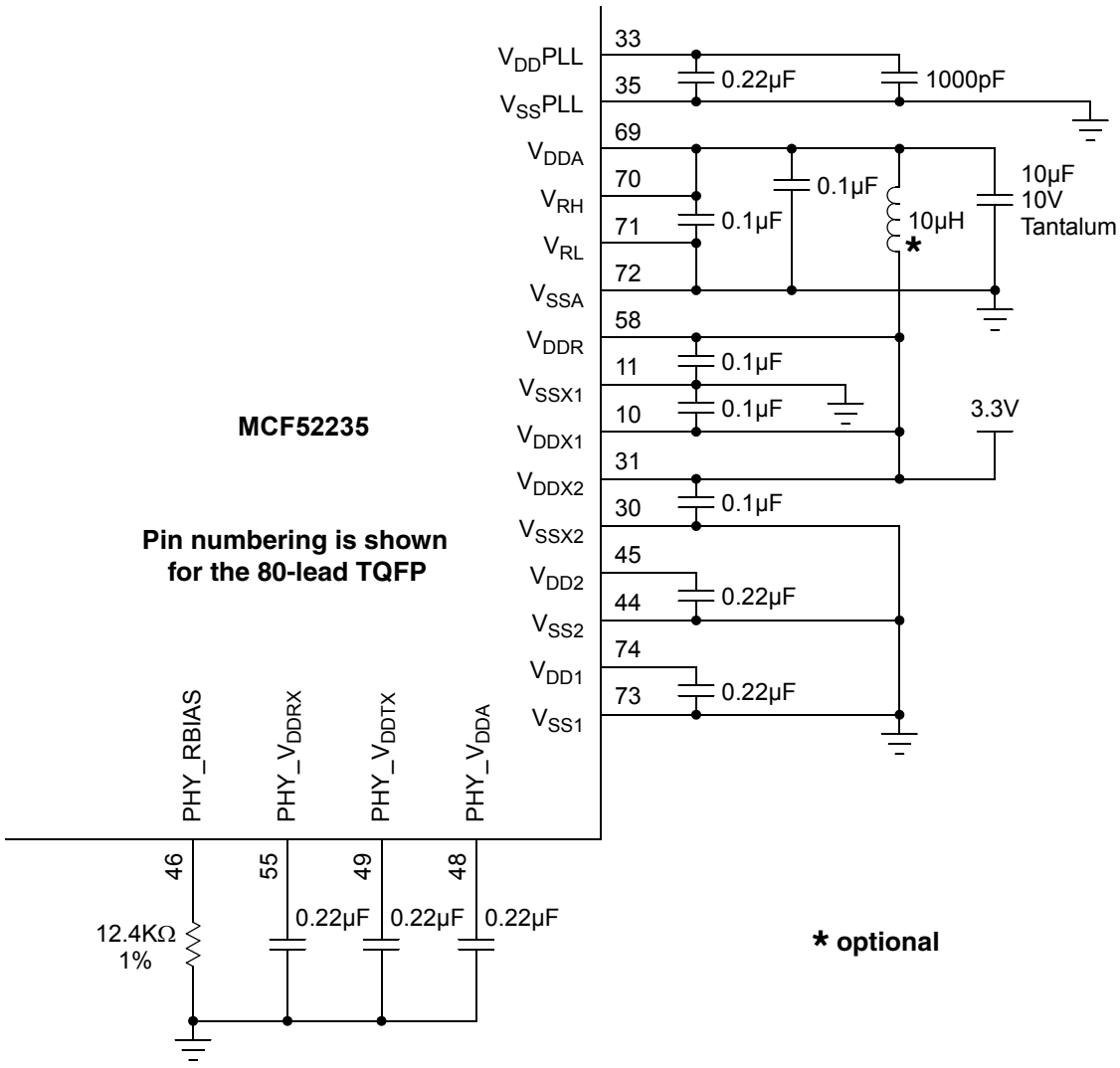

Figure 4. Suggested connection scheme for Power and Ground

2 Preliminary Electrical Characteristics

This section contains electrical specification tables and reference timing diagrams for the MCF52235 microcontroller unit. This section contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications of MCF52235.

The electrical specifications are preliminary and are from previous designs or design simulations. These specifications may not be fully tested or guaranteed at this early stage of the product life cycle, however for production silicon these specifications will be met. Finalized specifications will be published after complete characterization and device qualifications have been completed.

NOTE

The parameters specified in this appendix supersede any values found in the module specifications.

2.1 Maximum Ratings

Table 19. Absolute Maximum Ratings[1, 2]

Rating	Symbol	Value	Unit
Supply Voltage	V_{DD}	– 0.3 to +4.0	V
Clock Synthesizer Supply Voltage	V_{DDPLL}	– 0.3 to +4.0	V
RAM Memory Standby Supply Voltage	V_{STBY}	– 0.3 to + 4.0	V
Digital Input Voltage [3]	V_{IN}	– 0.3 to + 4.0	V
EXTAL pin voltage	V_{EXTAL}	0 to 3.3	V
XTAL pin voltage	V_{XTAL}	0 to 3.3	V
Instantaneous Maximum Current Single pin limit (applies to all pins) [4, 5]	I_{DD}	25	mA
Operating Temperature Range (Packaged)	T_A (T_L - T_H)	– 40 to 85	°C
Storage Temperature Range	T_{stg}	– 65 to 150	°C

NOTES:
1. Functional operating conditions are given in DC Electrical Specifications. Absolute Maximum Ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond those listed may affect device reliability or cause permanent damage to the device.
2. This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).
3. Input must be current limited to the I_{DD} value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.
4. All functional non-supply pins are internally clamped to V_{SS} and V_{DD}.
5. Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{in} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Insure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power (ex; no clock).Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions.

Table 20 lists thermal resistance values

Table 20. Thermal Characteristics

Characteristic		Symbol	Value	Unit
Junction to ambient, natural convection	112 LQFP Four layer board (2s2p)	θ_{JMA}	TBD[1,2]	°C/W
Junction to ambient (@200 ft/min)	112 LQFP Four layer board (2s2p)	θ_{JMA}	TBD	°C/W
Junction to board	112 LQFP	θ_{JB}	TBD[3]	°C/W
Junction to case	112 LQFP	θ_{JC}	TBD[4]	°C/W
Junction to top of package	Natural convection	Ψ_{jt}	TBD[5]	°C/W
Maximum operating junction temperature	112 LQFP	T_j	105	°C

NOTES:
1. θ_{JMA} and Ψ_{jt} parameters are simulated in conformance with EIA/JESD Standard 51-2 for natural convection. Freescale recommends the use of θ_{JmA} and power dissipation specifications in the system design to prevent device junction temperatures from exceeding the rated specification. System designers should be aware that device junction temperatures can be significantly influenced by board layout and surrounding devices. Conformance to the device junction temperature specification can be verified by physical measurement in the customer's system using the Ψ_{jt} parameter, the device power dissipation, and the method described in EIA/JESD Standard 51-2.
2. Per JEDEC JESD51-6 with the board horizontal.
3. Thermal resistance between the die and the printed circuit board in conformance with JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
4. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
5. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written in conformance with Psi-JT.

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \Theta_{JMA}) \quad (1)$$

Where:

T_A = Ambient Temperature, °C

Θ_{JMA} = Package Thermal Resistance, Junction-to-Ambient, °C/W

P_D = $P_{INT} + P_{I/O}$

P_{INT} = $I_{DD} \times V_{DD}$, Watts - Chip Internal Power

$P_{I/O}$ = Power Dissipation on Input and Output Pins — User Determined

For most applications $P_{I/O} < P_{INT}$ and can be ignored. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273°C) \quad (2)$$

Solving equations 1 and 2 for K gives:

$$K = P_D \times (T_A + 273\ °C) + \Theta_{JMA} \times P_D^2 \quad (3)$$

where K is a constant pertaining to the particular part. K can be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

2.2 ESD Protection

Table 21. ESD Protection Characteristics[1, 2]

Characteristics	Symbol	Value	Units
ESD Target for Human Body Model	HBM	2000	V
ESD Target for Machine Model	MM	200	V
HBM Circuit Description	R_{series}	1500	ohms
	C	100	pF
MM Circuit Description	R_{series}	0	ohms
	C	200	pF
Number of pulses per pin (HBM) positive pulses negative pulses	 — —	 1 1	—
Number of pulses per pin (MM) positive pulses negative pulses	 — —	 3 3	—
Interval of Pulses	—	1	sec

NOTES:
1 All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.
2 A device is defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing is performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

2.3 DC Electrical Specifications

Table 22. DC Electrical Specifications [1]

Characteristic	Symbol	Min	Max	Unit
Supply Voltage	V_{DD}	3.0	3.6	V
Input High Voltage	V_{IH}	0.7 x V_{DD}	4.0	V
Input Low Voltage	V_{IL}	V_{SS} – 0.3	0.35 x V_{DD}	V
Input Hysteresis	V_{HYS}	0.06 x V_{DD}	—	mV
Input Leakage Current V_{in} = V_{DD} or V_{SS}, Input-only pins	I_{in}	–1.0	1.0	μA
High Impedance (Off-State) Leakage Current V_{in} = V_{DD} or V_{SS}, All input/output and output pins	I_{OZ}	–1.0	1.0	μA
Output High Voltage (All input/output and all output pins) I_{OH} = –2.0 mA	V_{OH}	O V_{DD} - 0.5	—	V
Output Low Voltage (All input/output and all output pins) I_{OL} = 2.0mA	V_{OL}	—	0.5	V
Weak Internal Pull Up Device Current, tested at V_{IL} Max.[2]	I_{APU}	-10	- 130	μA
Input Capacitance [3] All input-only pins All input/output (three-state) pins	C_{in}	 — —	 7 7	pF
Load Capacitance[4] Low Drive Strength High Drive Strength	C_L		 25 50	pF

Table 22. DC Electrical Specifications (continued)[1]

Characteristic	Symbol	Min	Max	Unit
Operating Supply Current [5] Master Mode WAIT DOZE STOP	I_{DD}	 — — — —	 TBD TBD TBD TBD	 mA mA mA μA
DC Injection Current [3, 6, 7, 8] $V_{NEGCLAMP} = V_{SS} - 0.3$ V, $V_{POSCLAMP} = V_{DD} + 0.3$ Single Pin Limit Total MCU Limit, Includes sum of all stressed pins	I_{IC}	 -1.0 -10	 1.0 10	mA

NOTES:
1. Refer to Table 23 for additional PLL specifications.
2. Refer to the MCF52235 signals chapter for pins having weak internal pull-up devices.
3. This parameter is characterized before qualification rather than 100% tested.
4. pF load ratings are based on DC loading and are provided as an indication of driver strength. High speed interfaces require transmission line analysis to determine proper drive strength and termination.
5. Current measured at maximum system clock frequency, all modules active, and default drive strength with matching load.
6. All functional non-supply pins are internally clamped to V_{SS} and their respective V_{DD}.
7. Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.
8. Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{in} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Insure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if clock rate is very low which would reduce overall power consumption. Also, at power-up, system clock is not present during the power-up sequence until the PLL has attained lock.

2.4 Phase Lock Loop Electrical Specifications

Table 23. PLL Electrical Specifications

(V_{DD} and V_{DDPLL} = 2.7 to 3.6 V, $V_{SS} = V_{SSPLL}$ = 0 V)

Characteristic	Symbol	Min	Max	Unit
PLL Reference Frequency Range[1] Crystal reference External reference	 $f_{ref\_crystal}$ f_{ref_ext}	 2 2	 10.0 10.0	MHz
System Frequency [2] External Clock Mode On-Chip PLL Frequency	f_{sys}	 0 f_{ref} / 32	 60 60	MHz
Loss of Reference Frequency [3, 5]	f_{LOR}	100	1000	kHz
Self Clocked Mode Frequency [4, 5]	f_{SCM}	1	5	MHz
Crystal Start-up Time [5, 6]	t_{cst}	—	10	ms
EXTAL Input High Voltage Crystal reference External reference	V_{IHEXT}	 V_{DD}- 1.0 2.0	 V_{DD} V_{DD}	V
EXTAL Input Low Voltage Crystal reference External reference	V_{ILEXT}	 V_{SS} V_{SS}	 1.0 0.8	V

Table 23. PLL Electrical Specifications (continued)

(V_{DD} and V_{DDPLL} = 2.7 to 3.6 V, V_{SS} = V_{SSPLL} = 0 V)

Characteristic	Symbol	Min	Max	Unit
XTAL Output High Voltage I_{OH} = 1.0 mA	V_{OL}	 V_{DD}- 1.0	 —	V
XTAL Output Low Voltage I_{OL} = 1.0 mA	V_{OL}	 —	 0.5	V
XTAL Load Capacitance[7]		—	—	pF
PLL Lock Time[5,9]	t_{lpll}	—	500	µs
Power-up To Lock Time [5, 7,8] With Crystal Reference Without Crystal Reference	t_{lplk}	 — —	 10.5 500	 ms µs
Duty Cycle of reference [5]	t_{dc}	40	60	% f_{sys}
Frequency un-LOCK Range	f_{UL}	- 1.5	1.5	% f_{sys}
Frequency LOCK Range	fLCK	- 0.75	0.75	% % f_{sys}
CLKOUT Period Jitter [5, 6, 8, 9,10], Measured at f_{SYS} Max Peak-to-peak Jitter (Clock edge to clock edge) Long Term Jitter (Averaged over 2 ms interval)	C_{jitter}	 — —	 5 .01	% f_{sys}

NOTES:
1. Input to the PLL is limited to 10MHz max, however the PLL divider can accept up to 40MHz. The input must be divided down to a frequency no greater than 10MHz. This is controlled by register CCHR.
2. All internal registers retain data at 0 Hz.
3. "Loss of Reference Frequency" is the reference frequency detected internally, which transitions the PLL into self clocked mode.
4. Self clocked mode frequency is the frequency that the PLL operates at when the reference frequency falls below f_{LOR} with default MFD/RFD settings.
5. This parameter is characterized before qualification rather than 100% tested.
6. Proper PC board layout procedures must be followed to achieve specifications.
7. Load Capacitance determined from crystal manufacturer specifications and will include circuit board parasitics.
8. Assuming a reference is available at power up, lock time is measured from the time V_{DD} and V_{DDPLL} are valid to $\overline{RSTO}$ negating. If the crystal oscillator is being used as the reference for the PLL, then the crystal start up time must be added to the PLL lock time to determine the total start-up time.
9. Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{sys}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the PLL circuitry via V_{DDPLL} and V_{SSPLL} and variation in crystal oscillator frequency increase the Cjitter percentage for a given interval
10. Based on slow system clock of 40 MHz measured at f_{sys} max.

2.5 General Purpose I/O Timing

GPIO can be configured for certain pins of the QSPI, TIMERS, UARTS, FEC, Interrupts and USB interfaces. When in GPIO mode, the timing specification for these pins is given in Table 24 and Figure 5.

Table 24. GPIO Timing

NUM	Characteristic	Symbol	Min	Max	Unit
G1	CLKOUT High to GPIO Output Valid	t_{CHPOV}	-	10	ns
G2	CLKOUT High to GPIO Output Invalid	t_{CHPOI}	1.5	-	ns
G3	GPIO Input Valid to CLKOUT High	t_{PVCH}	9	-	ns
G4	CLKOUT High to GPIO Input Invalid	t_{CHPI}	1.5	-	ns

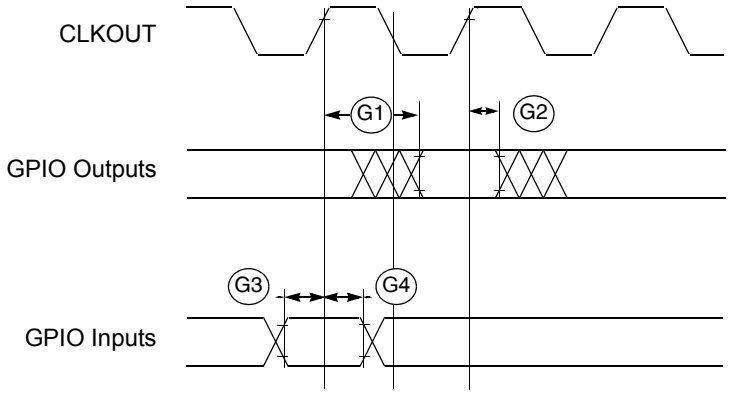

Figure 5. GPIO Timing

2.6 Reset Timing

Table 25. Reset and Configuration Override Timing

(V_{DD} = 2.7 to 3.6 V, V_{SS} = 0 V, T_A = T_L to T_H)[1]

NUM	Characteristic	Symbol	Min	Max	Unit
R1	$\overline{RSTI}$ Input valid to CLKOUT High	t_{RVCH}	9	-	ns
R2	CLKOUT High to $\overline{RSTI}$ Input invalid	t_{CHRI}	1.5	-	ns
R3	$\overline{RSTI}$ Input valid Time [2]	t_{RIVT}	5	-	t_{CYC}
R4	CLKOUT High to $\overline{RSTO}$ Valid	t_{CHROV}	-	10	ns

NOTES:
1 All AC timing is shown with respect to 50% O V_{DD} levels unless otherwise noted.
2 During low power STOP, the synchronizers for the $\overline{RSTI}$ input are bypassed and $\overline{RSTI}$ is asserted asynchronously to the system. Thus, $\overline{RSTI}$ must be held a minimum of 100 ns.

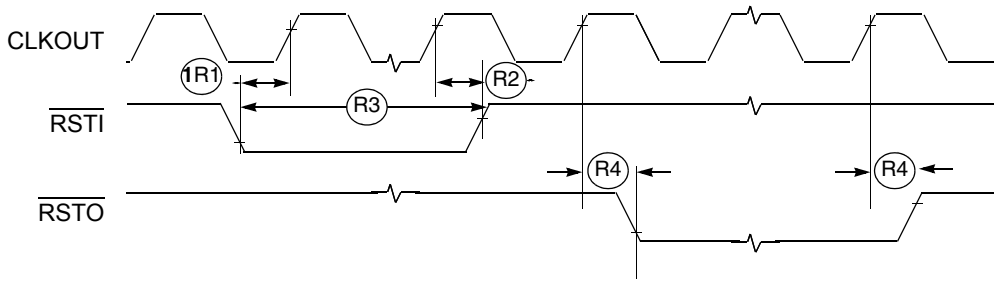

Figure 6. $\overline{\text{RSTI}}$ and Configuration Override Timing

2.7 I²C Input/Output Timing Specifications

Table 26 lists specifications for the I²C input timing parameters shown in Figure 7.

Table 26. I²C Input Timing Specifications between I2C_SCL and I2C_SDA

Num	Characteristic	Min	Max	Units
11	Start condition hold time	2 x t_{CYC}	—	ns
I2	Clock low period	8 x t_{CYC}	—	ns
I3	SCL/SDA rise time (V_{IL} = 0.5 V to V_{IH} = 2.4 V)	—	1	mS
I4	Data hold time	0	—	ns
I5	SCL/SDA fall time (V_{IH} = 2.4 V to V_{IL} = 0.5 V)	—	1	mS
I6	Clock high time	4 x t_{CYC}	—	ns
I7	Data setup time	0	—	ns
I8	Start condition setup time (for repeated start condition only)	2 x t_{CYC}	—	ns
I9	Stop condition setup time	2 x t_{CYC}	—	ns

Table 27 lists specifications for the I²C output timing parameters shown in Figure 7.

Table 27. I²C Output Timing Specifications between I2C_SCL and I2C_SDA

Num	Characteristic	Min	Max	Units
11[1]	Start condition hold time	6 x t_{CYC}	—	ns
I2[1]	Clock low period	10 x t_{CYC}	—	ns
I3[2]	I2C_SCL/I2C_SDA rise time (V_{IL} = 0.5 V to V_{IH} = 2.4 V)	—	—	µS
I4[1]	Data hold time	7 x t_{CYC}	—	ns
I5[3]	I2C_SCL/I2C_SDA fall time (V_{IH} = 2.4 V to V_{IL} = 0.5 V)	—	3	ns
I6[1]	Clock high time	10 x t_{CYC}	—	ns
I7[1]	Data setup time	2 x t_{CYC}	—	ns

Table 27. I^2C Output Timing Specifications between I2C_SCL and I2C_SDA (continued)

Num	Characteristic	Min	Max	Units
I8 [1]	Start condition setup time (for repeated start condition only)	20 x t_{CYC}	—	ns
I9 [1]	Stop condition setup time	10 x t_{CYC}	—	ns

NOTES:
1. Note: Output numbers depend on the value programmed into the IFDR; an IFDR programmed with the maximum frequency (IFDR = 0x20) results in minimum output timings as shown in Table 27. The I^2C interface is designed to scale the actual data transition time to move it to the middle of the SCL low period. The actual position is affected by the prescale and division values programmed into the IFDR; however, the numbers given in Table 27 are minimum values.
2. Because SCL and SDA are open-collector-type outputs, which the processor can only actively drive low, the time SCL or SDA take to reach a high level depends on external signal capacitance and pull-up resistor values.
3. Specified at a nominal 50-pF load.

Figure 7 shows timing for the values in Table 26 and Table 27.

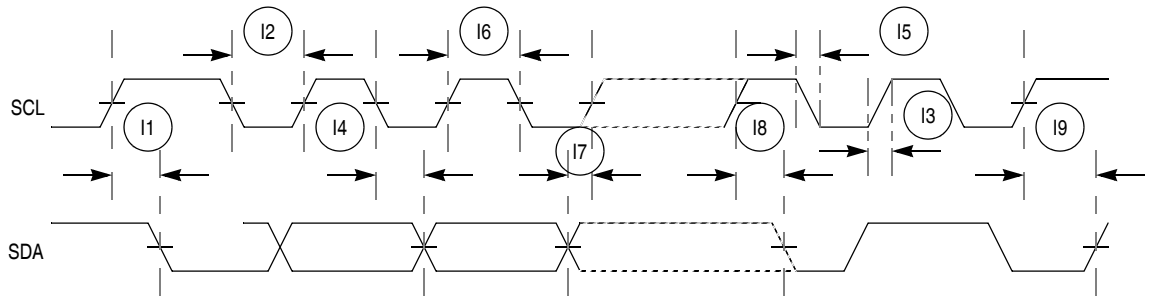

Figure 7. I^2C Input/Output Timings

2.8 Analog-to-Digital Converter (ADC) Parameters

Table 28 lists specifications for the analog-to-digital converter.

Table 28. ADC Parameters[1]

Name	Characteristic	Min	Typical	Max	Unit
V_{ADIN}	Input voltages	V_{REFL}	—	V_{REFH}	V
R_{ES}	Resolution	12	—	12	Bits
INL	Integral Non-Linearity (Full input signal range)[2]	—	±2.5	±3	LSB[3]
INL	Integral Non-Linearity (10% to 90% input signal range)[4]	—	±2.5	±3	LSB
DNL	Differential Non-Linearity	—	-1 < DNL < +1	<+1	LSB
	Monotonicity	GUARANTEED			
f_{ADIC}	ADC internal clock	0.1	—	5.0	MHz
R_{AD}	Conversion Range	V_{REFL}	—	V_{REFH}	V

Table 28. ADC Parameters[1] (continued)

Name	Characteristic	Min	Typical	Max	Unit
t_{ADPU}	ADC power-up time[5]	—	6	13	t_{AIC} cycles[6]
t_{REC}	Recovery from auto standby	—	0	1	t_{AIC} cycles
t_{ADC}	Conversion time	—	6	—	t_{AIC} cycles
t_{ADS}	Sample time	—	1	—	t_{AIC} cycles
C_{ADI}	Input capacitance	—	TBD	—	pF
X_{IN}	Input impedance		TBD		Ω
I_{ADI}	Input injection current[7], per pin	—	—	3	mA
I_{VREFH}	V_{REFH} current	—	0	—	µ
V_{OFFSET}	Offset voltage internal reference	—	±11	±15	mV
E_{GAIN}	Gain Error (transfer path)	.99	1	1.01	—
V_{OFFSET}	Offset voltage external reference	—	±3	TBD	mV
SNR	Signal-to-Noise ratio	TBD	62 to 66		dB
THD	Total Harmonic Distortion	TBD	-75		dB
SFDR	Spurious Free Dynamic Range	TBD	75		dB
SINAD	Signal-to-Noise plus Distortion	TBD	65		dB
ENOB	Effective Number OF Bits	9.1	10.6		Bits

NOTES:
1. All measurements are preliminary pending full characterization, and were made at V_{DD} = 3.3V, V_{REFH} = 3.3V, and V_{REFL} = ground
2. INL measured from $V_{IN} = V_{REFL}$ to $V_{IN} = V_{REFH}$
3. LSB = Least Significant Bit
4. INL measured from $V_{IN} = 0.1V_{REFH}$ to $V_{IN} = 0.9V_{REFH}$
5. Includes power-up of ADC and V_{REF}
6. ADC clock cycles
7. The current that can be injected or sourced from an unselected ADC signal input without impacting the performance of the ADC

2.9 DMA Timers Timing Specifications

Table 29 lists timer module AC timings.

Table 29. Timer Module AC Timing Specifications

Name	Characteristic [1]	Min	Max	Unit
T1	DTIN0 / DTIN1 / DTIN2 / DTIN3 cycle time	3 x t_{CYC}	—	ns
T2	DTIN0 / DTIN1 / DTIN2 / DTIN3 pulse width	1 x t_{CYC}	—	ns

NOTES:
1. All timing references to CLKOUT are given to its rising edge.

2.10 QSPI Electrical Specifications

Table 30 lists QSPI timings.

Table 30. QSPI Modules AC Timing Specifications

Name	Characteristic	Min	Max	Unit
QS1	QSPI_CS[3:0] to QSPI_CLK	1	510	t_{CYC}
QS2	QSPI_CLK high to QSPI_DOUT valid.	—	10	ns
QS3	QSPI_CLK high to QSPI_DOUT invalid (Output hold)	2	—	ns
QS4	QSPI_DIN to QSPI_CLK (Input setup)	9	—	ns
QS5	QSPI_DIN to QSPI_CLK (Input hold)	9	—	ns

The values in Table 30 correspond to Figure 8.

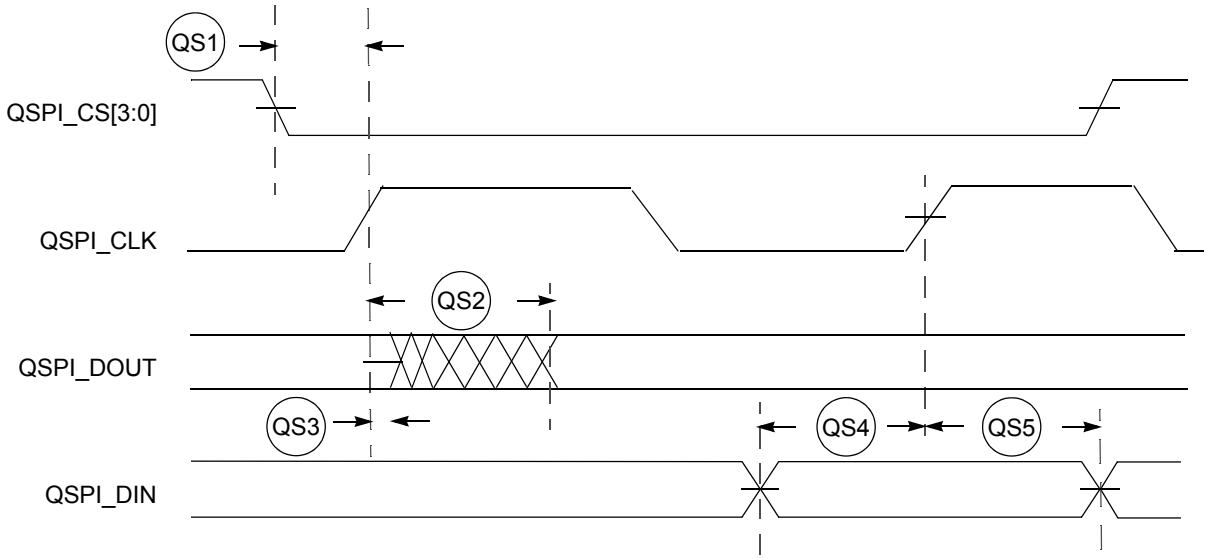

Figure 8. QSPI Timing

2.11 JTAG and Boundary Scan Timing

Table 31. JTAG and Boundary Scan Timing

Num	Characteristics[1]	Symbol	Min	Max	Unit
J1	TCLK Frequency of Operation	f_{JCYC}	DC	1/4	$f_{sys/2}$
J2	TCLK Cycle Period	t_{JCYC}	4 x t_{CYC}	-	ns
J3	TCLK Clock Pulse Width	t_{JCW}	26	-	ns
J4	TCLK Rise and Fall Times	t_{JCRF}	0	3	ns
J5	Boundary Scan Input Data Setup Time to TCLK Rise	t_{BSDST}	4	-	ns
J6	Boundary Scan Input Data Hold Time after TCLK Rise	t_{BSDHT}	26	-	ns

Table 31. JTAG and Boundary Scan Timing (continued)

Num	Characteristics[1]	Symbol	Min	Max	Unit
J7	TCLK Low to Boundary Scan Output Data Valid	t_{BSDV}	0	33	ns
J8	TCLK Low to Boundary Scan Output High Z	t_{BSDZ}	0	33	ns
J9	TMS, TDI Input Data Setup Time to TCLK Rise	t_{TAPBST}	4	-	ns
J10	TMS, TDI Input Data Hold Time after TCLK Rise	t_{TAPBHT}	10	-	ns
J11	TCLK Low to TDO Data Valid	t_{TDODV}	0	26	ns
J12	TCLK Low to TDO High Z	t_{TDODZ}	0	8	ns
J13	$\overline{TRST}$ Assert Time	t_{TRSTAT}	100	-	ns
J14	$\overline{TRST}$ Setup Time (Negation) to TCLK High	t_{TRSTST}	10	-	ns

NOTES:
1 JTAG_EN is expected to be a static signal. Hence, it is not associated with any timing.

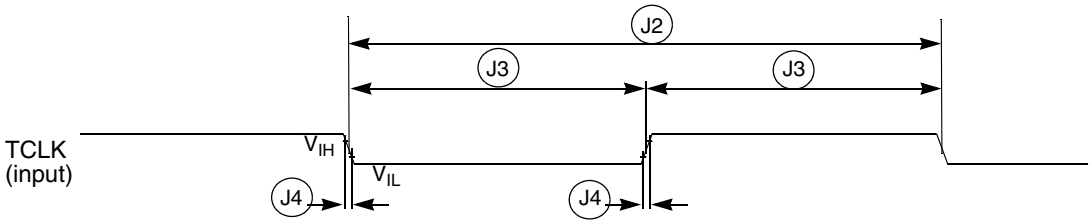

Figure 9. Test Clock Input Timing

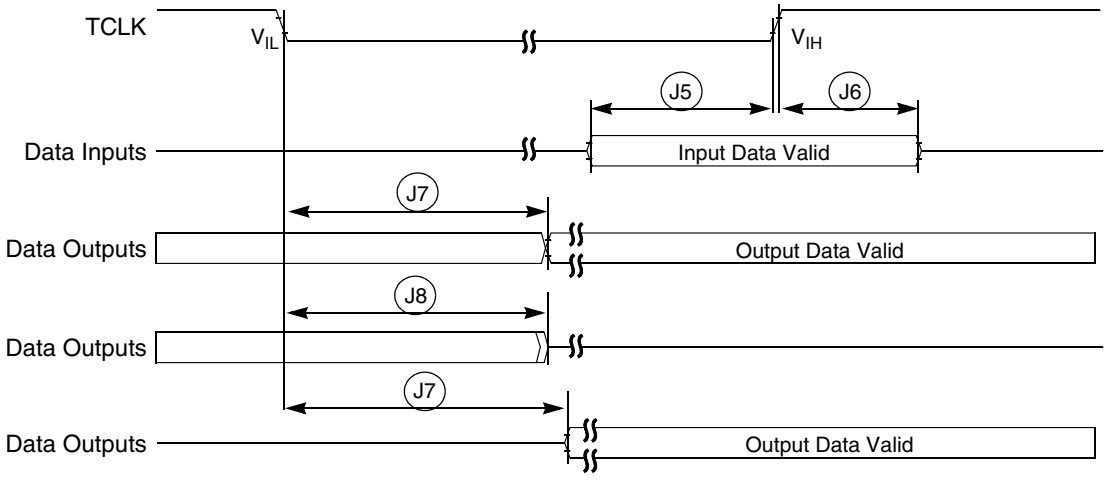

Figure 10. Boundary Scan (JTAG) Timing

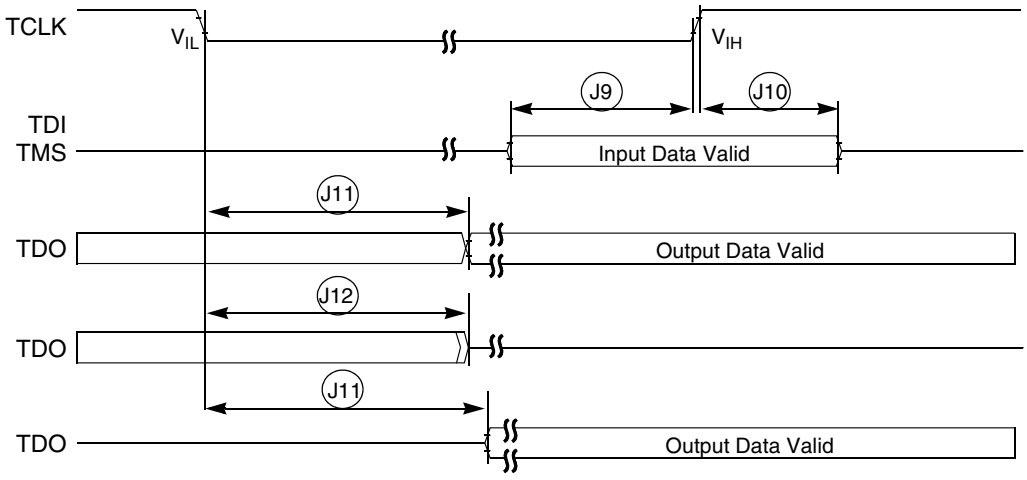

Figure 11. Test Access Port Timing

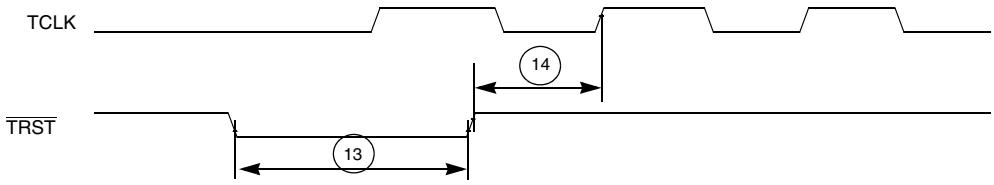

Figure 12. TRST Timing

2.12 Debug AC Timing Specifications

Table 32 lists specifications for the debug AC timing parameters shown in Figure 14.

Table 32. Debug AC Timing Specification

Num	Characteristic	60 MHz		Units
		Min	Max	
D0	PSTCLK cycle time		0.5	t_{CYC}
D1	PST, DDATA to CLKOUT setup	4		ns
D2	CLKOUT to PST, DDATA hold	1.5		ns
D3	DSI-to-DSCLK setup	1 x t_{CYC}		ns
D4 [1]	DSCLK-to-DSO hold	4 x t_{CYC}		ns
D5	DSCLK cycle time	5 x t_{CYC}		ns
D6	$\overline{BKPT}$ input data setup time to CLKOUT Rise	4		ns
D7	$\overline{BKPT}$ input data hold time to CLKOUT Rise	1.5		ns
D8	CLKOUT high to $\overline{BKPT}$ high Z	0.0	10.0	ns

NOTES:
1 DSCLK and DSI are synchronized internally. D4 is measured from the synchronized DSCLK input relative to the rising edge of CLKOUT.

Figure 13 shows real-time trace timing for the values in Table 32.

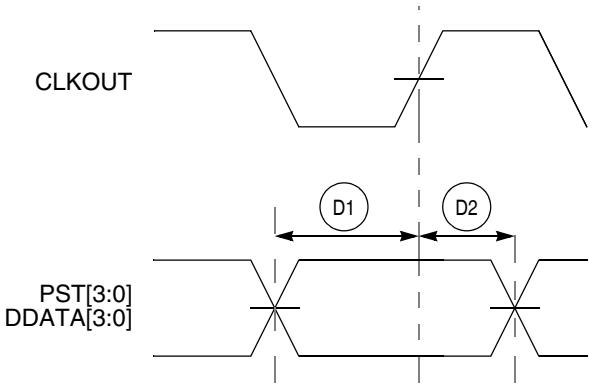

Figure 13. Real-Time Trace AC Timing

Figure 14 shows BDM serial port AC timing for the values in Table 32.

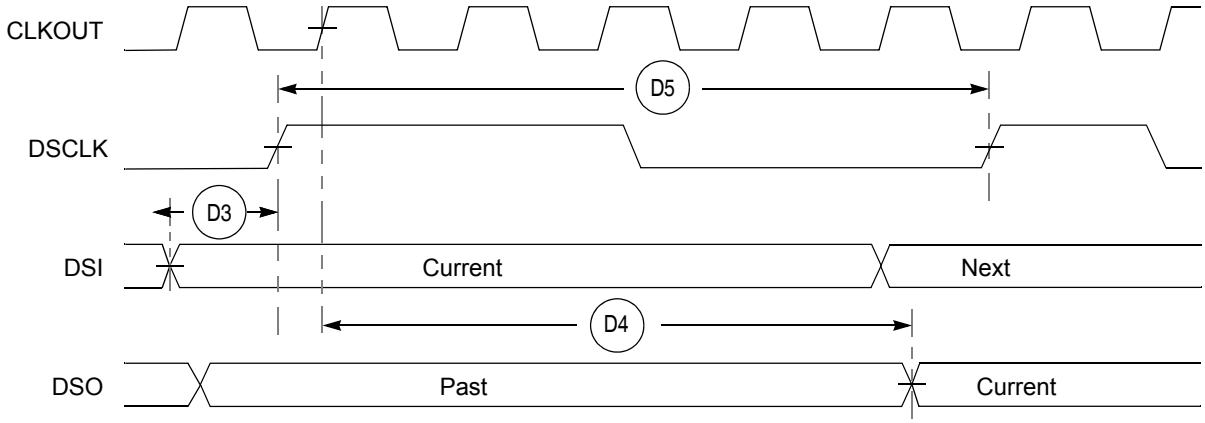

Figure 14. BDM Serial Port AC Timing

3 Mechanical Outline Drawings

This section describes the physical properties of the MCF52235 and its derivatives.

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. DATUMS A, B AND D TO BE DETERMINED AT DATUM PLANE H.
4. DIMENSIONS TO BE DETERMINED AT SEATING PLANE C.
5. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE UPPER LIMIT BY MORE THAN 0.08 mm AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT BE LESS THAN 0.07 mm.
6. THIS DIMENSION DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. THIS DIMENSION IS MAXIMUM PLASTIC BODY SIZE DIMENSION INCLUDING MOLD MISMATCH.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1 mm AND 0.25 mm FROM THE LEAD TIP.

MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE

TITLE: 64LD LQFP, 10 X 10 X 1.4 PKG, 0.5 PITCH, CASE OUTLINE	DOCUMENT NO: 98ASS23234W	REV: D
	CASE NUMBER: 840F-02	06 APR 2005
	STANDARD: JEDEC MS-026 BCD	

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