



PIMC31

500 mA, 50 V NPN/PNP double resistor-equipped transistor;
R1 = 1 k Ω , R2 = 10 k Ω

Rev. 01 — 24 March 2009

Product data sheet

1. Product profile

1.1 General description

500 mA, 50 V NPN/PNP double Resistor-Equipped Transistor (RET) in a small SOT457 (SC-74) Surface-Mounted Device (SMD) plastic package.

NPN/NPN complement: PIMN31

1.2 Features

- 500 mA output current capability
- Built-in bias resistors
- Simplifies circuit design
- Reduces component count
- Reduces pick and place costs
- AEC-Q101 qualified

1.3 Applications

- Digital application in automotive and industrial segments
- Switching loads

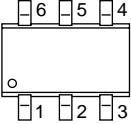
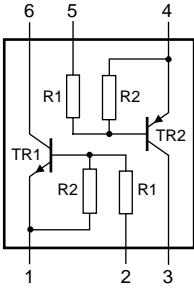
1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Per transistor; for the PNP transistor with negative polarity						
V _{CEO}	collector-emitter voltage	open base	-	-	50	V
I _O	output current		-	-	500	mA
R1	bias resistor 1 (input)		0.7	1	1.3	k Ω
R2/R1	bias resistor ratio		9	10	11	

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	GND (emitter) TR1		
2	input (base) TR1		
3	output (collector) TR2		
4	GND (emitter) TR2		
5	input (base) TR2		
6	output (collector) TR1		

006aaa143

3. Ordering information

Table 3. Ordering information

Type number	Package		Version
	Name	Description	
PIMC31	SC-74	plastic surface-mounted package (TSOP6); 6 leads	SOT457

4. Marking

Table 4. Marking codes

Type number	Marking code
PIMC31	ZH

5. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
Per transistor; for the PNP transistor with negative polarity					
V_{CBO}	collector-base voltage	open emitter	-	50	V
V_{CEO}	collector-emitter voltage	open base	-	50	V
V_{EBO}	emitter-base voltage	open collector	-	5	V
V_I	input voltage TR1				
		positive	-	+10	V
		negative	-	-5	V
	input voltage TR2				
		positive	-	+5	V
		negative	-	-10	V

Table 5. Limiting values ...continued
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
I_O	output current		-	500	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25\text{ °C}$	[1]	290	mW
Per device					
P_{tot}	total power dissipation	$T_{amb} \leq 25\text{ °C}$	[1]	420	mW
T_j	junction temperature		-	150	°C
T_{amb}	ambient temperature		-55	+150	°C
T_{stg}	storage temperature		-65	+150	°C

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.

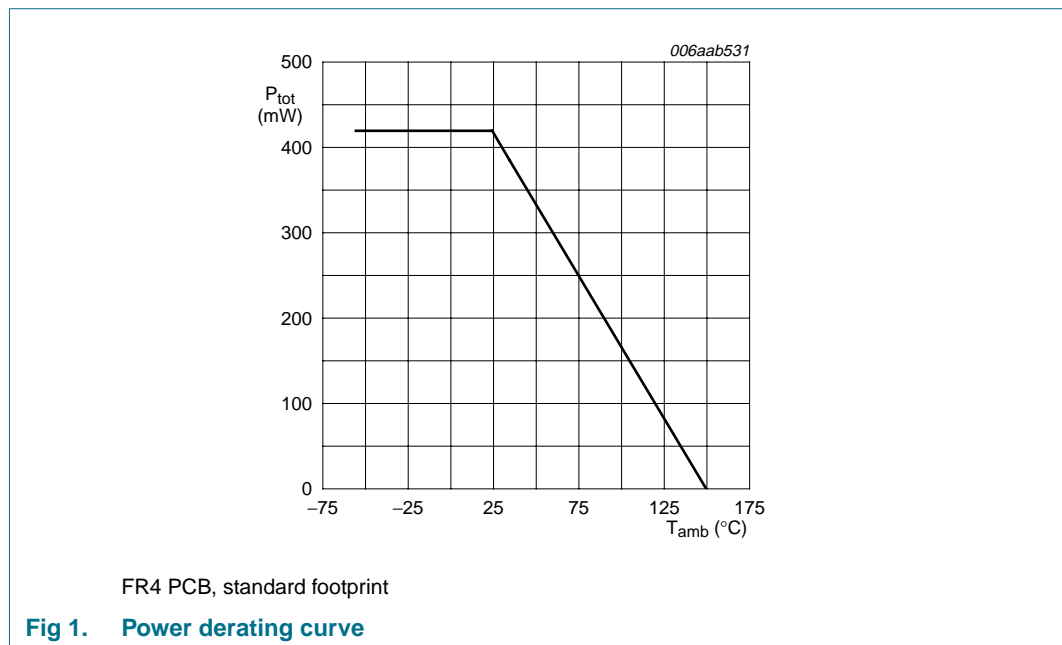


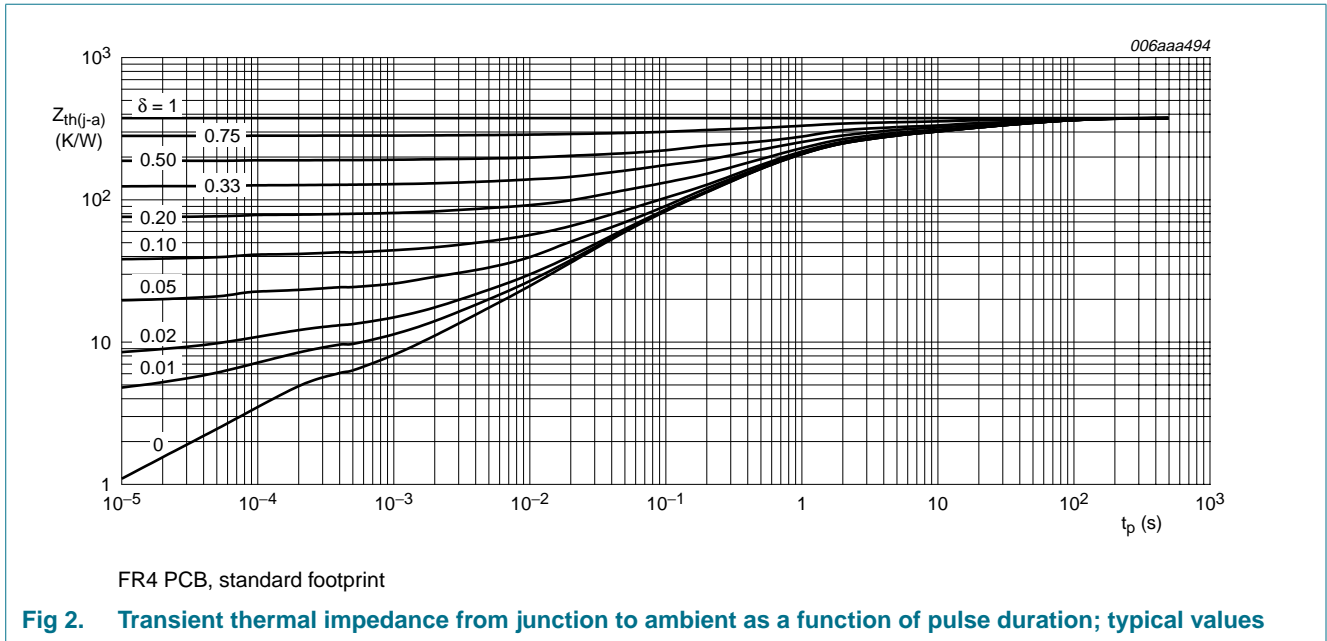
Fig 1. Power derating curve

6. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Per transistor						
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	431	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point		-	-	105	K/W
Per device						
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	298	K/W

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

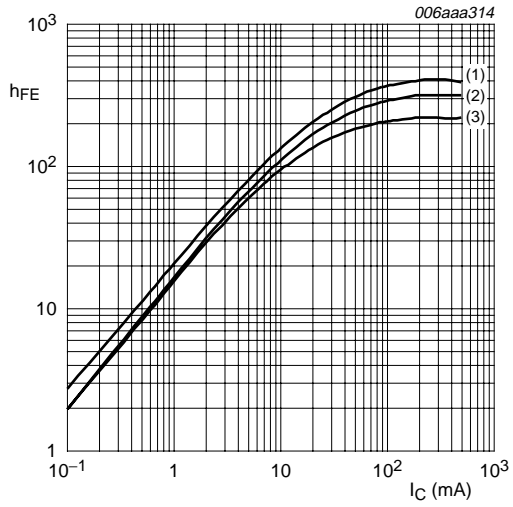


7. Characteristics

Table 7. Characteristics

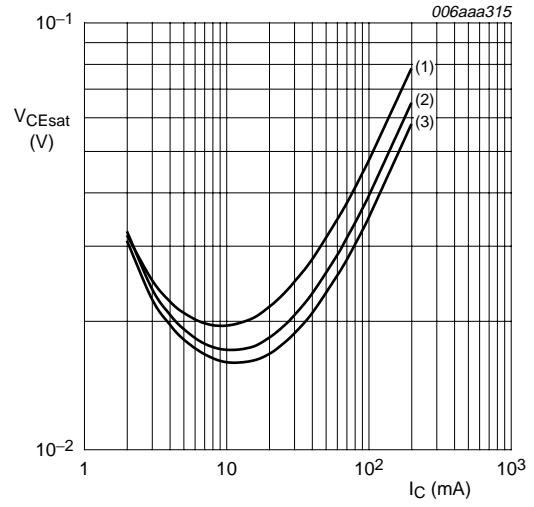
$T_{amb} = 25^{\circ}C$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Per transistor; for the PNP transistor with negative polarity						
I_{CBO}	collector-base cut-off current	$V_{CB} = 50\text{ V}; I_E = 0\text{ A}$	-	-	100	nA
I_{CEO}	collector-emitter cut-off current	$V_{CE} = 50\text{ V}; I_B = 0\text{ A}$	-	-	0.5	μA
I_{EBO}	emitter-base cut-off current	$V_{EB} = 5\text{ V}; I_C = 0\text{ A}$	-	-	0.72	mA
h_{FE}	DC current gain	$V_{CE} = 5\text{ V}; I_C = 50\text{ mA}$	70	-	-	
V_{CEsat}	collector-emitter saturation voltage	$I_C = 50\text{ mA}; I_B = 2.5\text{ mA}$	-	-	0.3	V
$V_{I(off)}$	off-state input voltage	$V_{CE} = 5\text{ V}; I_C = 100\ \mu\text{A}$	0.3	0.6	1	V
$V_{I(on)}$	on-state input voltage	$V_{CE} = 0.3\text{ V}; I_C = 20\text{ mA}$	0.4	0.8	1.4	V
R1	bias resistor 1 (input)		0.7	1	1.3	kΩ
R2/R1	bias resistor ratio		9	10	11	
C_c	collector capacitance	$V_{CB} = 10\text{ V}; I_E = i_e = 0\text{ A};$ $f = 1\text{ MHz}$				
	TR1 (NPN)		-	7	-	pF
	TR2 (PNP)		-	11	-	pF



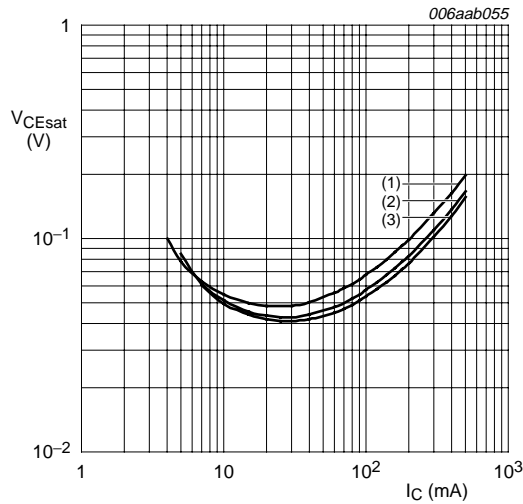
- V_{CE} = 5 V
- (1) T_{amb} = 100 °C
 - (2) T_{amb} = 25 °C
 - (3) T_{amb} = -40 °C

Fig 3. TR1 (NPN): DC current gain as a function of collector current; typical values



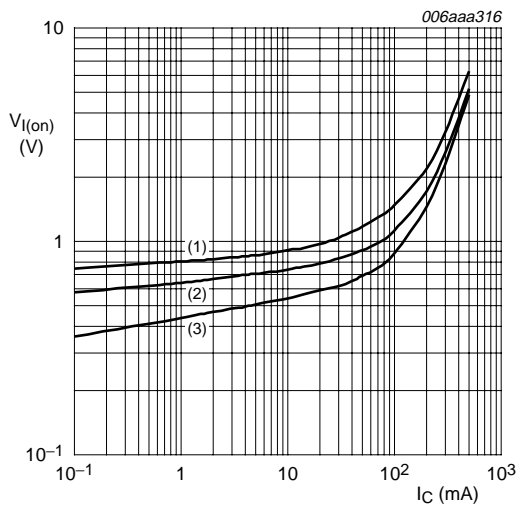
- I_C/I_B = 20
- (1) T_{amb} = 100 °C
 - (2) T_{amb} = 25 °C
 - (3) T_{amb} = -40 °C

Fig 4. TR1 (NPN): Collector-emitter saturation voltage as a function of collector current; typical values



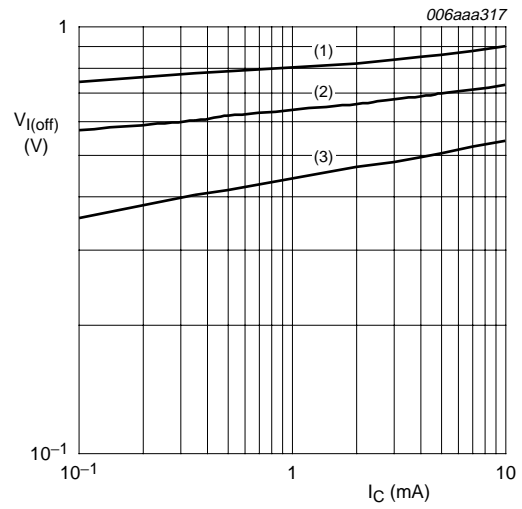
- I_C/I_B = 50
- (1) T_{amb} = 100 °C
 - (2) T_{amb} = 25 °C
 - (3) T_{amb} = -40 °C

Fig 5. TR1 (NPN): Collector-emitter saturation voltage as a function of collector current; typical values



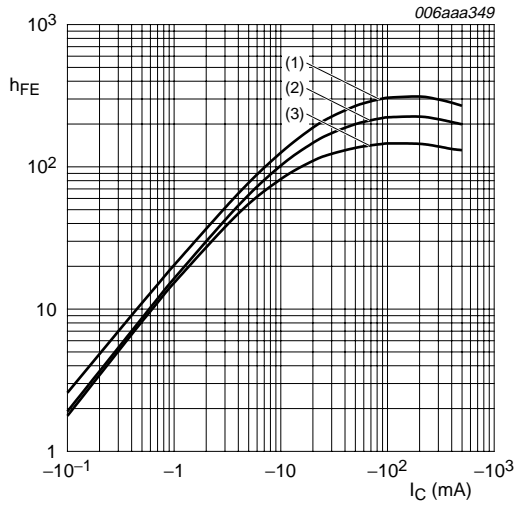
$V_{CE} = 0.3 \text{ V}$
 (1) $T_{amb} = -40 \text{ }^\circ\text{C}$
 (2) $T_{amb} = 25 \text{ }^\circ\text{C}$
 (3) $T_{amb} = 100 \text{ }^\circ\text{C}$

Fig 6. TR1 (NPN): On-state input voltage as a function of collector current; typical values



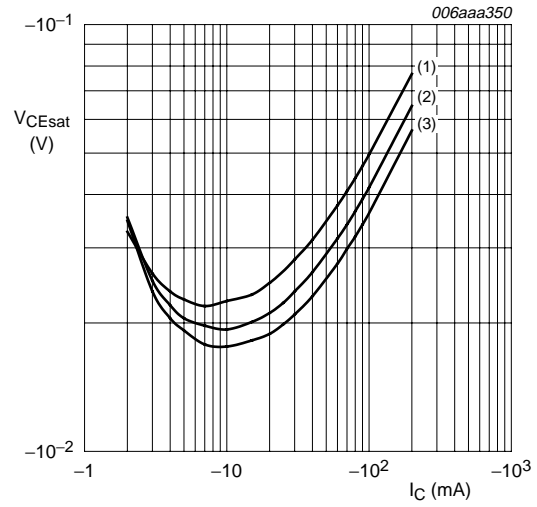
$V_{CE} = 5 \text{ V}$
 (1) $T_{amb} = -40 \text{ }^\circ\text{C}$
 (2) $T_{amb} = 25 \text{ }^\circ\text{C}$
 (3) $T_{amb} = 100 \text{ }^\circ\text{C}$

Fig 7. TR1 (NPN): Off-state input voltage as a function of collector current; typical values



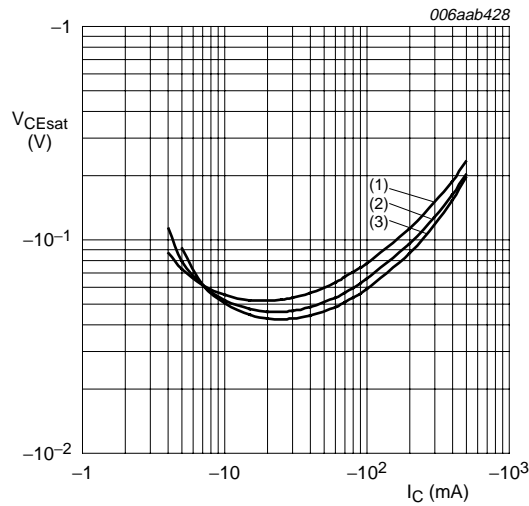
$V_{CE} = -5\text{ V}$
 (1) $T_{amb} = 100\text{ °C}$
 (2) $T_{amb} = 25\text{ °C}$
 (3) $T_{amb} = -40\text{ °C}$

Fig 8. TR2 (PNP): DC current gain as a function of collector current; typical values



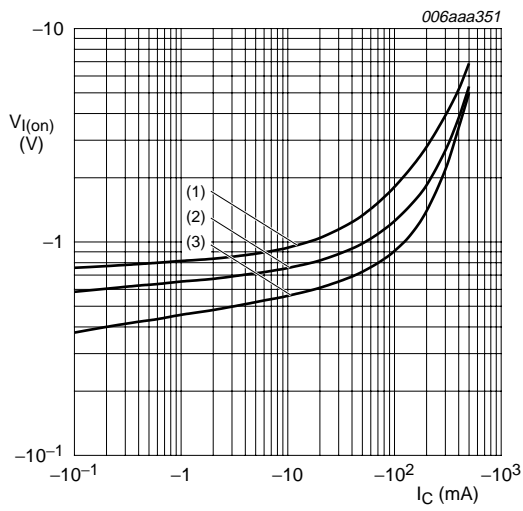
$I_C/I_B = 20$
 (1) $T_{amb} = 100\text{ °C}$
 (2) $T_{amb} = 25\text{ °C}$
 (3) $T_{amb} = -40\text{ °C}$

Fig 9. TR2 (PNP): Collector-emitter saturation voltage as a function of collector current; typical values



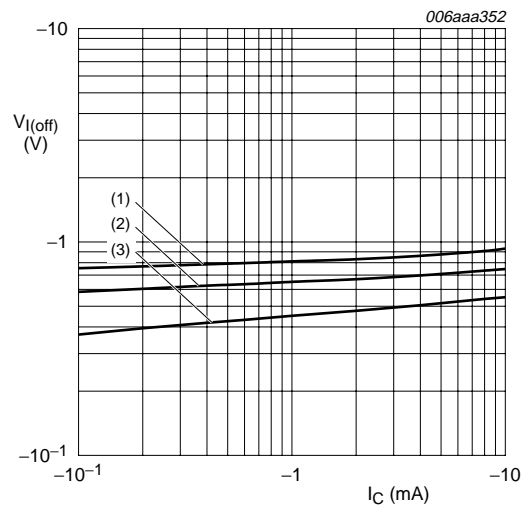
$I_C/I_B = 50$
 (1) $T_{amb} = 100\text{ °C}$
 (2) $T_{amb} = 25\text{ °C}$
 (3) $T_{amb} = -40\text{ °C}$

Fig 10. TR2 (PNP): Collector-emitter saturation voltage as a function of collector current; typical values



- $V_{CE} = -0.3 \text{ V}$
 (1) $T_{amb} = -40 \text{ }^\circ\text{C}$
 (2) $T_{amb} = 25 \text{ }^\circ\text{C}$
 (3) $T_{amb} = 100 \text{ }^\circ\text{C}$

Fig 11. TR2 (PNP): On-state input voltage as a function of collector current; typical values



- $V_{CE} = -5 \text{ V}$
 (1) $T_{amb} = -40 \text{ }^\circ\text{C}$
 (2) $T_{amb} = 25 \text{ }^\circ\text{C}$
 (3) $T_{amb} = 100 \text{ }^\circ\text{C}$

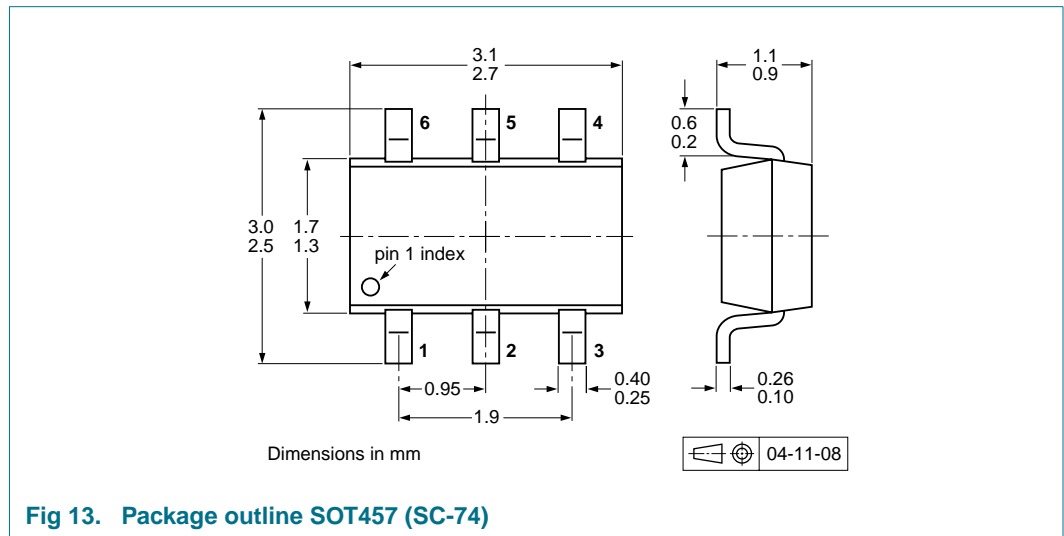
Fig 12. TR2 (PNP): Off-state input voltage as a function of collector current; typical values

8. Test information

8.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard *Q101 - Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

9. Package outline



10. Packing information

Table 8. Packing methods

The indicated -xxx are the last three digits of the 12NC ordering code.^[1]

Type number	Package	Description	Packing quantity	
			3000	10000
PIMC31	SOT457	4 mm pitch, 8 mm tape and reel; T1	[2] -115	-135
		4 mm pitch, 8 mm tape and reel; T2	[3] -125	-165

[1] For further information and the availability of packing methods, see [Section 14](#).

[2] T1: normal taping

[3] T2: reverse taping

11. Soldering

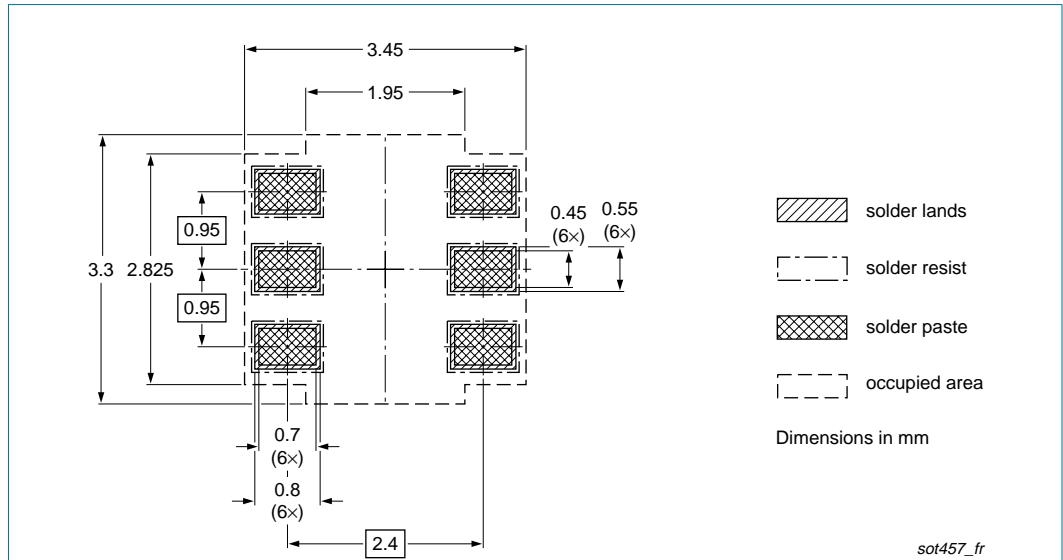


Fig 14. Reflow soldering footprint SOT457 (SC-74)

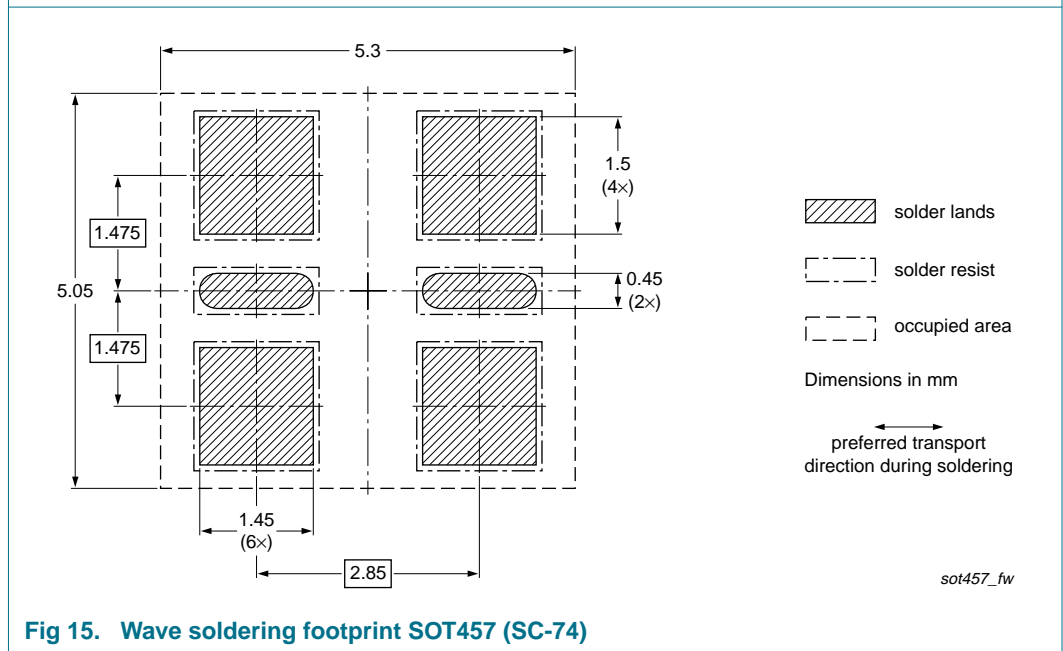


Fig 15. Wave soldering footprint SOT457 (SC-74)

12. Revision history

Table 9. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PIMC31_1	20090324	Product data sheet	-	-

13. Legal information

13.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

13.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

13.3 Disclaimers

General — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental

damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) may cause permanent damage to the device. Limiting values are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of this document is not implied. Exposure to limiting values for extended periods may affect device reliability.

Terms and conditions of sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, including those pertaining to warranty, intellectual property rights infringement and limitation of liability, unless explicitly otherwise agreed to in writing by NXP Semiconductors. In case of any inconsistency or conflict between information in this document and such terms and conditions, the latter will prevail.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Quick reference data — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from national authorities.

13.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

14. Contact information

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

15. Contents

1 Product profile 1

1.1 General description 1

1.2 Features 1

1.3 Applications 1

1.4 Quick reference data 1

2 Pinning information 2

3 Ordering information 2

4 Marking 2

5 Limiting values 2

6 Thermal characteristics 3

7 Characteristics 4

8 Test information 9

8.1 Quality information 9

9 Package outline 9

10 Packing information 9

11 Soldering 10

12 Revision history 11

13 Legal information 12

13.1 Data sheet status 12

13.2 Definitions 12

13.3 Disclaimers 12

13.4 Trademarks 12

14 Contact information 12

15 Contents 13

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.



© NXP B.V. 2009.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 24 March 2009

Document identifier: PIMC31_1