# PCS5P23Z05D
# PCS5P23Z09D

## Multiple Output Timing-Safe™ Peak EMI reduction IC

### General Features

- Input frequency range: 100MHz to 150MHz
- Clock distribution with Timing-Safe™ Peak EMI Reduction
- Zero input - output propagation delay
- Multiple low-skew outputs
- Output-output skew less than 250pS
- Device-device skew less than 700pS
- One input drives 9 outputs, grouped as 4 + 4 + 1(PCS5P23Z09D)
- One input drives 5 outputs (PCS5P23Z05D)
- Less than 200 pS cycle-to-cycle jitter is compatible with Pentium® based systems
- Available in 16pin 150-mil SOIC, 4.4 mm TSSOP (PCS5P23Z09D), and in 8pin 150-mil SOIC, 4.4mm TSSOP package (PCS5P23Z05D)
- 3.3V operation
- Advanced CMOS technology
- The First True Drop-in Solution

### Functional Description

PCS5P23Z05D/09D is a versatile, 3.3V zero-delay buffer designed to distribute high-speed Timing-Safe™ clocks with Peak EMI reduction. PCS5P23Z09D accepts one reference input and drives out nine low-skew clocks. It is available in a 16-pin package. The PCS5P23Z05D is the eight-pin version of the PCS5P23Z09D. It accepts one reference input and drives out five low-skew clocks.

All parts have on-chip PLLs that lock to an input clock on the REF pin. The PLL feedback is on-chip and is obtained from the CLKOUT pad.

The PCS5P23Z09D has two banks of four outputs each, which can be controlled by the Select inputs as shown in the Select Input Decoding Table. The select input also allows the input clock to be directly applied to the outputs for chip and system testing purposes.

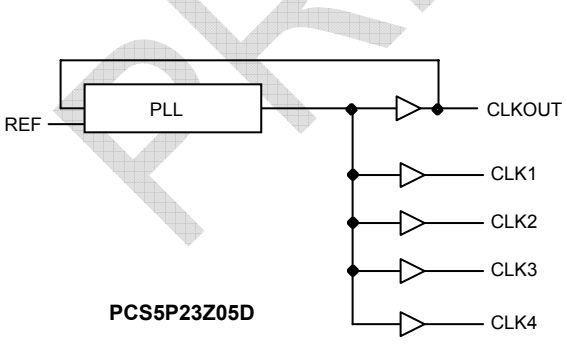
Multiple PCS5P23Z05D/09D devices can accept the same input clock and distribute it. In this case the skew between the outputs of the two devices is guaranteed to be less than 700pS.

All outputs have less than 200pS of cycle-to-cycle jitter. The input and output propagation delay is guaranteed to be less than ±350pS, and the output to output skew is guaranteed to be less than 250pS.

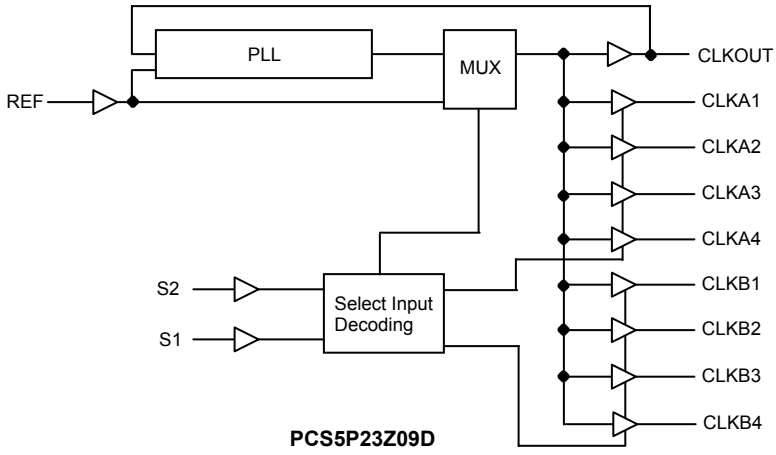
Refer "Spread Spectrum Control and Input-Output Skew Table" for deviations and Input-Output skew for PCS5P23Z05D and PCS5P23Z09D devices.

The PCS5P23Z05D/09D is available in two different packages, as shown in the ordering information table.

### Block Diagram




PCS5P23Z05D




PCS5P23Z09D



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### Select Input Decoding for PCS5P23Z09D

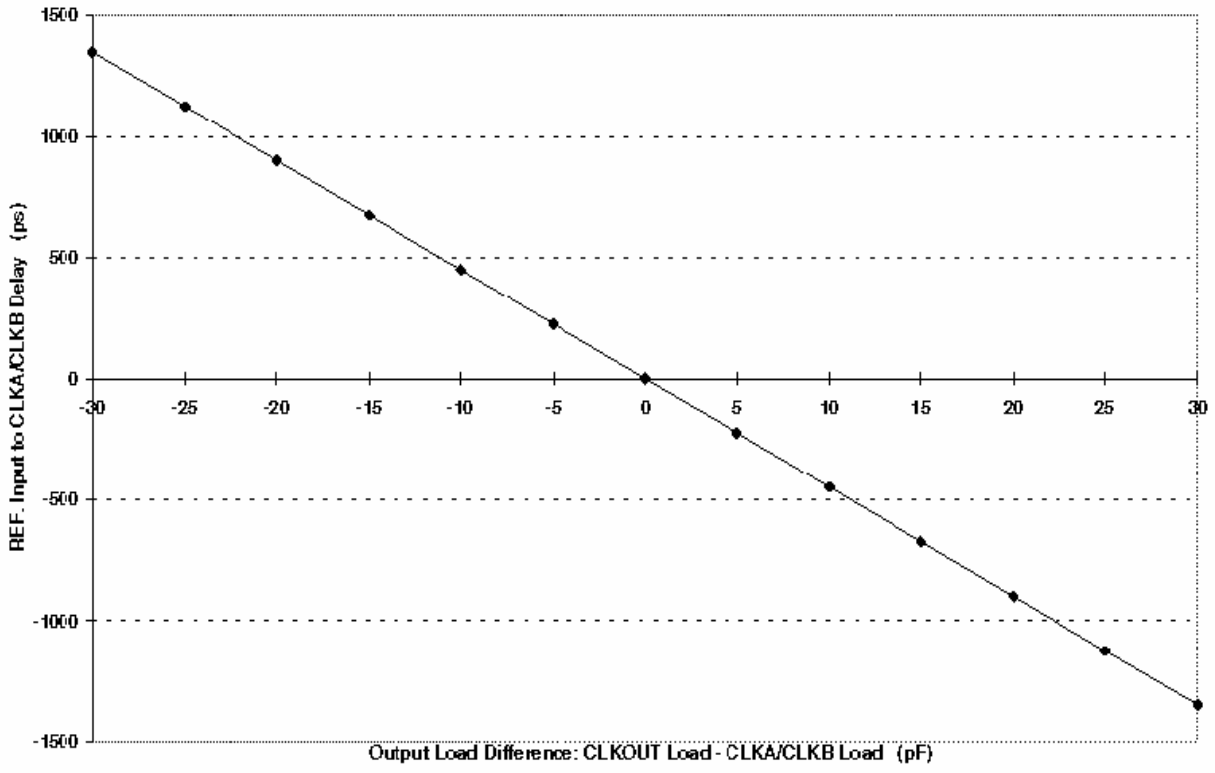
| S2 | S1 | Clock A1 - A4 | Clock B1 - B4 | CLKOUT[1] | Output Source | PLL Shut-Down |
|---|---|---|---|---|---|---|
| 0 | 0 | Three-state | Three-state | Driven | PLL | N |
| 0 | 1 | Driven | Three-state | Driven | PLL | N |
| 1 | 0 | Driven | Driven | Driven | Reference | Y |
| 1 | 1 | Driven | Driven | Driven | PLL | N |

Notes:1. This output is driven and has an internal feedback for the PLL. The load on this output can be adjusted to change the skew between the reference and the output.

### Zero Delay and Skew Control

All outputs should be uniformly loaded to achieve Zero Delay between input and output. Since the CLKOUT pin is the internal feedback to the PLL, its relative loading can adjust the input-output delay.

For applications requiring zero input-output delay, all outputs, including CLKOUT, must be equally loaded. Even if CLKOUT is not used, it must have a capacitive load equal to that on other outputs, for obtaining zero-input-output delay.



rev 0.2

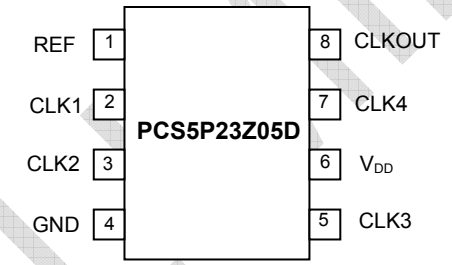
## Spread Spectrum Frequency Generation

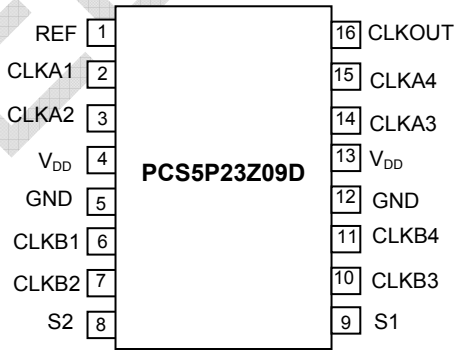
The clocks in digital systems are typically square waves with a 50% duty cycle and as frequencies increase the edge rates also get faster. Analysis shows that a square wave is composed of fundamental frequency and harmonics. The fundamental frequency and harmonics generate the energy peaks that become the source of EMI. Regulatory agencies test electronic equipment by measuring the amount of peak energy radiated from the equipment. In fact, the peak level allowed decreases as the frequency increases. The standard methods of reducing EMI are to use shielding, filtering, multi-layer PCBs etc. These methods are expensive. Spread spectrum clocking reduces the peak energy by reducing the Q factor of the clock. This is done by slowly modulating the clock frequency. The PCS5P23Z05D/09D uses the center modulation spread spectrum technique in which the modulated output frequency varies above and below the reference frequency with a specified modulation rate. With center modulation, the average frequency is same as the unmodulated frequency and there is no performance degradation

## Timing-Safe™ technology

Timing-Safe™ technology is the ability to modulate a clock source with Spread Spectrum technology and maintain synchronization with any associated data path.

## Pin Configuration



**rev0.2**

## Pin Description for PCS5P23Z05D

| Pin # | Pin Name | Description |
|---|---|---|
| 1 | REF | Input reference frequency, 5V-tolerant input |
| 2 | CLK1 [1] | Buffered clock output |
| 3 | CLK2[1] | Buffered clock output |
| 4 | GND | Ground |
| 5 | CLK3 [1] | Buffered clock output |
| 6 | $V_{DD}$ | 3.3V supply |
| 7 | CLK4[1] | Buffered clock output |
| 8 | CLKOUT[1,2] | Buffered clock output, internal feedback on this pin |

Notes: 1. Weak pull-down on these outputs.
2. This output is driven and has an internal feedback for the PLL.
3. Buffered clock outputs are Timing-Safe™

## Pin Description for PCS5P23Z09D

| Pin # | Pin Name | Description |
|---|---|---|
| 1 | REF | Input reference frequency, 5V tolerant input |
| 2 | CLKA1[1] | Buffered clock output, bank A |
| 3 | CLKA2[1] | Buffered clock output, bank A |
| 4 | $V_{DD}$ | 3.3V supply |
| 5 | GND | Ground |
| 6 | CLKB1[1] | Buffered clock output, bank B |
| 7 | CLKB2[1] | Buffered clock output, bank B |
| 8 | S2[2] | Select input, bit 2 |
| 9 | S1[2] | Select input, bit 1 |
| 10 | CLKB3[1] | Buffered clock output, bank B |
| 11 | CLKB4[1] | Buffered clock output, bank B |
| 12 | GND | Ground |
| 13 | $V_{DD}$ | 3.3V supply |
| 14 | CLKA3[1] | Buffered clock output, bank A |
| 15 | CLKA4[1] | Buffered clock output, bank A |
| 16 | CLKOUT[1,3] | Buffered output, internal feedback on this pin |

Notes: 1. Weak pull-down on these outputs.
2. Weak pull-up on these inputs.
3. This output is driven and has an internal feedback for the PLL.
4. Buffered clock outputs are Timing-Safe™

### Spread Spectrum Control and Input-Output Skew Table
(Note: The values given in the table are for an input frequency of 140MHz)

| Device | Deviation | Input-Output Skew($\pm T_{SKEW}$) |
|---|---|---|
| PCS5P23Z05D | ±0.125 % | 0.075 |
| PCS5P23Z09D | ±0.125 % | 0.075 |

Note: $T_{SKEW}$ is measured in units of the Clock Period

### Absolute Maximum Ratings

| Parameter | Min | Max | Unit |
|---|---|---|---|
| Supply Voltage to Ground Potential | -0.5 | 7 | V |
| DC Input Voltage (Except REF) | -0.5 | $V_{DD}$ + 0.5 | V |
| DC Input Voltage (REF) | -0.5 | 7 | V |
| Storage Temperature | -65 | +150 | °C |
| Max. Soldering Temperature (10 sec) | | 260 | °C |
| Junction Temperature | | 150 | °C |
| Static Discharge Voltage (As per JEDEC STD22- A114-B) | | 2 | KV |
| Note: These are stress ratings only and functional usage is not implied. Exposure to absolute maximum ratings for prolonged periods can affect device reliability. | | | |

### Operating Conditions for PCS5P23Z05D and PCS5P23Z09D

| Parameter | Description | Min | Max | Unit |
|---|---|---|---|---|
| $V_{DD}$ | Supply Voltage | 3.0 | 3.6 | V |
| $T_A$ | Operating Temperature (Ambient Temperature) | 0 | 70 | °C |
| $C_L$ | Load Capacitance | | 10 | pF |
| $C_{IN}$ | Input Capacitance | | 7 | pF |

### Electrical Characteristics for PCS5P23Z05D and PCS5P23Z09D

| Parameter | Description | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IL}$ | Input LOW Voltage[1] | | | | 0.8 | V |
| $V_{IH}$ | Input HIGH Voltage[1] | | 2.0 | | | V |
| $I_{IL}$ | Input LOW Current | $V_{IN}$ = 0V | | | 50 | µA |
| $I_{IH}$ | Input HIGH Current | $V_{IN}$ = $V_{DD}$ | | | 100 | µA |
| $V_{OL}$ | Output LOW Voltage[2] | $I_{OL}$ = 8mA | | | 0.4 | V |
| $V_{OH}$ | Output HIGH Voltage[2] | $I_{OH}$ = -8mA | 2.4 | | | V |
| $I_{DD}$ | Supply Current | Unloaded outputs at 150MHz | | | 60 | mA |
| $Z_o$ | Output Impedance | | | 23 | | Ω |

Notes:
1. REF input has a threshold voltage of VDD/2
2. Parameter is guaranteed by design and characterization. Not 100% tested in production

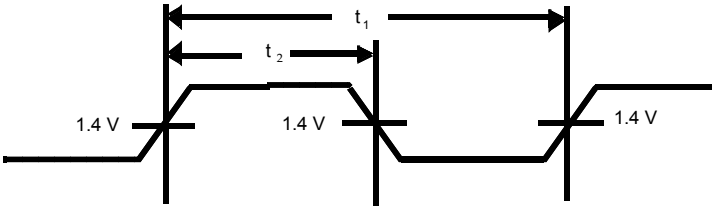
### Switching Characteristics for PCS5P23Z05D and PCS5P23Z09D

| Parameter | Description | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $1/t_1$ | Output Frequency | 10pF load | 100 | | 150 | MHz |
| | Duty Cycle[2] = ($t_2$ / $t_1$) * 100 | Measured at 1.4V | 40 | 50 | 60 | % |
| $t_3$ | Output Rise Time[1,2] | Measured between 0.8V and 2.0V | | | 2.50 | nS |
| $t_4$ | Output Fall Time [1,2] | Measured between 2.0V and 0.8V | | | 2.50 | nS |
| $t_5$ | Output-to-output skew [2] | All outputs equally loaded | | | 250 | pS |
| $t_6$ | Delay, REF Rising Edge to CLKOUT Rising Edge [2] | Measured at $V_{DD}$ /2 | | 0 | ±350 | pS |
| $t_7$ | Device-to-Device Skew [2] | Measured at $V_{DD}$/2 on the CLKOUT pins of the device | | 0 | 700 | pS |
| $t_J$ | Cycle-to-cycle jitter [2] | Measured at 100MHz, loaded outputs | | | 200 | pS |
| $t_{LOCK}$ | PLL Lock Time [2] | Stable power supply, valid clock presented on REF pin | | | 1.0 | mS |

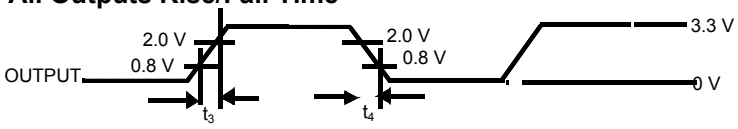
Notes:
1. All parameters specified with loaded outputs.
2. Parameter is guaranteed by design and characterization. Not 100% tested in production

## Switching Waveforms

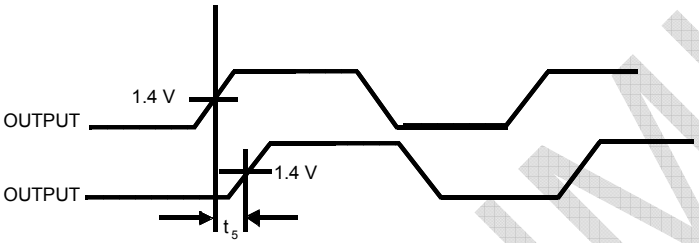
### Duty Cycle Timing



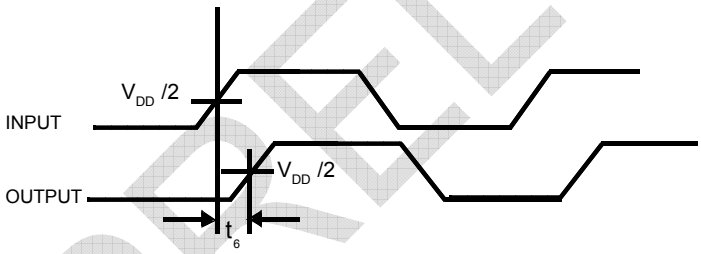

### All Outputs Rise/Fall Time



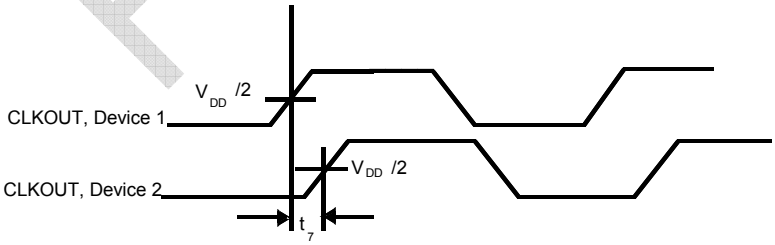

### Output - Output Skew



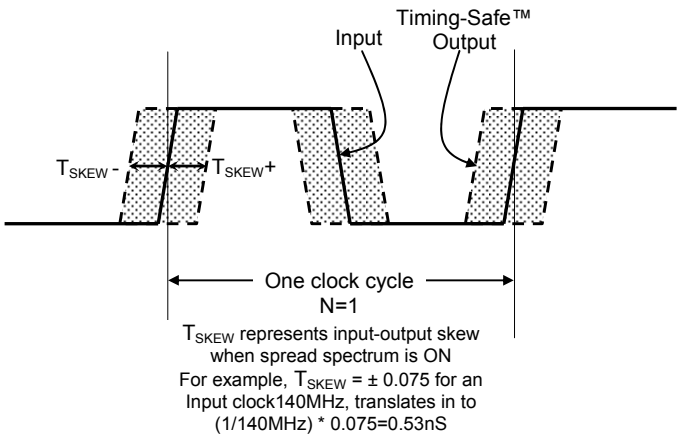

### Input - Output Propagation Delay




### Device - Device Skew

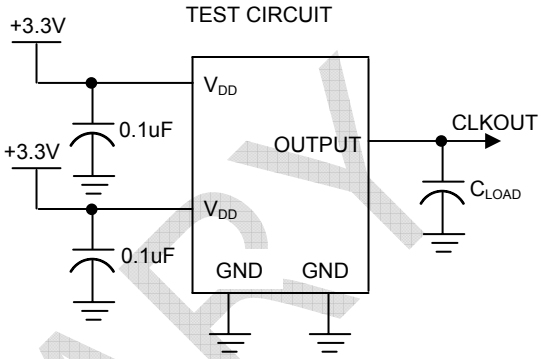


### Input-Output Skew

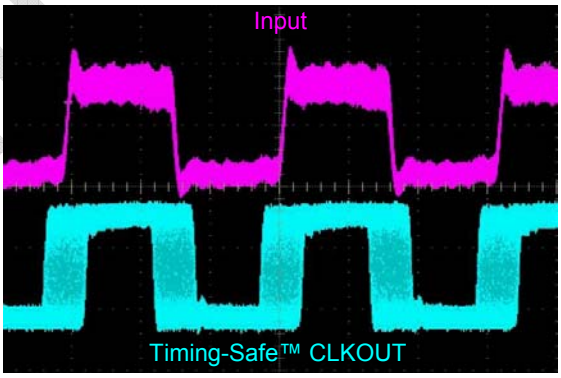



$T_{SKEW}$ represents input-output skew when spread spectrum is ON
For example, $T_{SKEW}$ = ± 0.075 for an Input clock140MHz, translates in to (1/140MHz) * 0.075=0.53nS

### Test Circuit

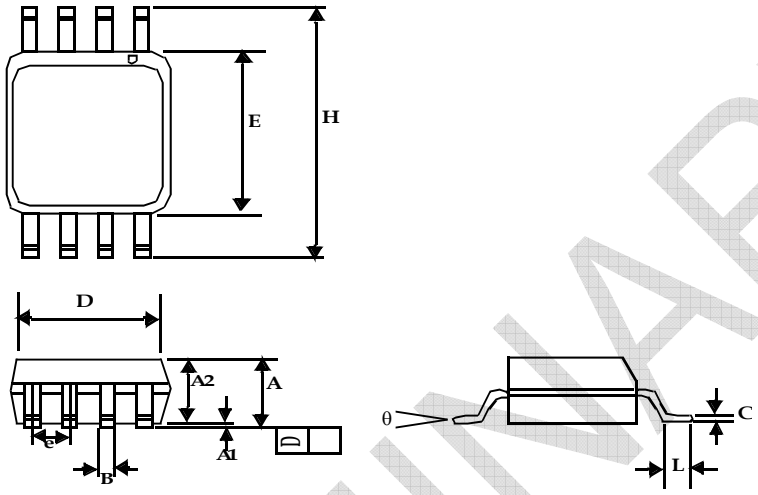



### A Typical example of Timing-Safe™ waveform

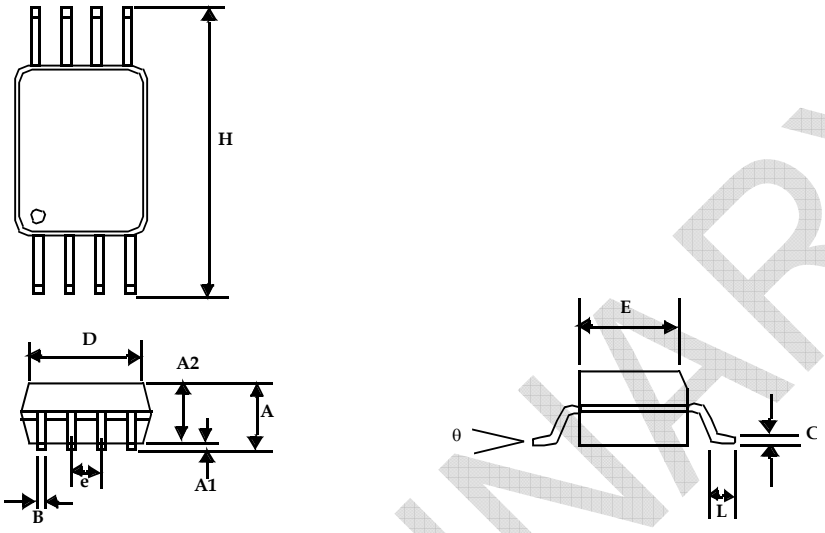
## Package Information

### 8-lead (150-mil) SOIC Package



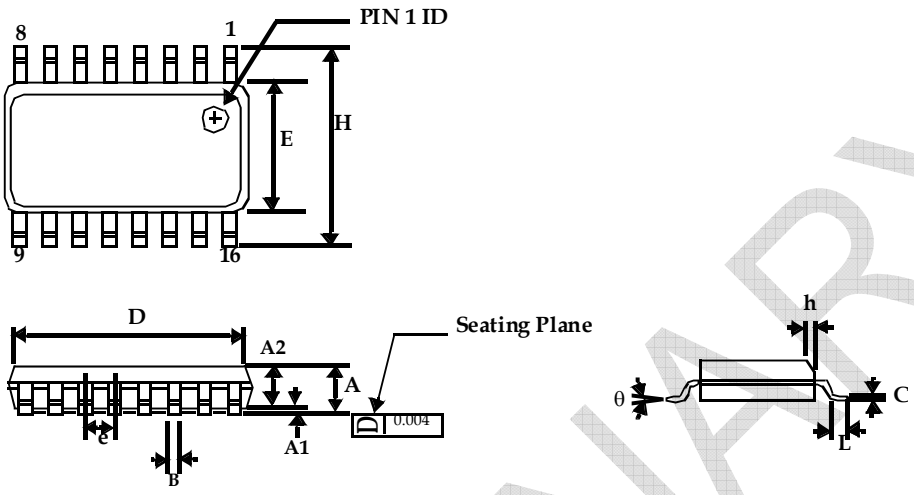

| Symbol | Dimensions | | | |
|---|---|---|---|---|
| | Inches | | Millimeters | |
| | Min | Max | Min | Max |
| A1 | 0.004 | 0.010 | 0.10 | 0.25 |
| A | 0.053 | 0.069 | 1.35 | 1.75 |
| A2 | 0.049 | 0.059 | 1.25 | 1.50 |
| B | 0.012 | 0.020 | 0.31 | 0.51 |
| C | 0.007 | 0.010 | 0.18 | 0.25 |
| D | 0.193 BSC | | 4.90 BSC | |
| E | 0.154 BSC | | 3.91 BSC | |
| e | 0.050 BSC | | 1.27 BSC | |
| H | 0.236 BSC | | 6.00 BSC | |
| L | 0.016 | 0.050 | 0.41 | 1.27 |
| θ | 0° | 8° | 0° | 8° |

## 8-lead TSSOP Package (4.40-MM Body)



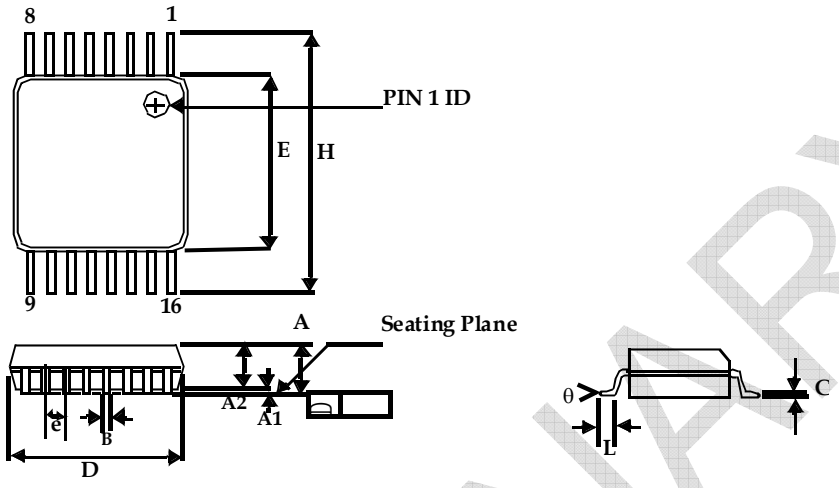

| Symbol | Dimensions | | | |
|---|---|---|---|---|
| | Inches | | Millimeters | |
| | Min | Max | Min | Max |
| A | | 0.043 | | 1.10 |
| A1 | 0.002 | 0.006 | 0.05 | 0.15 |
| A2 | 0.033 | 0.037 | 0.85 | 0.95 |
| B | 0.008 | 0.012 | 0.19 | 0.30 |
| c | 0.004 | 0.008 | 0.09 | 0.20 |
| D | 0.114 | 0.122 | 2.90 | 3.10 |
| E | 0.169 | 0.177 | 4.30 | 4.50 |
| e | 0.026 BSC | | 0.65 BSC | |
| H | 0.252 BSC | | 6.40 BSC | |
| L | 0.020 | 0.028 | 0.50 | 0.70 |
| θ | 0° | 8° | 0° | 8° |

## 16-lead (150 Mil) Molded SOIC Package




| Symbol | Dimensions | | | |
|---|---|---|---|---|
| | Inches | | Millimeters | |
| | Min | Max | Min | Max |
| A | 0.053 | 0.069 | 1.35 | 1.75 |
| A1 | 0.004 | 0.010 | 0.10 | 0.25 |
| A2 | 0.049 | 0.059 | 1.25 | 1.50 |
| B | 0.013 | 0.022 | 0.33 | 0.53 |
| C | 0.008 | 0.012 | 0.19 | 0.27 |
| D | 0.386 | 0.394 | 9.80 | 10.01 |
| E | 0.150 | 0.157 | 3.80 | 4.00 |
| e | 0.050 BSC | | 1.27 BSC | |
| H | 0.228 | 0.244 | 5.80 | 6.20 |
| h | 0.010 | 0.016 | 0.25 | 0.41 |
| L | 0.016 | 0.035 | 0.40 | 0.89 |
| θ | 0° | 8° | 0° | 8° |

## 16-lead TSSOP Package (4.40-MM Body)

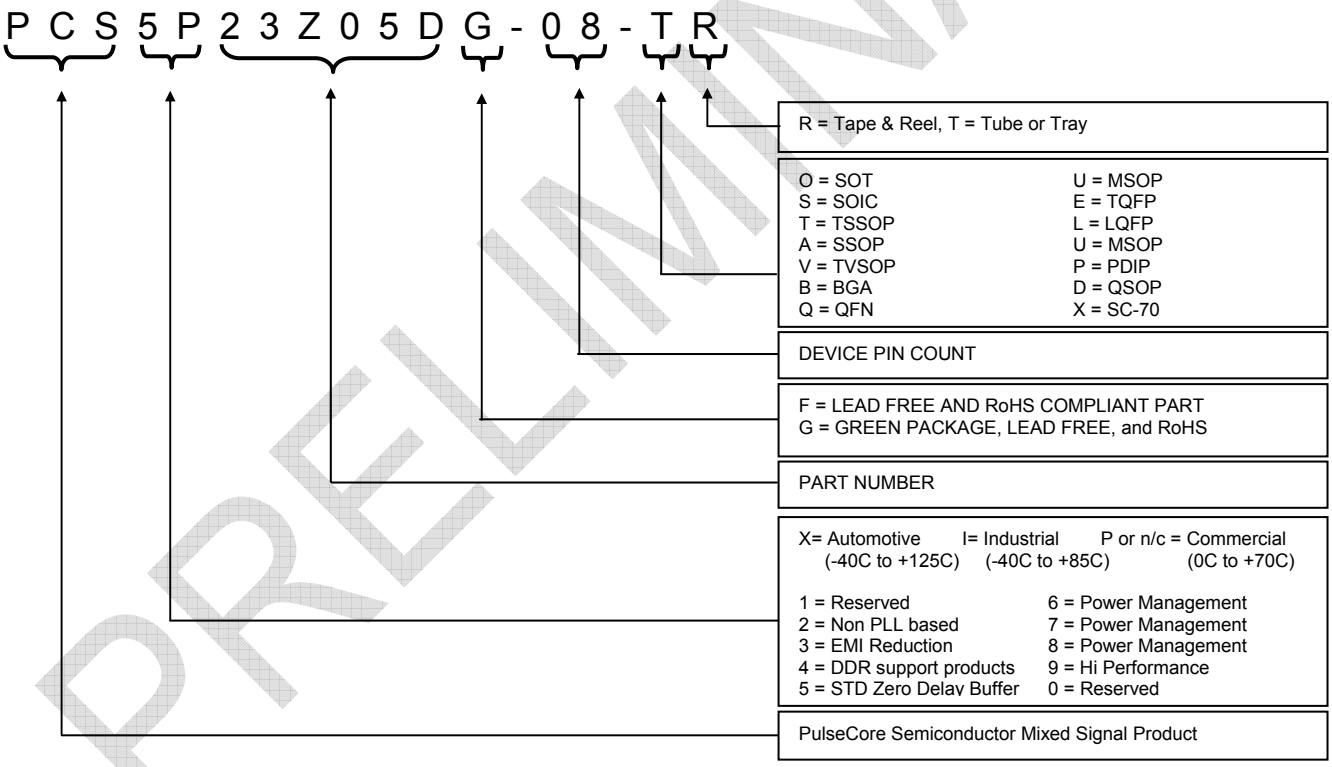



| Symbol | Dimensions | | | |
|---|---|---|---|---|
| | Inches | | Millimeters | |
| | Min | Max | Min | Max |
| A | | 0.043 | | 1.20 |
| A1 | 0.002 | 0.006 | 0.05 | 0.15 |
| A2 | 0.031 | 0.041 | 0.80 | 1.05 |
| B | 0.007 | 0.012 | 0.19 | 0.30 |
| C | 0.004 | 0.008 | 0.09 | 0.20 |
| D | 0.193 | 0.201 | 4.90 | 5.10 |
| E | 0.169 | 0.177 | 4.30 | 4.50 |
| e | 0.026 BSC | | 0.65 BSC | |
| H | 0.252 BSC | | 6.40 BSC | |
| L | 0.020 | 0.030 | 0.50 | 0.75 |
| θ | 0° | 8° | 0° | 8° |

## Ordering Codes

| Ordering Code | Marking | Package Type | Tempeature |
|---|---|---|---|
| PCS5P23Z05DG-08-ST | 5P23Z05DG | 8-pin 150-mil SOIC-TUBE | Commercial |
| PCS5P23Z05DG-08-SR | 5P23Z05DG | 8-pin 150-mil SOIC-TAPE & REEL | Commercial |
| PCS5P23Z05DG-08-TT | 5P23Z05DG | 8-pin 4.4-mm TSSOP - TUBE | Commercial |
| PCS5P23Z05DG-08-TR | 5P23Z05DG | 8-pin 4.4-mm TSSOP - TAPE & REEL | Commercial |
| PCS5P23Z09DG-16-ST | 5P23Z09DG | 16-pin 150-mil SOIC-TUBE | Commercial |
| PCS5P23Z09DG-16-SR | 5P23Z09DG | 16-pin 150-mil SOIC-TAPE & REEL | Commercial |
| PCS5P23Z09DG-16-TT | 5P23Z09DG | 16-pin 4.4-mm TSSOP - TUBE | Commercial |
| PCS5P23Z09DG-16-TR | 5P23Z09DG | 16-pin 4.4-mm TSSOP - TAPE & REEL | Commercial |

## Device Ordering Information



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Part Number: PCS5P23Z05D
PCS5P23Z09D
Document Version: 0.1

Note: This product utilizes US Patent # 6,646,463 Impedance Emulator Patent issued to PulseCore Semiconductor, dated 11-11-2003
Timing-Safe™ US Patent Pending.