

STRUCTURE	Silicon Monolithic Integrated Circuit
PRODUCT SERIES	Single-Phase Full-Wave Motor Driver for Fan Motor
TYPE	B D 6 7 2 1 F S
FEATURES	Speed controllable by DC / PWM input Current limit circuit PWM soft switching drive

○ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Limit	Unit
Supply voltage	V _{cc}	20	V
Power dissipation	P _d	812.5*	mW
Operating temperature	T _{opr}	-40~+100	°C
Storage temperature	T _{stg}	-55~+150	°C
Output current	I _{omax}	1.0* *	A
FG signal output current	I _{FG}	10	mA
FG signal output voltage	V _{FG}	20	V
AL signal output current	I _{AL}	10	mA
AL signal output voltage	V _{AL}	20	V
VREF current ability	I _{VREF}	8	mA
Junction temperature	T _{jmax}	150	°C

* Reduce by 6.5mW/°C over Ta=25°C.
(On 70.0mm×70.0mm×1.6mm glass epoxy board)

* * This value is not to exceed P_d.

○OPERATING CONDITIONS

Parameter	Symbol	Limit	Unit
Operating supply voltage range	V _{cc}	4.5~17.0	V
Hall input voltage range	V _H	0~V _{cc} -2.0	V
VTH input voltage range	V _{VTH}	0~V _{cc} -2.0	V
VMIN input voltage range	V _{VMIN}	0~V _{cc} -2.0	V

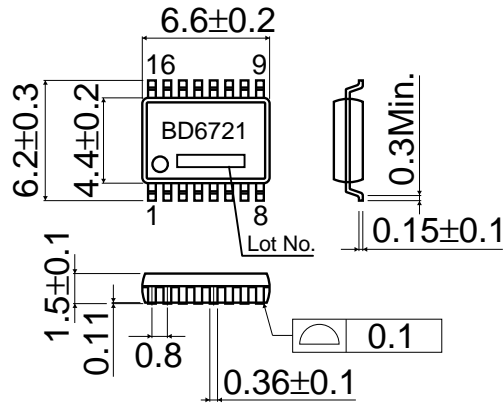
* This product is not designed for production against radioactive rays.

* This document may be strategic data subject to COCOM regulations.

○ ELECTRICAL CHARACTERISTICS (Unless otherwise specified Ta=25°C, Vcc=12V)

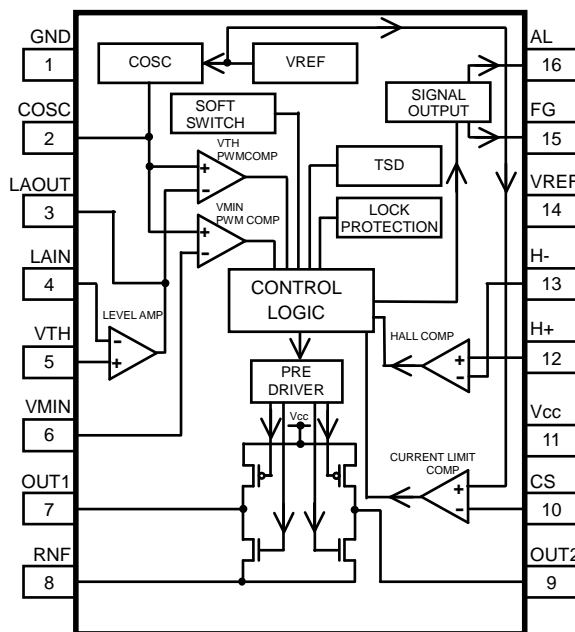
Parameter	Symbol	Limit			Unit	Conditions
		Min.	Typ.	Max.		
Circuit current	I _{CC}	4.0	7.0	10.0	mA	
Hall input hysteresis	V _{HYS}	±5	±10	±15	mV	
Output voltage	V _O	-	0.6	0.9	V	I _o =300mA Upper and Lower total
Lock detection ON time	T _{ON}	0.3	0.5	0.7	s	
Lock detection OFF time	T _{OFF}	3.0	5.0	7.0	s	
FG output low voltage	V _{FGL}	-	0.15	0.3	V	I _{FG} =5mA
FG output leak current	I _{FGL}	-	-	50	μA	V _{FG} =17V
AL output low voltage	V _{ALL}	-	0.15	0.3	V	I _{AL} =5mA
AL output leak current	I _{ALL}	-	-	50	μA	V _{AL} =17V
OSC low voltage	V _{OSCL}	0.8	1.0	1.2	V	
OSC high voltage	V _{OSCH}	2.3	2.5	2.7	V	
OSC charge current	I _{CO}	-50	-32	-26	μA	
OSC discharge current	I _{DOS}	26	32	50	μA	
Level amp gain	G _{LA}	50	-	-	dB	
Level amp output low voltage	V _{LAOL}	-	0.2	0.3	V	
Level amp output high voltage	V _{LAOH}	-	1.6	2.0	V	Voltage between LAOUT and Vcc
Output ON duty 1	DUTY1	85	90	95	%	V _{TH} =V _{REF} *0.383 OUT=Pull down 1kΩ C _{OSC} =470pF
Output ON duty 2	DUTY2	45	50	55	%	V _{TH} =V _{REF} *0.583 OUT=Pull down 1kΩ C _{OSC} =470pF
Output ON duty 3	DUTY3	5	10	15	%	V _{TH} =V _{REF} *0.783 OUT=Pull down 1kΩ C _{OSC} =470pF
VREF voltage	V _{REF}	2.8	3.0	3.2	V	I _{VREF} =-2mA
Current limit voltage	V _{CL}	290	310	330	mV	
VTH bias current	I _{VTH}	-	-	0.2	μA	
VMIN bias current	I _{VMIN}	-	-	0.2	μA	

PACKAGE OUTLINES



SSOP-A16 (UNIT:mm)

BLOCK DIAGRAM



TERMINAL NAME

PIN No.	Terminal name
1	GND
2	COSC
3	LAOUT
4	LAIN
5	VTH
6	VMIN
7	OUT1
8	RNF
9	OUT2
10	CS
11	VCC
12	H+
13	H-
14	VREF
15	FG
16	AL

CAUTIONS ON USE

1) Absolute maximum ratings

An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down the devices, thus making impossible to identify breaking mode, such as a short circuit or an open circuit. If any over rated values will expect to exceed the absolute maximum ratings, consider adding circuit protection devices, such as fuses.

2) Connecting the power supply connector backward

Connecting of the power supply in reverse polarity can damage IC. Take precautions when connecting the power supply lines. An external direction diode can be added.

3) Power supply line

Back electromotive force causes regenerated current to power supply line, therefore take a measure such as placing a capacitor between power supply and GND for routing regenerated current. And fully ensure that the capacitor characteristics have no problem before determine a capacitor value. (when applying electrolytic capacitors, capacitance characteristic values are reduced at low temperatures)

4) GND potential

The potential of GND pin must be minimum potential in all operating conditions. Also ensure that all terminals except GND terminal do not fall below GND voltage including transient characteristics. However, it is possible that the motor output terminal may deflect below GND because of influence by back electromotive force of motor. Malfunction may possibly occur depending on use condition, environment, and property of individual motor. Please make fully confirmation that no problem is found on operation of IC.

5) Thermal design

Use a thermal design that allows for a sufficient margin in light of the power dissipation(Pd) in actual operating conditions.

6) Inter-pin shorts and mounting errors

Use caution when positioning the IC for mounting on printed circuit boards. The IC may be damaged if there is any connection error or if pins are shorted together.

7) Actions in strong electromagnetic field

Use caution when using the IC in the presence of a strong electromagnetic field as doing so may cause the IC to malfunction.

8) ASO

When using the IC, set the output transistor so that it does not exceed absolute maximum ratings or ASO.

9) Thermal shut down circuit

The IC incorporates a built-in thermal shutdown circuit (TSD circuit). Operation temperature is 175°C(typ.) and has a hysteresis width of 25°C(typ.). When IC chip temperature rises and TSD circuit works, the output terminal becomes an open state. TSD circuit is designed only to shut the IC off to prevent thermal runaway. It is not designed to protect the IC or guarantee its operation. Do not continue to use the IC after operation this circuit or use the IC in an environment where the operation of this circuit is assumed.

10) Testing on application boards

When testing the IC on an application board, connecting a capacitor to a pin with low impedance subjects the IC to stress. Always discharge capacitors after each process or step. Always turn the IC's power supply off before connecting it to or removing it from a jig or fixture during the inspection process. Ground the IC during assembly steps as an antistatic measure. Use similar precaution when transporting or storing the IC.

11) GND wiring pattern

When using both small signal and large current GND patterns, it is recommended to isolate the two ground patterns, placing a single ground point at the ground potential of application so that the pattern wiring resistance and voltage variations caused by large currents do not cause variations in the small signal ground voltage. Be careful not to change the GND wiring pattern of any external components, either.

12) Capacitor between output and GND

When a large capacitor is connected between output and GND, if Vcc is shorted with 0V or GND for some cause, it is possible that the current charged in the capacitor may flow into the output resulting in destruction. Keep the capacitor between output and GND below 100uF.

13) IC terminal input

When Vcc voltage is not applied to IC, do not apply voltage to each input terminal. When voltage above Vcc or below GND is applied to the input terminal, parasitic element is actuated due to the structure of IC. Operation of parasitic element causes mutual interference between circuits, resulting in malfunction as well as destruction in the last. Do not use in a manner where parasitic element is actuated.

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