8-Channel, I²C, 12-Bit SAR ADC with Temperature Sensor

Preliminary Technical Data

AD7291

FEATURES

12 bit SAR ADC
- **8 single-ended inputs**
- **Channel sequencer functionality**
- **Analog Input Range 0 to 2.5V**

12-bit temperature-to-digital converter
- **Temperature sensor accuracy of ±2°C typical**

Temperature range: –40°C to +125°C
Specified for V_{DD} of 2.8 V to 3.6V
Logic Voltage V_{DRIVE} = 1.65V to 3.6V
Power-down current : <10 µA
Internal 2.5V Reference
I²C-compatible serial interface supports
- **standard & fast modes**

20-lead LFCSP

Functional Block Diagram

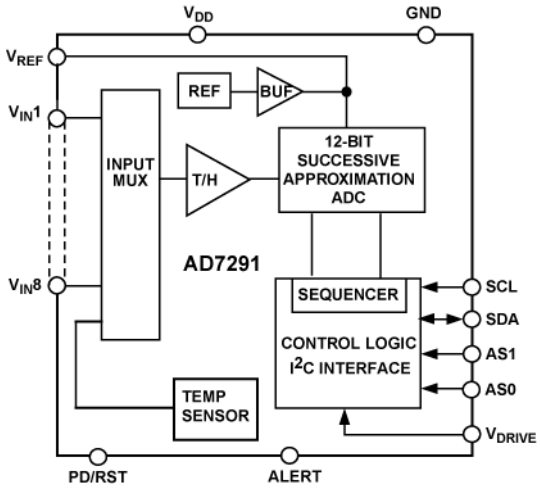

Figure 1.

GENERAL DESCRIPTION

The AD7291 is a 12-bit, high speed, low power, 8-channel, successive approximation ADC with an internal temperature sensor. The part operates from a single 3.3V power supply and features an I²C®-compatible interface. The track-and-hold amplifier which can handle input frequencies of up to 70MHz, and a multiplexer allows samples from eight channels.

Each AD7291 provides a 2-wire serial interface compatible with I²C interfaces. The AD7291 offers a programmable sequencer, which enables the selection of a pre-programmable sequence of channels for conversion. The device has an on-chip 2.5 V reference that can be disabled to allow the use of an external reference.

The AD7291 includes a high accuracy band-gap temperature sensor, which is monitored and digitized by the12-bit ADC to give a resolution of 0.25°C. The AD7291 uses advanced design techniques to achieve very low power dissipation at high throughput rates. The part also offers flexible power/throughput rate management options and is offered in a 20 lead LFCSP package

PRODUCT HIGHLIGHTS

1. Ideally suited to monitoring system variables in a variety of systems including telecommunications, process and industrial control
2. I²C-compatible serial interface. Standard and fast modes.
3. Eight Single-Ended Inputs with a Channel Sequencer. A consecutive sequence of channels can be selected on which the ADC cycles and converts.
4. Integrated temperature sensor with 0.25°C resolution.

Table 1. AD7298 and Related Products

Device	Resolution	Interface	Features
AD7298	12-Bit	SPI	8 Channel ADC & Temp Sensor
AD7291	12-Bit	I²C	8 Channel ADC & Temp Sensor

Rev. PrC

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SPECIFICATIONS

AD7291 SPECIFICATIONS

V_{DD} = 2.8V to 3.6V; V_{DRIVE} = 1.65 V to 3.6 V; f_{SCLK} = 400KHz, fast SCLK mode; V_{REF} = 2.5 V internal/external; T_A = −40°C to +125°C, unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE					f_{IN} = 10 kHz sine wave
Signal-to-Noise Ratio (SNR)[1]	70	71		dB	
Signal-to-Noise (+ Distortion) Ratio (SINAD)[1]	70	71		dB	
Total Harmonic Distortion (THD)[1]		−84	78	dB	
Spurious-Free Dynamic Range (SFDR)[1]		−85	80	dB	
Intermodulation Distortion (IMD)[1]					f_A = 5.4 kHz, f_B = 4.6 kHz
Second-Order Terms		−88		dB	
Third-Order Terms		−88		dB	
Channel-to-Channel Isolation[1]		−100		dB	
Full Power Bandwidth[2]		TBD		MHz	@ 3 dB
		TBD		MHz	@ 0.1 dB
DC ACCURACY					
Resolution	12			Bits	
Integral Nonlinearity (INL)[1]		±0.5	±1	LSB	
Differential Nonlinearity (DNL)[1]		±0.5	±0.99	LSB	Guaranteed no missed codes to 12 bits
Offset Error		±1	±6	LSB	
Offset Error Matching		±0.5	±1	LSB	
Offset Temperature Drift		4		ppm/°C	
Gain Error		±1	±2	LSB	
Gain Error Matching		±0.5	±1	LSB	
Gain Temperature Drift		0.5		ppm/°C	
ANALOG INPUT					
Input Voltage Ranges	0		V_{REF}	V	
DC Leakage Current		±0.01	±1	µA	
Input Capacitance[2]		32		pF	During Acquisition Outside Acquisition
Input Impedance[2]		TBD		kΩ	
REFERENCE INPUT/OUTPUT					
Reference Output Voltage[3]	2.4875	2.5	2.5125	V	±0.5% maximum @ 25°C
Long-Term Stability		150		ppm	For 1000 hours
Output Voltage Hysteresis[1]		50		ppm	
Reference Input Voltage Range[4]	2.0		2.5	V	
DC Leakage Current		±0.01	±1	µA	External reference applied to Pin V_{REF}
Input Capacitance		TBD		pF	
V_{REF} Output Impedance		TBD		Ω	
Reference Temperature Coefficient		6	25	ppm/°C	
V_{REF} Noise[2]		60		µV rms	Bandwidth = TBD kHz

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LOGIC INPUTS (SDA, SCL)					
Input High Voltage, V_{INH}	$0.7 \times V_{DRIVE}$			V	
Input Low Voltage, V_{INL}			+0.3 x V_{DRIVE}	V	
Input Current, I_{IN}		±0.01	±1	µA	V_{IN} = 0 V or V_{DRIVE}
Input Capacitance, C_{IN}[2]		3		pF	
Input Hysteresis, V_{HYST}	0.1 (V_{DRIVE})			V	
LOGIC OUTPUTS (OPEN DRAIN)					
Output Low Voltage, V_{OL}			0.4	V	I_{SINK} = 3 mA
			0.6	V	I_{SINK} = 6 mA
Floating State Leakage Current		±0.01	±1	µA	
Floating State Output Capacitance[2]		8		pF	
Output Coding	Straight (natural) binary				
TEMPERATURE SENSOR—INTERNAL					
Operating Range	−40		+125		
Accuracy		±1	±2	°C	T_A = −40°C to +85°C
		±1	±3	°C	T_A = >85°C to 125°C
Resolution		0.25		°C	LSB size
CONVERSION RATE					
Conversion Time		3		µs	
Autocycle Update Rate		TBD			
Throughput Rate			22.22	kSPS	F_{SCL} = 400kHz
POWER REQUIREMENTS					Digital inputs = 0 V or V_{DRIVE}
V_{DD}	2.8	3	3.6	V	See
V_{DRIVE}	1.65	3	3.6	V	
I_{TOTAL}[5]					V_{DD} = 3.3V
ADC Operating, Interface Active (Fully Operational)			5	mA	
Full Power-Down Mode		5	60	µA	
Power Dissipation					V_{DD} = 3.3V
ADC Operating, Interface Active (Fully Operational)			16.5	mW	
Full Power-Down Mode			1.65	µW	

[1] See the Terminology Section.
[2] Sample tested during initial release to ensure compliance.
[3] Refers to Pin V_{REF} specified for 25°C.
[4] V_{REF} variations from 2.5V will alter the gain error of the temperature sensor, °C per LSB, and a correction factor may be required, See Section X.
[5] I_{TOTAL} is the total current flowing in V_{DD} and V_{DRIVE}.

I²C TIMING SPECIFICATIONS

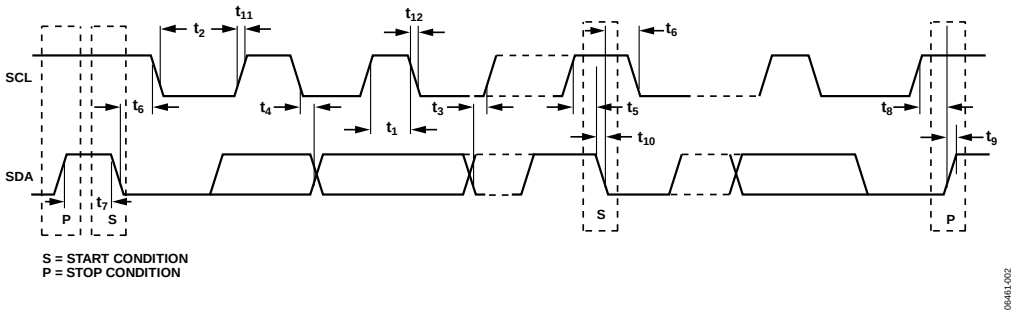


Figure 2. 2-Wire Serial Interface Timing Diagram

All values were measured with the input filtering enabled. C_B refers to the capacitive load on the bus line, with tr and tf measured between 0.3 V_{DRIVE} and 0.7 V_{DRIVE} (see *Figure 2*) Unless otherwise noted, V_{DD} = 2.8V to 3.6V; V_{DRIVE} = 1.65 V to 3.6 V; V_{REF} = 2.5 V internal/external; T_A = −40°C to + 125°C, unless otherwise noted.

Table 3.

Parameter	Conditions	Limit at t_{MIN}, t_{MAX} Min	Typ	Max	Unit	Description
f_{SCL}	Standard mode			100	kHz	Serial clock frequency
	Fast mode			400	kHz	
t_1	Standard mode	4			µs	t_{HIGH}, SCL high time
	Fast mode	0.6			µs	
t_2	Standard mode	4.7			µs	t_{LOW}, SCL low time
	Fast mode	1.3			µs	
t_3	Standard mode	250			ns	$t_{SU;DAT}$, data setup time
	Fast mode	100			ns	
t_4[1]	Standard mode	0		3.45	µs	$t_{HD;DAT}$, data hold time
	Fast mode	0		0.9	µs	
t_5	Standard mode	4.7			µs	$t_{SU;STA}$, setup time for a repeated start condition
	Fast mode	0.6			µs	
t_6	Standard mode	4			µs	$t_{HD;STA}$, hold time for a repeated start condition
	Fast mode	0.6			µs	
t_7	Standard mode	4.7			µs	t_{BUF}, bus-free time between a stop and a start condition
	Fast mode	1.3			µs	
t_8	Standard mode	4			µs	$t_{SU;STO}$, setup time for a stop condition
	Fast mode	0.6			µs	
t_9	Standard mode			1000	ns	t_{RDA}, rise time of the SDA signal
	Fast mode	20 + 0.1 C_B		300	ns	
t_{10}	Standard mode			300	ns	t_{FDA}, fall time of the SDA signal
	Fast mode	20 + 0.1 C_B		300	ns	
t_{11}	Standard mode			1000	ns	t_{RCL}, rise time of the SCL signal
	Fast mode	20 + 0.1 C_B		300	ns	
t_{11A}	Standard mode			1000	ns	t_{RCL1}, rise time of the SCL signal after a repeated
	Fast mode	20 + 0.1 C_B		300	ns	start condition and after an acknowledge bit
t_{12}	Standard mode			300	ns	t_{FCL}, fall time of the SCL signal
	Fast mode	20 + 0.1 C_B		300	ns	
t_{SP}	Fast mode	0		50	ns	Pulse width of the suppressed spike
$t_{POWER-UP}$			0.6		µs	Power-up and acquisition time

[1] A device must provide a data hold time for SDA in order to bridge the undefined region of the SCL falling edge.

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
V_{DD} to AGND, DGND,	−0.3 V to +5 V
V_{DRIVE} to AGND, DGND,	−0.3 V to + 5 V
Analog Input Voltage to AGND	−0.3 V to 3V
Digital Input Voltage to AGND	−0.3 V to V_{DRIVE} + 0.3 V
Digital Output Voltage to AGND	−0.3 V to V_{DRIVE} + 0.3 V
V_{REF} to AGND	−0.3 V to +3V
AGND to DGND	−0.3 V to +0.3V
Input Current to Any Pin Except Supplies[1]	±10 mA
Operating Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
LFCSP Package	
θ_{JA} Thermal Impedance	TBD°C/W
θ_{JC} Thermal Impedance	TBD°C/W
Pb-free Temperature, Soldering	
Reflow	260(+0)°C
ESD	2 kV

[1] Transient currents of up to 100 mA do not cause latch-up.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

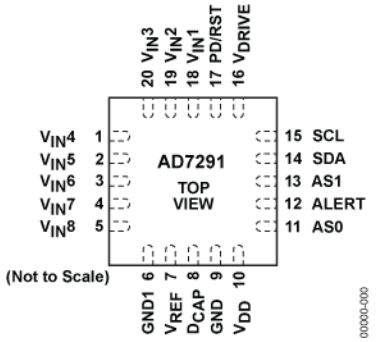


Figure 3. Pin Configuration

Note: The exposed metal paddle on the bottom of the LFCSP package should be soldered to PCB ground for proper heat dissipation and performance.

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1-5, 18,19, 20	$V_{IN}1$, $V_{IN}2$, $V_{IN}3$, $V_{IN}4$, $V_{IN}5$, $V_{IN}6$ $V_{IN}7$, $V_{IN}8$	Analog Inputs. The AD7291 has 8 single-ended analog inputs that are multiplexed into the on-chip track-and-hold. Each input channel can accept analog inputs from 0V to 2.5V. Any unused input channels should be connected to GND1 to avoid noise pickup.
14	SDA	Digital Input/Output. Serial bus bidirectional data. This open-drain output requires a pull-up resistor. The output coding is straight binary for the voltage channels and two's complement for the temperature sensor result.
16	V_{DRIVE}	Logic Power Supply Input. The voltage supplied at this pin determines at the voltage at which the interface operates. This pin should be decoupled to GND. The voltage range on this pin is 1.65V to 3.6V and may be less than the voltage at V_{DD}, but should never exceed it by more than 0.3V. To set the input and output thresholds, connect this pin to the supply to which the I^2C bus is pulled.
10	V_{DD}	Supply Voltage, 2.8 V to 3.6 V. This supply should be decoupled to GND with 10 µF and 100 nF decoupling capacitors.
7	V_{REF}	Internal Reference / External Reference supply. The nominal internal reference voltage of 2.5V appears at this pin. Provided the output is buffered, the on-chip reference can be taken from this pin and applied externally to the rest of a system. Decoupling capacitors should be connected to this pin to decouple the reference buffer to GND1. For best performance, it is recommended to use a 10 µF decoupling capacitor. The internal reference can be disabled and an external reference supplied to this pin if required. The input voltage range for the external reference is 2.0 V to 2.5V.
6	GND1	Ground. Ground reference point for the internal reference circuitry on the AD7291. All analog input signals and the external reference signals should be referred to this GND1 voltage. The GND1 pin should be connected to the GND plane of a system. All GND1 pins should ideally be at the same potential and must not be more than 0.3 V apart, even on a transient basis. The V_{REF} should be decoupled to this ground pin via a 10 µF decoupling cap.
9	GND	Ground. Ground reference point for all analog and digital circuitry on the AD7291. The GND pin should be connected to the GND plane of a system. All GND pins should ideally be at the same potential and must not be more than 0.3 V apart, even on a transient basis. Both D_{CAP} and V_{DD} should be decoupled to this GND pin.
15	SCL	Serial I^2C Bus Clock. The data transfer rate in I^2C mode is compatible with both 100 kHz and 400 kHz operating modes. This open-drain output requires pull-up resistors.
12	ALERT	Digital Output. This pin acts as an out-of-range indicator and if enabled, becomes active when the conversion result violates the $DATA_{HIGH}$ or $DATA_{LOW}$ register values. See the Limit Register section.
11, 13	AS0, AS1	Logic Input. Together, the logic state of these inputs selects a unique I^2C address for the AD7291. See Table X for details. The device address depends on the voltage applied to these pins.
17	$\overline{PD}$/RST	Power Down Pin. This pin will place the part into a full power down mode and will enable power conservation when the parts operation is not required. This pin can be used to RESET the device by toggling the pin LOW for a minimum of TBD ns and a maximum of TBDns. If the maximum time is exceeded the part will enter power-down mode.
8	D_{CAP}	Decoupling Capacitor Pin. Decoupling capacitor (10 µF recommended) is connected to this pin to decouple the internal LDO.

CIRCUIT INFORMATION

The AD7291 includes an 8-channel multiplexer, an on-chip track-and-hold, an A/D converter, an on-chip oscillator, internal data registers, internal temperature sensor and an I²C-compatible serial interface, all housed in a 20-lead LFCSP. This package offers considerable space-saving advantages over alternative solutions. The part can be operated from a single supply from 2.8V to 3.6 V and offers 12 bits of resolution. The AD7291 has eight single-ended input channels and an on-chip ±6ppm reference. The analog input range for the AD7928 is 0V to $V_{REF.}$ The AD7298 includes a high accuracy band-gap temperature sensor, which is monitored and digitized by the 12-bit ADC to give a resolution of 0.25°C.

The AD7291 typically remains in a partial power-down state while not converting. When supplies are first applied, the parts power up in a power-down state. Power-up is initiated prior to a conversion, and the device returns to shutdown when the conversion is complete. Conversions can be initiated using the autocycle mode or command mode where the wake-up and a conversion occur during a write address function (see the Modes of Operation section). When the conversion is complete, the AD7291 again enters partial power down mode. This automatic partial power down feature allows power saving between conversions. This means any read or write operation across the I²C interface can occur while the device is in partial power down.

CONVERTER OPERATION

The AD7298 is a 12-bit successive approximation ADC based around a capacitive DAC. Figure 4 and Figure 5 show simplified schematics of the ADC. The ADC is comprised of control logic, SAR, and a capacitive DAC that are used to add and subtract fixed amounts of charge from the sampling capacitor to bring the comparator back into a balanced condition. Figure 4 shows the ADC during its acquisition phase. SW2 is closed and SW1 is in Position A. The comparator is held in a balanced condition and the sampling capacitor acquires the signal on the selected V_{IN} channel.

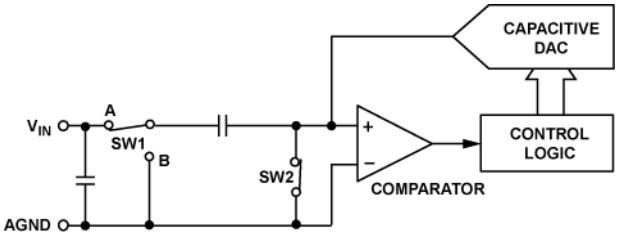


Figure 4. ADC Acquisition Phase

When the ADC starts a conversion (see Figure 5Figure 5), SW2 opens and SW1 moves to Position B, causing the comparator to become unbalanced. The control logic and the capacitive DAC are used to add and subtract fixed amounts of charge to bring the comparator back into a balanced condition. When the comparator is rebalanced, the conversion is complete. The control logic generates the ADC output code. Figure 7 shows the ADC's transfer functions.

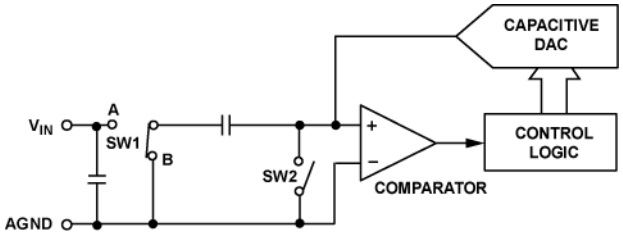


Figure 5. ADC Conversion Phase

ANALOG INPUT

Figure 6 shows an equivalent circuit of the analog input structure of the AD7291. The two diodes, D1 and D2, provide ESD protection for the analog inputs. Care must be taken to ensure that the analog input signal never exceeds the internally generated LDO voltage of 2.5V (D_{CAP}) by more than 300 mV. This causes the diodes to become forward biased and start conducting current into the substrate. 10 mA is the maximum current these diodes can conduct without causing irreversible damage to the part. Capacitor C1, in Figure 6 is typically about TBD pF and can primarily be attributed to pin capacitance. The Resistor R1 is a lumped component made up of the on resistance of a switch (track-and-hold switch) and also includes the on resistance of the input multiplexer. The total resistance is typically about TBD Ω. The capacitor, C2, is the ADC sampling capacitor and has a capacitance of TBD pF typically.

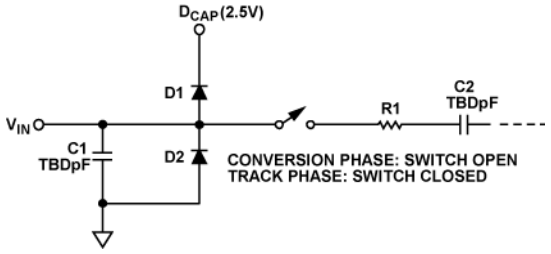


Figure 6. Equivalent Analog Input Circuit

For AC applications, removing high frequency components from the analog input signal is recommended by using an RC low-pass filter on the relevant analog input pin. In applications where harmonic distortion and signal-to-noise ratios are critical, the analog input should be driven from a low impedance source. Large source impedances significantly affect the ac performance of the ADC. This may necessitate the use of an input buffer amplifier. The choice of the op amp is a function of the particular application performance criteria.

ADC TRANSFER FUNCTION

The output coding of the AD7291 is straight binary for the analog input channel conversion results and twos complement, for the temperature conversion result. The designed code transitions occur at successive LSB values (that is, 1 LSB, 2 LSBs, and so forth). The LSB size is V_{REF}/4096 for the AD7291. The ideal transfer characteristic for the AD7291 for straight binary coding is shown in Figure 7.

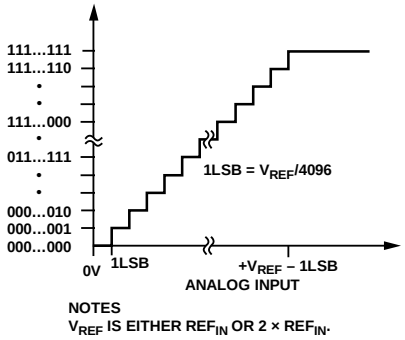


Figure 7. Straight Binary Transfer Characteristic

TEMPERATURE SENSOR OPERATION

The AD7291 contains one local temperature sensor. The on-chip, band gap temperature sensor measures the temperature of the AD7291 die. The temperature sensor module on the AD7291 is based on the three current principle (see Figure 8), where three currents are passed through a diode and the forward voltage drop is measured, allowing the temperature to be calculated free of errors caused by series resistance.

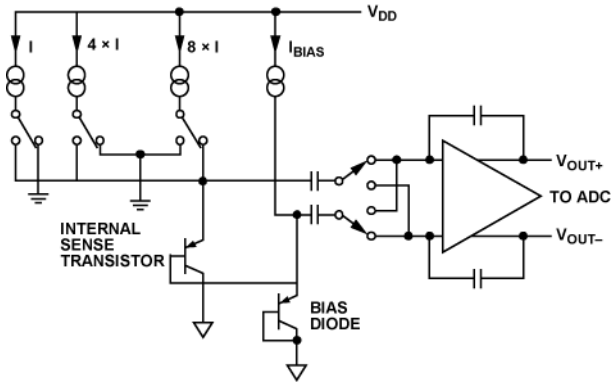


Figure 8. Top Level Structure of Internal Temperature Sensor

The temperature conversion consists of two phases, the integration followed by the conversion. The T_{SENSE} integrates in turn, over a period of one hundred microseconds once the T_{SENSE} bit is selected in the Command Register. This takes place continuously in the background, leaving the user free to perform conversions on the other channels. When integration is complete, a signal passes to the control logic internally to initiate a conversion automatically. It takes a period of approximately100µs to complete the integration and conversion of the temperature result. If the ADC is in command mode, the temperature conversion is performed as soon as the next conversion is completed. In autocycle mode, the conversion is inserted into an appropriate place in the current sequence. If the ADC is idle, the conversion takes place immediately. The T_{SENSE} Result Register stores the result of the last conversion on the temperature channel; these can be read at any time.

Theoretically, the temperature measuring circuit can measure temperatures from –512°C to +511°C with a resolution of 0.25°C. However, temperatures outside T_A (the specified temperature range for the AD7291) are outside the guaranteed operating temperature range of the device.

Temperature Sensor Averaging

The AD7291 incorporates a temperature sensor averaging feature to enhance the accuracy of the temperature measurements. The temperature averaging is performed continuously in the background once the T_{SENSE} bit in the command register is enabled. The temperature is measured each time a T_{SENSE} conversion is performed and a moving average method is used to determine the result in the T_{SENSE} Average Result Register. The average result is given by the following equation;

$$TSENSE\_AVG = \frac{7}{8}\left(\mathrm{Pr}evious\_\mathrm{Re}sult\right)+\frac{1}{8}\left(Current\_\mathrm{Re}sult\right)$$

The average result is then available in the T_{SENSE} Average Result Register whose content is updated after every T_{SENSE} conversion.

The first T_{SENSE} conversion result given by the AD7291 after the temperature sensor has been selected in the command register (bit D7) is the actual first T_{SENSE} conversion result and this result will remain valid until the next T_{SENSE} conversion is completed and the result register updated. If the status of the T_{SENSE}AVG bit is not changed on successive writes to the command register, the averaging function will not be reinitialized and will continue calculating the cumulative average. If the command register is written to and the content of the T_{SENSE}AVG bit changed the averaging function is reset and the next T_{SENSE} average conversion result is the current temperature conversion result.

Temperature Value Format

One LSB of the ADC corresponds to 0.25°C. The temperature reading from the ADC is stored in a 12-bit twos complement format, to accommodate both positive and negative temperature measurements. The temperature data format is provided in Table 10.

Table 6. Temperature Data Format

Temperature (°C)	Digital Output
−40	1111 0110 0000
−25	1111 1001 1100
−10	1111 1101 1000
−0.25	1111 1111 1111
0	0000 0000 0000
+0.25	0000 0000 0001
+10	0000 0010 1000
+25	0000 0110 0100
+50	0000 1100 1000
+75	0001 0010 1100
+100	0001 1001 0000
+105	0001 1010 0100
+125	0001 1111 0100

Temperature Conversion Formula:

Positive Temperature = *ADC Code*/4

Negative Temperature = (4096 - *ADC Code*)/4

V_{DRIVE}

The AD7291 also has the V_{DRIVE} feature. V_{DRIVE} controls the voltage at which the serial interface operates. V_{DRIVE} allows the ADC to easily interface to both a 1.8V and 3V processors. For example, if the AD7291 were operated with an V_{DD} of 3.3V, the V_{DRIVE} pin could be powered from a 1.8V supply. This enables the AD7291 to operate with a larger dynamic range with an V_{DD} of 3.3V while still being able to interface to 1.8V processors. Take care to ensure V_{DRIVE} does not exceed V_{DD} by more than 0.3V (see the Maximum Ratings Section).

THE REFERENCE

The AD7291 can operate with either the internal 2.5V on-chip reference or an externally applied reference. The EXT_REF bit in the Command Register is used to determine whether the internal reference is used. If the EXT_REF bit is selected in the command register, an external reference can be supplied through the V_{REF} pin. On power-up, the internal reference is enabled. Suitable external reference sources for the AD7291 include AD780, AD1582, ADR431, REF193, and ADR391.

The internal reference circuitry consists of a 2.5V band-gap reference and a reference buffer. When the AD7291 is operated in internal reference mode, the 2.5V internal reference is available at the V_{REF} pin, which should be decoupled to GND using a 10 µF capacitor. It is recommended that the internal reference be buffered before applying it elsewhere in the system. The internal reference is capable of sourcing up to TBD µA of current when the converter is static. The reference buffer requires 10ms to power up and charge the TBD µF decoupling capacitor during the power-up time.

RESET

The AD7291 includes a reset feature, which can be used to reset the device and the content of all internal registers including the control register to their default state. To activate the reset operation, the PD pin should be brought low for a minimum of TBD ns and a maximum of 100ns and is asynchronous to the clock, hence it can be triggered at any time. If the PD pin is held low for greater than 100ns the part will enter full power-down mode. It is imperative that the PD pin be held at a stable logic level at all times to ensure normal operation.

INTERNAL REGISTER STRUCTURE

The AD7291 contains 34 internal registers (see Figure 9) that are used to store conversion results, high and low conversion limits, and information to configure and control the device. There are thirty-three data registers and one address pointer register.

Each data register has an address that the address pointer register points to when communicating with it. Table 7 details which registers are read, write or read and write.

ADDRESS POINTER REGISTER

The address pointer register is the register to which the first data byte of every write operation is written automatically, hence this register does not have and does not require an address. The address pointer register is an 8-bit register in which the 6 LSBs are used as pointer bits to store an address that points to one of the AD7291's data registers. The first byte following each write address is to the address pointer register, containing the address of one of the data registers. The 6 LSBs select the data register to which subsequent data bytes are written. Only the 6 LSBs of this register are used to select a data register. On power-up, the address pointer register contains all 0s, pointing to the command register.

Table 6. Address Pointer Register

D1	D0	P5	P4	P3	P2	P1	P0
0	0	Register Select					

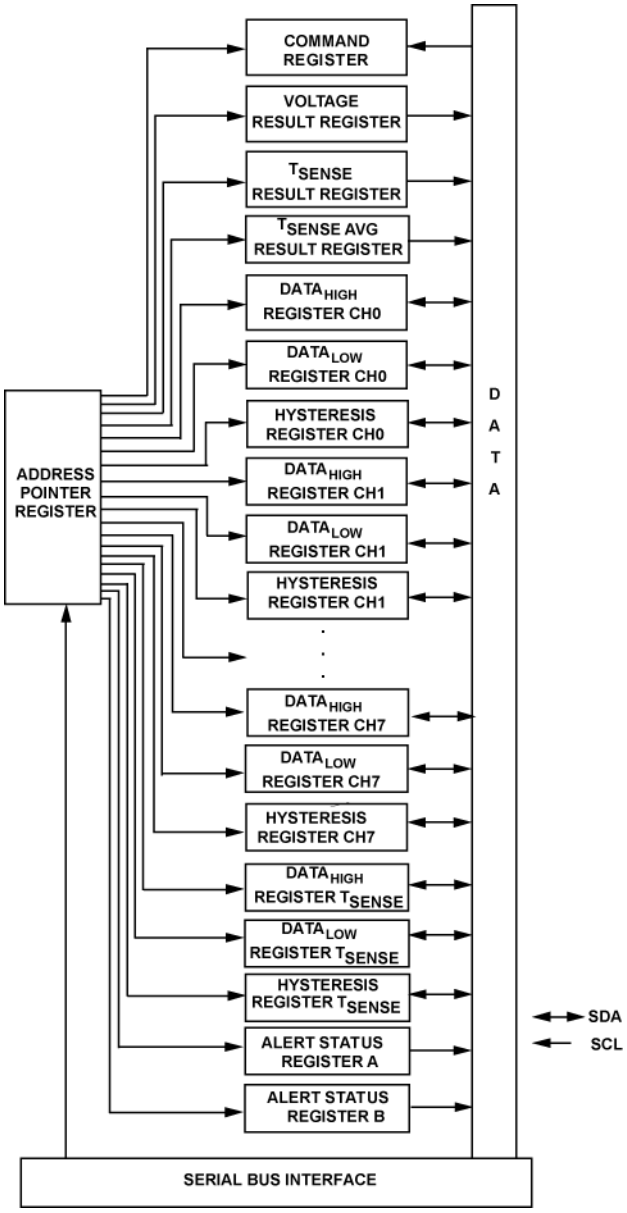


Figure 9.. AD7291 Register Structure

Table 7. AD7291 Register Addresses

HEX Code	P5	P4	P3	P2	P1	P0	Registers	Read or Write
0x00	0	0	0	0	0	0	Command Register	Write
0x01	0	0	0	0	0	1	Voltage Conversion Result Register	Read
0x02	0	0	0	0	1	0	T_{SENSE} Conversion Result Register	Read
0x03	0	0	0	0	1	1	T_{SENSE} Average Result Register	Read
0x04	0	0	0	1	0	0	$DATA_{HIGH}$ Reg CH1	Read/Write
0x05	0	0	0	1	0	1	$DATA_{LOW}$ Reg CH1	Read/Write
0x06	0	0	0	1	1	0	Hysteresis Reg CH1	Read/Write
0x07	0	0	0	1	1	1	$DATA_{HIGH}$ Reg CH2	Read/Write
0x08	0	0	1	0	0	0	$DATA_{LOW}$ Reg CH2	Read/Write
0x09	0	0	1	0	0	1	Hysteresis Reg CH2	Read/Write
0x0A	0	0	1	0	1	0	$DATA_{HIGH}$ Reg CH3	Read/Write
0x0B	0	0	1	0	1	1	$DATA_{LOW}$ Reg CH3	Read/Write
0x0C	0	0	1	1	0	0	Hysteresis Reg CH3	Read/Write
0x0D	0	0	1	1	0	1	$DATA_{LOW}$ Reg CH4	Read/Write
0x0E	0	0	1	1	1	0	$DATA_{HIGH}$ Reg CH4	Read/Write
0x0F	0	0	1	1	1	1	Hysteresis Reg CH4	Read/Write
0x10	0	1	0	0	0	0	$DATA_{HIGH}$ Reg CH5	Read/Write
0x11	0	1	0	0	0	1	$DATA_{LOW}$ Reg CH5	Read/Write
0x12	0	1	0	0	1	0	Hysteresis Reg CH5	Read/Write
0x13	0	1	0	0	1	1	$DATA_{HIGH}$ Reg CH6	Read/Write
0x14	0	1	0	1	0	0	$DATA_{LOW}$ Reg CH6	Read/Write
0x15	0	1	0	1	0	1	Hysteresis Reg CH6	Read/Write
0x16	0	1	0	1	1	0	$DATA_{HIGH}$ Reg CH7	Read/Write
0x17	0	1	0	1	1	1	$DATA_{LOW}$ Reg CH7	Read/Write
0x18	0	1	1	0	0	0	Hysteresis Reg CH7	Read/Write
0x19	0	1	1	0	0	1	$DATA_{HIGH}$ Reg CH8	Read/Write
0x1A	0	1	1	0	1	0	$DATA_{LOW}$ Reg CH8	Read/Write
0x1B	0	1	1	0	1	1	Hysteresis Reg CH8	Read/Write
0x1C	0	1	1	1	0	0	$DATA_{HIGH}$ Reg T_{SENSE}	Read/Write
0x1D	0	1	1	1	0	1	$DATA_{LOW}$ Reg T_{SENSE}	Read/Write
0x1E	0	1	1	1	1	0	Hysteresis Reg T_{SENSE}	Read/Write
0x1F	0	1	1	1	1	1	Alert Status Register A	Read
0x20	1	0	0	0	0	0	Alert Status Register B	Read
0x3F	1	1	1	1	1	1	Factory Test Mode	The user should not access this register.

COMMAND REGISTER

The command register is a 16-bit write-only register that is used to set the operating modes of the AD7291. The bit functions are outlined in Table 8. A two-byte write is necessary when writing to the configuration register. MSB denotes the first bit in the data stream. On power up the default content of the command register is all zero's.

Table 8. Command Register Bits and Default Settings at Power-Up

	MSB							
Channel Bit	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**
Function	CH1	CH2	CH3	CH4	CH5	CH6	CH7	CH8
Setting	Enable = 1 Disable = 0	Enable = 1 Disable = 0	Enable = 1 Disable = 0	Enable = 1 Disable = 0	Enable = 1 Disable = 0	Enable = 1 Disable = 0	Enable = 1 Disable = 0	Enable = 1 Disable = 0

								LSB
Channel Bit	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Function	TSENSE	DONTC	Noise-delayed bit trial sampling.	EXT_REF	Polarity of Alert pin (active high/active low)	Clear Alert	RESET	Autocycle Mode
Default Setting	Enable = 1 Disable = 0		Enable = 1 Disable = 0	Enable = 1 Disable = 0	Active Low = 1 Active High = 0	Enable = 1 Disable = 0	Enable = 1 Disable = 0	Enable = 1 Disable = 0

Table 9. Bit Function Descriptions

Bit	**Mnemonic**	**Comment**
D15 to D8	CH1 to CH8	These 8-channel address bits select the analog input channel(s) to be converted. A 1 in any of Bits D15 to D8 selects a channel for conversion. If more than one channel bit is set to 1, the AD7291 will sequence through the selected channels, starting with the lowest channel. All unused channels should be set to 0. A channel or sequence of channels for conversion must be selected in the command register, prior to initiating a conversion,
D7	TSENSE	This channel selects the temperature sensor channel for conversion. If other analog input channels are also selected for conversion, the AD7291 sequences through the selected analog voltage input channels first and then converts the temperature sensor channel after the conversion of last selected voltage channel is completed.
D5	Noise-delayed bit trial sampling	When this function is enabled, it delays the critical sampling intervals and bit trials from occurring when there is activity on the I^2C bus, thus ensuring optimum dc performance of the AD7291. When this feature is enabled the conversion time may vary. This bit is disabled on power up and it is recommended to write a 1 to enable this feature for normal operation.
D4	EXT_REF	Writing a logic 1 to this bit, enables the use of an external reference. The input voltage range for the external reference is 2V to 2.5V. The external reference should not exceed 2.5V or the device performance will be adversely affected. On power up, the default configuration will have the internal reference enabled.
D3	Polarity of Alert Pin	This bit determines the active polarity of the ALERT pin. The ALERT pin is configured for active low operation if this bit is set to 1, and active high if this bit is set to 0. The default configuration on power up is active high (0).
D2	Clear Alert	This bit clears the content of the Alert Status register. Once the content of the Alert Status register is cleared, this bit should be reprogrammed to a logic 0 to ensure future alerts are detected.
D1	RESET	Setting this bit in the command register resets the content of all internal registers in the AD7291 to their default state including the command register itself. This bit is returned to a 0 once the reset is completed to enable the internal registers to be reprogrammed.
D0	Autocycle Mode	Writing a 1 to this bit in the command registers enables the auto-cycle mode of operation. In this mode, the channels selected in bit D15 to D7 are continuously converted by the AD7291. This function is used in conjunction with the limit registers, which can be programmed to issue an alert if the conversion result exceeds the preset limit for any channel selected for conversion.

Table 10. Channel Selection bits for Command Register

D15	D14	D13	D12	D11	D10	D9	D8	Selected Analog Input Channel	Comments
0	0	0	0	0	0	0	0	No channel selected	If more than one channel is selected, the AD7291 converts the selected sequence of channels starting with the lowest channel in the sequence.
0	0	0	0	0	0	0	1	Convert on Channel 8 ($V_{IN}8$)	
0	0	0	0	0	0	1	0	Convert on Channel 7 ($V_{IN}7$)	
0	0	0	0	0	1	0	0	Convert on Channel 6 ($V_{IN}6$)	
0	0	0	0	1	0	0	0	Convert on Channel 5 ($V_{IN}5$)	
0	0	0	1	0	0	0	0	Convert on Channel 4 ($V_{IN}4$)	
0	0	1	0	0	0	0	0	Convert on Channel 3 ($V_{IN}3$)	
0	1	0	0	0	0	0	0	Convert on Channel 2 ($V_{IN}2$)	
1	0	0	0	0	0	0	0	Convert on Channel 1 ($V_{IN}1$)	

Table 11. T_{SENSE} Data Format

Input	D11(MSB)	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0 (LSB)
Value (°C)	−512	+256	+128	+64	+32	+16	+8	+4	+2	+1	+0.5	+0.25

Sample Delay and Bit Trial Delay

It is recommended that no I^2C bus activity occur when a conversion is taking place; however, this may not be possible, for example, when operating in autocycle mode. Bit D5 in the configuration register is used to delay critical sample intervals and bit trials from occurring while there is activity on the I^2C bus. This results in a quiet period for each bit decision. On power up, Bit[D5] is disabled and the bit trial-and-sample interval delaying mechanism is not implemented. It is recommended to enabled this bit in the command register to ensure the conversion results are less susceptible to interference from external noise. To enable this functionality write a 1 to the respective bit in the command register. When enabled, the AD7291 delays the bit trials from occurring when there is activity on the I^2C bus, thus ensuring good dc linearity performance by reducing the glitch noise seen by the converter. In applications where ac rather than dc performance is critical, this function can be disabled to ensure the sampling point is fixed as this feature may introduce excessive jitter, degrading the SNR for large signals above 300 Hz. In cases where there is excessive activity on the interface lines, enabling these bits may cause the overall conversion time to increase.

The AD7291 also incorporates functionality that allows it to reject glitches shorter than 50 ns. This feature improves the noise susceptibility of the device.

VOLTAGE CONVERSION RESULT REGISTER (0X01)

The conversion result register is a 16-bit read-only register that stores the conversion result from the ADC in straight binary format. A 2-byte read is necessary to read data from this register. Table 12 and Table 13 show the contents of the first and second bytes of data to be read from AD7291. Each AD7291 conversion result consists of four channel address bits (see Table 14) and the 12-bit data result. Bit D15 to Bit D12 are the channel address bits which identifies the ADC channel that corresponds to the subsequent result. Bit D11 to Bit D0 contain the most recent ADC result.

Table 12. Conversion Value Register (First Read)

D15	D14	D13	D12	D11	D10	D9	D8
ADD3	ADD2	ADD1	ADD0	B11 (MSB)	B10	B9	B8

Table 13. Conversion Value Register (Second Read)

D7	D6	D5	D4	D3	D2	D1	D0
B7	B6	B5	B4	B3	B2	B1	B0

Table 14. Channel Address bits for Result Register

ADD2	ADD2	ADD1	ADD0	Analog Input Channel
0	0	0	0	$V_{IN}1$
0	0	0	1	$V_{IN}2$
0	0	1	0	$V_{IN}3$
0	0	1	1	$V_{IN}4$
0	1	0	0	$V_{IN}5$
0	1	0	1	$V_{IN}6$
0	1	1	0	$V_{IN}7$
0	1	1	1	$V_{IN}8$
1	0	0	0	T_{SENSE}
1	0	0	1	T_{SENSE} average result

Temperature Value Format

The temperature reading from the ADC is stored in an 11-bit twos complement format, D11 to D0, to accommodate both positive and negative temperature measurements. The temperature data format is provided in Table 11.

T_{SENSE} RESULT REGISTER (0x02)

The T_{SENSE} result register is a 16-bit read-only register used to store the ADC data generated from the internal temperature sensor. This register stores the temperature readings from the ADC in an 11-bit twos complement format, D11 to D0, and uses bits[D15:D12] to store the channel address bits. Conversions take place approximately every 5ms. Table 11 details the temperature data format which applies to the internal temperature sensor.

Table 15. T_{SENSE} Result Register (First Read)

MSB							LSB
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**
ADD3	ADD2	ADD1	ADD0	B11	B10	B9	B8

Table 16. T_{SENSE} Result Register (Second Read)

MSB							LSB
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
B7	B6	B5	B4	B3	B2	B1	B0

T_{SENSE} AVERAGE RESULT REGISTER (0x03)

The T_{SENSE} average result register is a 16-bit read-only register used to store the average result from the internal temperature sensor. This register stores the average temperature readings from the ADC in an 11-bit twos complement format, D11 to D0, and uses bits[D15:D12] to store the channel address bits. The T_{SENSE} average result register is updated after every T_{SENSE} conversion is completed. The first T_{SENSE} average conversion result given by the AD7291 after averaging is enabled is the actual first T_{SENSE} conversion result. Table 11 details the temperature data format, which applies to the internal temperature sensor. (See Temperature Sensor Averaging section for more details)

Table 17. T_{SENSE} Average Register (First Read)

MSB							LSB
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**
ADD3	ADD2	ADD1	ADD0	B11	B10	B9	B8

Table 18. T_{SENSE} Average Register (Second Read)

MSB							LSB
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
B7	B6	B5	B4	B3	B2	B1	B0

LIMIT REGISTERS

The AD7291 has nine pairs of limit registers. Each pair stores high and low conversion limits for each analog input channel and the internal temperature sensor. Each pair of limit registers has one associated hysteresis register. All 27 registers are 16 bits wide; only the 12 LSBs of the registers are used for the AD7291. The 4 MSBs, D15 and D12 in these registers, should contain 0s.

On power-up, the contents of the $DATA_{HIGH}$ register for each analog voltage channel is full scale (0x0FFF), while the default contents of the $DATA_{LOW}$ voltage channels registers is zero scale (0x0000). The default content for the $DATA_{HIGH}T_{SENSE}$ is 0x07FF and 0x0800 for the $DATA_{LOW}$ T_{SENSE} limits register because they are in twos complement 12-bit format. The AD7291 signals an alert in hardware if the conversion result moves outside the upper or lower limit set by the limit registers.

$DATA_{HIGH}$ Register

The $DATA_{HIGH}$ registers for CH1 to CH8 and the internal temperature sensor are 16-bit read/write registers; only the 12 LSBs of each register are used. D15 to D12 are not used in the register and are set to 0s. This register stores the upper limit that activates the ALERT output. If the value in the conversion result register is greater than the value in the $DATA_{HIGH}$ register, an ALERT occurs for that channel. When the conversion result returns to a value at least *N* LSBs below the $DATA_{HIGH}$ register value, the ALERT output pin is reset. The value of *N* is taken from the hysteresis register associated with that channel. The ALERT pin can also be reset by writing to bit D2 in the command register.

Table 19. $DATA_{HIGH}$ Register (First Read/Write)

D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**
0	0	0	0	B11	B10	B9	B8

Table 20. $DATA_{HIGH}$ Register (Second Read/Write)

D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
B7	B6	B5	B4	B3	B2	B1	B0

$DATA_{LOW}$ Register

The $DATA_{LOW}$ register for each channel is a 16-bit read/write register; only the 12 LSBs of each register are used. D15 to D12 are not used in the register and are set to 0s. The register stores the lower limit that activates the ALERT output. If the value in the conversion result register is less than the value in the $DATA_{LOW}$ register, an ALERT occurs for that channel. When the conversion result returns to a value at least *N* LSBs above the $DATA_{LOW}$ register value, the ALERT output pin is reset. The value of *N* is taken from the hysteresis register associated with that channel. The ALERT output pin can also be reset by writing to bit D2 in the command register.

Table 21. $DATA_{LOW}$ Register (First Read/Write)

D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**
0	0	0	0	B11	B10	B9	B8

Table 22. $DATA_{LOW}$ Register (Second Read/Write)

D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
B7	B6	B5	B4	B3	B2	B1	B0

Hysteresis Register

Each analog input channel and the internal temperature sensor has its own hysteresis register, which is a 16-bit read/write register. Only the 12 LSBs are used. D15 to D12 are not used in the register and are set to 0s. The hysteresis register stores the hysteresis value, *N,* when using the limit registers. Each pair of limit registers has a dedicated hysteresis register. The hysteresis value determines the reset point for the ALERT pin if a violation of the limits has occurred. For example, if a hysteresis value of 8 LSBs is required on the upper and lower limits of Channel 1, the 12-bit word, 0000 0000 0000 1000, should be written to the hysteresis register of CH1, the address of which is 0x06. (See Table 24 & Table 25) On power-up, the hysteresis registers content defaults to all zeros (0x0000). If a hysteresis value is required, that value must be written to the hysteresis register for the channel in question.

Table 23. Hysteresis Register (First Read/Write)

D15	D14	D13	D12	D11	D10	D9	D8
0	0	0	0	B11	B10	B9	B8

Table 24. Hysteresis Register (Second Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0
B7	B6	B5	B4	B3	B2	B1	B0

ALERT STATUS REGISTERS A & B

The alert status register is a 16-bit, read only register that provides information on an alert event. If a conversion result activates the ALERT pin, as described in the Limit Registers section, the alert status register may be read to gain further information. There are two Alert Status Registers on the AD7291; Alert Register A which stores alerts for the analog voltage conversion channels (see Table 25 & Table 26) and Alert Register B which stores alerts for the internal temperature sensor only (see Table 27 & Table 28).

Both Alert Status Registers contain two status bits per channel, one corresponding to the $DATA_{HIGH}$ limit and the other to the $DATA_{LOW}$ limit. The bit with a status of 1 shows where the violation occurred—that is, on which channel—and whether the violation occurred on the upper or lower limit. If a second alert event occurs on the other channel between receiving the first alert and interrogating the alert status register, the corresponding bit for that alert event is also set. The entire contents of the alert status register can be cleared by writing 1, to Bits D2 in the command register.

For example, if bit D14 in Alert Status Register A is set to 1, this indicates that the lower limit on Channel 4 (Register 0x0D) has been violated while if bit D11 is set 1, the upper limit on channel 2 has been violated (Register 0x07). The $TSENSE\_AVG_{HI}$ and $TSENSE\_AVG_{LO}$ alerts are determined from the comparison of the T_{SENSE} average results register with the $DATA_{HIGH}$ and $DATA_{LOW}$ limits for the T_{SENSE} channel (0x1C, 0x1D)

Table 25. Alert Status Register A (First Read Byte)

D15	D14	D13	D12	D11	D10	D9	D8
$CH8_{HI}$	$CH8_{LO}$	$CH7_{HI}$	$CH7_{LO}$	$CH6_{HI}$	$CH6_{LO}$	$CH5_{HI}$	$CH5_{LO}$

Table 26. Alert Status Register A (Second Read Byte)

D7	D6	D5	D4	D3	D2	D1	D0
$CH4_{HI}$	$CH4_{O}$	$CH3_{HI}$	$CH3_{LO}$	$CH2_{HI}$	$CH2_{LO}$	$CH1_{HI}$	$CH1_{LO}$

Table 27. Alert Status Register B (First Read Byte)

D15	D14	D13	D12	D11	D10	D9	D8
0	0	0	0	0	0	0	0

Table 28. Alert Status Register B (Second Read Byte)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	TSENSE AVG_{HI}	TSENSE AVG_{LO}	TSENSE HIGH	TSENSE LOW

MODES OF OPERATION

When supplies are first applied to the AD7291, the ADC powers up in partial power down mode and normally remains in this partial power down state while not converting. Once the master addresses the AD7291 it exits partial power down. There are two methods of initiating a conversion on the AD7291, Command mode and Autocycle mode.

COMMAND MODE

In command mode, the AD7291 ADC converts on-demand on either a single channel or a sequence of channels. Writing in the command register puts the part into command mode. This is the default mode of operation and allows a conversion to be automatically selected any time a write operation occurs to the Command Register. To enter this mode, the required combination of channels is written into the command register (0x00). Following the write operation, the AD7291 must be addressed again to indicate that a read operation is required. The read then takes place from the voltage or temperature conversion result register. For the first conversion to occur the address pointer written to the AD7291 must points to the Voltage or Temperature Conversion Result Register. The conversion is completed while the first four Channel Address bits are read. The next conversion in the sequence takes place, once the next read from the result register is initiated. The acquisition and conversion times combined should take approximately 3 µs. When in command mode, the part cycles through the selected channels from the lowest selected channel in the sequence to the next lowest until all the channels in the sequence are converted.

To exit the command mode, the master should not acknowledge the final byte of data. This stops the AD7291 transmitting, allowing the master to assert a stop condition on the bus. On the receipt of a STOP condition, the AD7291 stops converting and enters partial power down mode, but the content of the command register is preserved. Once the part is readdress and a read initiated from the Voltage Conversion Register the AD7291 will begin converting on the previously selected sequence of channels. The conversion sequence will starting converting the first selected channel in the sequence That is, if Channel 1, 2 and 3 are selected and a STOP condition occurs after Channel 1's result is read, on resumption of conversions Channel 1 will be reconverted and the conversion sequence will continue.

The example in Figure 10 shows the command mode converting on a sequence of channels including $V_{IN}1$, $V_{IN}2$, and $V_{IN}3$

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address followed by the write bit (low).
3. The addressed slave device (AD7291 asserts an acknowledge on SDA.
4. The master sends the Command Register Address 0x00. The slave asserts an acknowledge on SDA.
5. The master sends the first Data Byte 0xE0 to the Command Register, which selects the $V_{IN}1$, $V_{IN}2$ and $V_{IN}3$ channels.
   The slave asserts an acknowledge on SDA.
6. The master sends the second Data Byte 0x20 to the Command Register. The slave asserts an acknowledge on SDA.
7. The master sends the result register address (0x01). The slave asserts an acknowledge on SDA.
8. The master sends the 7-bit slave address followed by the write bit (high).
9. The slave (AD7291) asserts an acknowledge on SDA.
10. The master receives a data byte, which contains the channel address bits, and the four MSBs of the converted result for Channel $V_{IN}1$. The master then asserts an acknowledge on SDA.
11. The master receives the second data byte, which contains the eight LSBs of the converted result for Channel $V_{IN}1$. The master then asserts on acknowledge on SDA.
12. Point 10 and Point 11 repeat for Channel $V_{IN}2$ and Channel $V_{IN}3$.
13. Once the master has received the results from all the selected channels, the slave again converts and outputs the result for the first channel in the selected sequence. Point 10 to Point 12 are repeated.
14. Master asserts a no acknowledge on SDA and a stop condition on SDA to end the conversion and exit command mode.

To change the conversion sequence, rewrite a new sequence to the command mode. If a new write to the Command Register is performed while an existing conversion sequence is underway, the existing conversion sequence is terminated and the next conversion performed is the first selected channel from the new sequence. The maximum throughput that can be achieved using this mode with a 400 kHz I^2C clock is (400 kHz/18) = 22.2 kSPS.

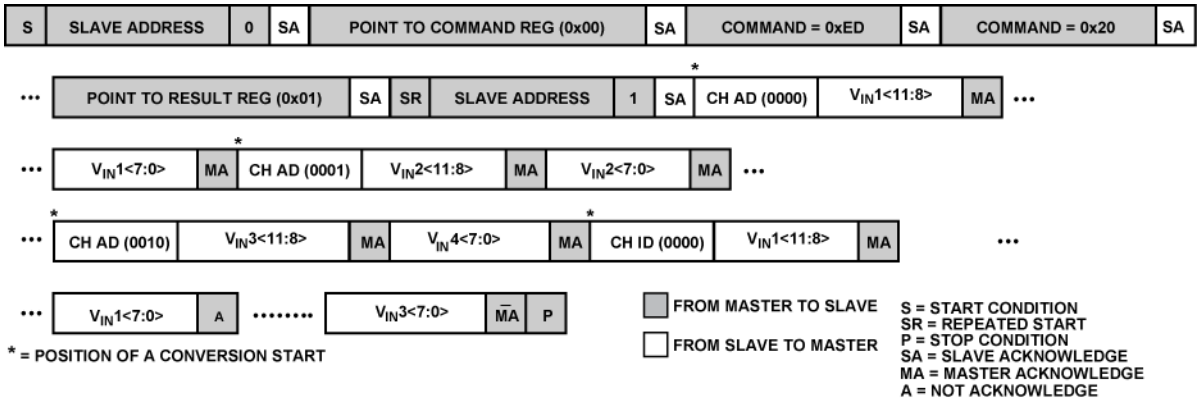


Figure 10. Command Mode Operation

AUTOCYCLE MODE

The AD7291 can be configured to convert continuously on a programmable sequence of channels making it the ideal mode of operation for system monitoring. These conversions take place in the background approximately every 50 µs, and are transparent to the master. The acquisition, and conversion times combined for any channel should take approximately 3 µs Typically, this mode is used to automatically monitor a selection of channels with either the limit registers programmed to signal an out-of-range condition via the alert function or the minimum/maximum recorders tracking the variation over time of a particular channel. Reads and writes can be performed at any time (the ADC Result Register 0x01 contains the most recent conversion result).

On power up, this mode is disabled. To enable this mode, write to Bit D0 in the Command Register (0x00) and select the desired channels for conversion by writing to the corresponding channel bits D15 to D7. If more than one channel bit is set in the configuration register, the ADC automatically cycles through the channel sequence starting with the lowest channel and working its way up through the sequence. Once the sequence is complete, the ADC starts converting on the lowest channel again, continuing to loop through the sequence until this mode is exited. Once a conversion is completed the conversion result is compared with the content of the Limit Registers and Alert Status Registers are automatically updated. If a violation of the Limit Registers is found the ALERT pin is asserted with the polarity determined by bit D3 in the Command Register.

If a command mode conversion is required while the autocycle mode is active, it is necessary to disable the autocycle mode before proceeding to the command mode. This is achieved by setting Bit D0 of the command register to 1. When the command mode conversion is complete, the user can re-enable Autocycle mode by setting bit D0 to 1 in the command register. In autocycle mode, the AD7291 does not enter partial power down on receipt of a STOP condition, hence conversions and alert monitoring will continue to function.

I²C INTERFACE

GENERAL I²C TIMING

Figure 11 shows the timing diagram for general read and write operations using an I²C-compliant interface.

The I²C bus uses open-drain drivers; therefore, when no device is driving the bus, both SCL and SDA are high. This is known as idle state. When the bus is idle, the master initiates a data transfer by establishing a start condition, defined as a high-to-low transition on the serial data line (SDA) while the serial clock line (SCL) remains high. This indicates that a data stream follows. The master device is responsible for generating the clock.

Data is sent over the serial bus in groups of nine bits—eight bits of data from the transmitter followed by an acknowledge bit (ACK) from the receiver. Data transitions on the SDA line must occur during the low period of the clock signal and remain stable during the high period. The receiver should pull the SDA line low during the acknowledge bit to signal that the preceding byte has been received correctly. If this is not the case, cancel the transaction.

The first byte that the master sends must consist of a 7-bit slave address, followed by a data direction bit. Each device on the bus has a unique slave address; therefore, the first byte sets up communication with a single slave device for the duration of the transaction.

The transaction can be used either to write to a slave device (data direction bit = 0) or to read data from it (data direction bit = 1). In the case of a read transaction, it is often necessary first to write to the slave device (in a separate write transaction) to tell it from which register to read. Reading and writing cannot be combined in one transaction.

When the transaction is complete, the master can keep control of the bus, initiating a new transaction by generating another start bit (high-to-low transition on SDA while SCL is high). This is known as a repeated start (Sr). Alternatively, the bus can be relinquished by releasing the SCL line followed by the SDA line. This low-to-high transition on SDA while SCL is high is known as a stop bit (P), and it leaves the I²C bus in its idle state (no current is consumed by the bus).

The example in Figure 11 shows a simple write transaction with an AD7291 as the slave device. In this example, the AD7291 register pointer is being set up ready for a future read transaction.

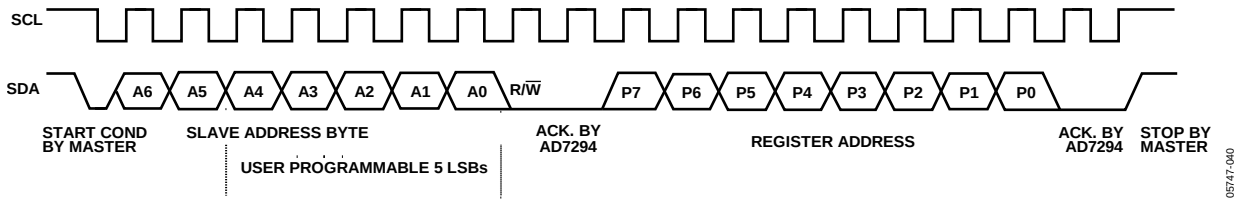


Figure 11. General I²C Timing

SERIAL BUS ADDRESS BYTE

The first byte the user writes to the device is the slave address byte. Similar to all I²C-compatible devices, the AD7291 has a 7-bit serial address. The 4 LSBs are user-programmable by the 3 three-state input pins, AS0 and AS1 as shown in Table 29.

In Table 29, H means tie the pin to V_{DRIVE}, L means tie the pin to GND, and NC refers to a pin left floating. Note that in this final case, the stray capacitance on the pin must be less than 30 pF to allow correct detection of the floating state; therefore, any PCB trace must be kept as short as possible.

Table 29. Slave Address Control Using Three-State Input Pins

AS1	AS0	Slave Address(A6 to A0)	
		Binary	Hex
H	H	010 0000	0x20
H	NC	010 0010	0x22
H	GND	010 0011	0x23
NC	H	010 1000	0x28
NC	NC	010 1010	0x2A
NC	GND	010 1011	0x2B
GND	H	010 1100	0x2C
GND	NC	010 1110	0x2E
GND	GND	010 1111	0x2F

INTERFACE PROTOCOL

The AD7291 uses the following I²C protocols.

Writing Two Bytes of Data to a 16-Bit Register

All registers on the AD7921 are 16 bit registers; therefore, two bytes of data are required to write a value to any one of these registers. Writing two bytes of data to a registers consists of the following sequence:

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address followed by the write bit (low).
3. The addressed slave device asserts an acknowledge on SDA.
4. The master sends a register address. The slave asserts an acknowledge on SDA.
5. The master sends the first data byte (most significant).
6. The slave asserts an acknowledge on SDA.
7. The master sends the second data byte (least significant).
8. The slave asserts an acknowledge on SDA.
9. The master asserts a stop condition on SDA to end the transaction.

Writing to Multiple Registers

Writing to multiple address registers consists of the following:

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address followed by the write bit (low).
3. The addressed slave device (AD7291) asserts an acknowledge on SDA.
4. The master sends a register address, for example the $DATA_{HIGH}$ CH1 register address. The slave asserts an acknowledge on SDA.
5. The master sends the first data byte.
6. The slave asserts an acknowledge on SDA.
7. The master sends the second data byte.
8. The slave asserts an acknowledge on SDA.
9. The master sends a second register address, for example the Command register. The slave asserts an acknowledge on SDA.
10. The master sends the first data byte.
11. The slave asserts an acknowledge on SDA.
12. The master sends the second data byte.
13. The slave asserts an acknowledge on SDA.
14. The master asserts a stop condition on SDA to end the transaction.

The previous examples detail writing to two registers only (the $DATA_{HIGH}$ CH1 register and the Command register). However, the AD7291 can read from multiple registers in one write operation as shown in Table 12.

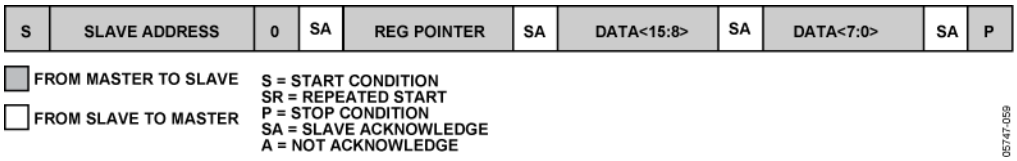


Figure 12. Writing Two Bytes of Data to a 16-Bit Register

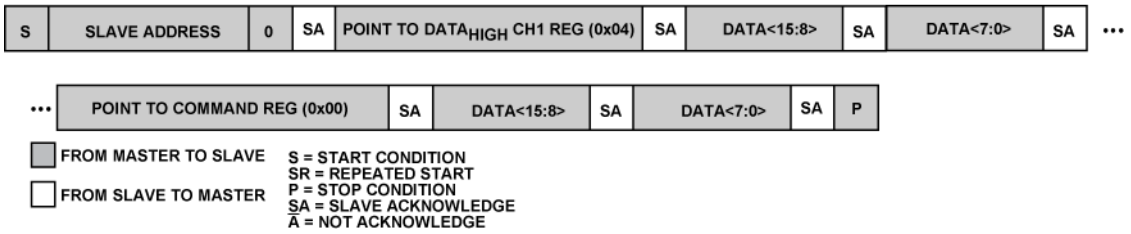


Figure 13. Writing to Multiple Registers

Reading Two Bytes of Data from a 16-Bit Register

Reading the contents from any of the 16-bit registers is a two byte read operation, as shown in Figure 12. In this protocol, the first part of the transaction writes to the register pointer. When the register address has been set up, any number of reads can be performed from that particular register without having to write to the address pointer register again. When the required number of reads is completed, the master should not acknowledge the final byte. This tells the slave to stop transmitting, allowing a stop condition to be asserted by the master. Further reads from this register can be performed in a future transaction without having to rewrite to the register pointer.

If a read from a different address is required, the relevant register address has to be written to the address pointer register, and again, any number of reads from this register can then be performed. In the following example, the master device reads three lots of two-byte data from a slave device, but as many lots consisting of two-bytes can be read as required. This protocol assumes that the particular register address has been set up by a single byte write operation to the address pointer register.

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address followed by the read bit (high).
3. The addressed slave device asserts an acknowledge on SDA.
4. The master receives a data byte.
5. The master asserts an acknowledge on SDA.
6. The master receives a second data byte.
7. The master asserts an acknowledge on SDA.
8. The master receives a data byte.
9. The master asserts an acknowledge on SDA.
10. The master receives a second data byte.
11. The master asserts an acknowledge on SDA.
12. The master receives a data byte.
13. The master asserts an acknowledge on SDA.
14. The master receives a second data byte.
15. The master asserts a no acknowledge on SDA to notify the slave that the data transfer is complete.
16. The master asserts a stop condition on SDA to end the transaction.

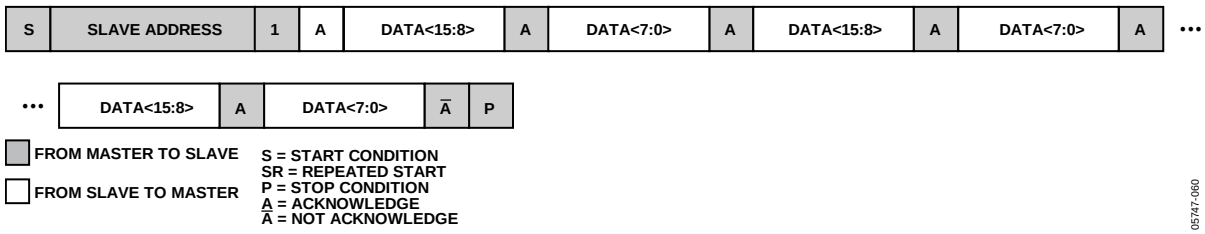
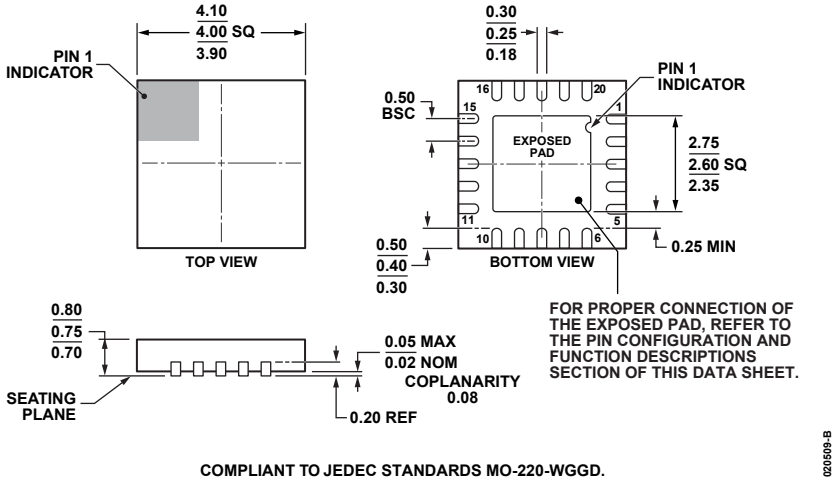


Figure 14. Reading Three Lots of Two Bytes of Data from the Conversion Result Register

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WGGD.

Figure 15. 20 Lead Lead Frame Chip Scale Package [LFCSP_WQ]
4 x 4 mm Body, Very Very Thin Quad
(CP-20-8)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD7291BCPZ	−40°C to +125°C	20 Lead - Lead Frame Chip Scale package	CP-20-8
AD7291BCPZ-RL7	−40°C to +125°C	20 Lead - Lead Frame Chip Scale package	CP-20-8

PR08729-0-11/09(PrC)