800mA Synchronous Buck-Boost DC/DC Converter

FEATURES

- **Regulated Output with Input Voltages Above, Below, or Equal to the Output**
- **800mA Continuous Output Current from a Single Lithium-Ion/Polymer Cell**
- **Single Inductor**
- **1.8V to 5.25V V_{OUT} Range**
- 2.4V to 5.5V V_{IN} Range
- 1MHz Fixed Frequency Operation
- Output Disconnect in Shutdown
- 35µA Quiesecent Current in Burst Mode Operation
- <5µA Shutdown Current
- Internal Soft-Start
- Small, Thermally Enhanced 8-Lead (2mm x 3mm) DFN package

APPLICATIONS

- Miniature Hard Disk Drives
- MP3 Players
- Digital Cameras
- Cellular Handsets
- PDAs, Handheld PC
- GPS Receivers

DESCRIPTION

The LTC®3538 is a highly efficient, low noise, buck-boost DC/DC converter that operates from input voltages above, below, and equal to the output voltage. The topology incorporated in the IC provides a continuous transfer function through all operating modes, making the product ideal for single Lithium Ion or multicell Alkaline or NiMH applications where the output voltage is within the battery voltage range.

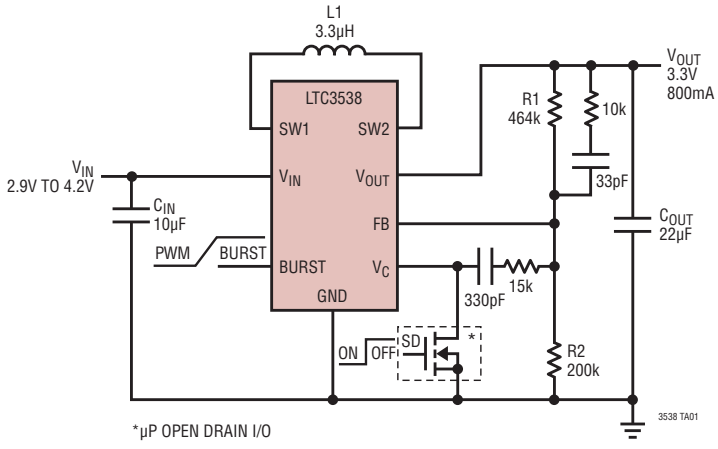
The LTC3538 is suited for use in Micro Hard Disk Drive (µHDD) applications with its 800mA current capability. Burst Mode® operation provides high efficiency at light loads.

The LTC3538 includes two 0.17Ω N-channel and two 0.2Ω P-channel MOSFET switches. Operating frequency is internally set to 1MHz to minimize solution footprint while maximizing efficiency.

Other features include <5µA shutdown current, internal soft-start, short circuit protection and thermal shutdown. The LTC3538 is available in a low profile (0.75mm), thermally enhanced 8-lead (2mm × 3mm) DFN package.

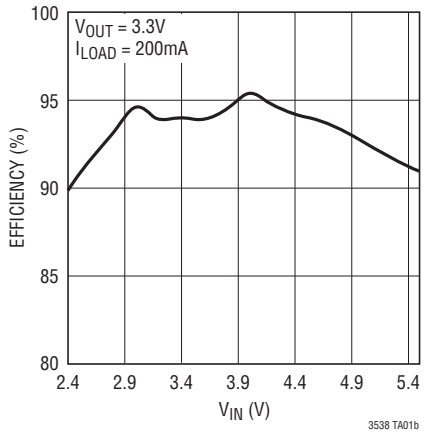
TYPICAL APPLICATION

Li-Ion/Polymer to 3.3V at 800mA



*µP OPEN DRAIN I/O

Efficiency vs V_{IN}

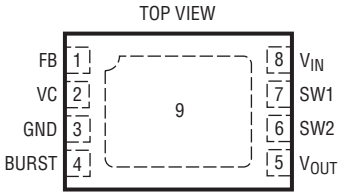


ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN},V_{OUT} Voltage ..... –0.3V to 6V
SW1,SW2 Voltage
DC ..... –0.3V to 6V
Pulsed < 100ns ..... –0.3V to 7V
BURST, FB, VC Voltage ..... –0.3V to 6V
Operating Temperature (Note 2) ..... –40°C to 85°C
Maximum Junction Temperature (Note 3) ..... 125°C
Storage Temperature Range ..... –65°C to 125°C

PIN CONFIGURATION



DCB PACKAGE
8-LEAD (2mm × 3mm) PLASTIC DFN

T_{JMAX} = 125°C
θ_{JA} = 75°C/W 4-LAYER BOARD, θ_{JC} = 13.5°C/W
EXPOSED PAD (PIN 9) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3538EDCB#PBF	LTC3538EDCB#TRPBF	LCRB	8-Lead (2mm × 3mm) Plastic DFN	–40°C to 85°C
LEAD BASED FINISH	**TAPE AND REEL**	**PART MARKING**	**PACKAGE DESCRIPTION**	**TEMPERATURE RANGE**
LTC3538EDCB	LTC3538EDCB#TR	LCRB	8-Lead (2mm × 3mm) Plastic DFN	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = V_{OUT} = 3.6V, BURST = 0V, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage		●	2.4		5.5	V
Feedback Voltage	(Note 4)	●	0.980	1.00	1.020	V
Feedback Input Current	(Note 4)			1	50	nA
V_{IN} Quiescent Current – Shutdown	V_C = 0V, Not Including Switch Leakage			1.5	5	µA
V_{IN} Quiescent Current – Active	FB = 0.8V			1	1.8	mA
V_{IN} Quiescent Current – Sleep	FB = 1.2V, BURST = V_{IN}			35	60	µA
NMOS Switch Leakage	Switches B and C			0.1	7	µA
PMOS Switch Leakage	Switches A and D			0.1	10	µA
NMOS Switch On-Resistance	Switches B and C			0.17		Ω
PMOS Switch On-Resistance	Switches A and D			0.2		Ω
Input Current Limit		●	1.4	2		A
Reverse Current Limit				0.5		A
Burst Mode Operational Peak Current				0.9		A
Maximum Duty Cycle	Boost (%Switch C On) Buck (% Switch A On) Buck (% Switch D On)	● ● ●	70 100 100	88		% % %

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = V_{OUT} = 3.6V, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Minimum Duty Cycle	FB = 1.2V	●			0	%
Frequency Accuracy		●	0.8	1	1.2	MHz
Internal Soft-Start Time				1.5		ms
Error Amp A_{VOL}				80		dB
Error Amp Source Current	V_C = 1.5V, FB = OV			–13		µA
Error Amp Sink Current	V_C = 1.5V, FB = 1.2V			130		µA
V_C Shutdown Threshold (Off)	IC is Disabled	●			0.25	V
V_C Output Current in Shutdown	V_C = GND			–1	–3	µA
BURST Threshold (High)		●	1.4			V
BURST Threshold (Low)		●			0.4	V
BURST Input Current	V_{BURST} = 3.6V			0.1	1	µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3538 is guaranteed to meet performance specifications from 0°C to 85°C. Specifications over –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.

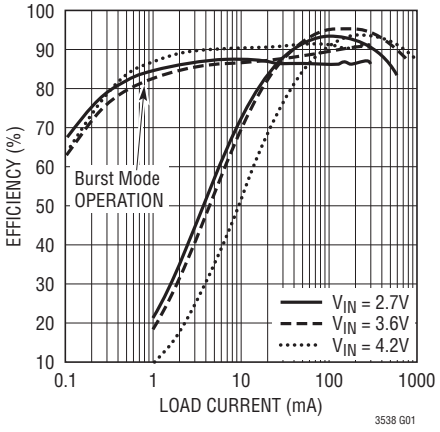
Note 3: This IC includes over-temperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when over-temperature protection is active. Continuous operation above the specified maximum operating junction temperature may result in device degradation or failure.

Note 4: The IC is tested in a feedback loop to make the measurement.

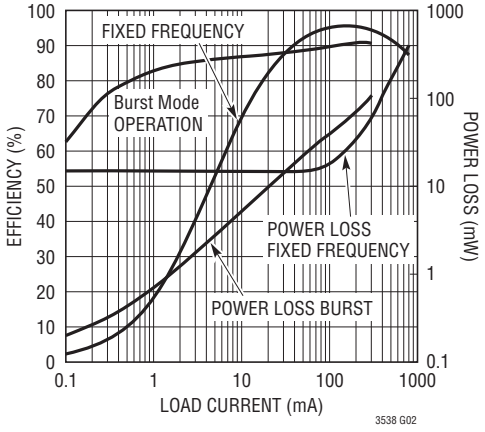
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C unless otherwise noted

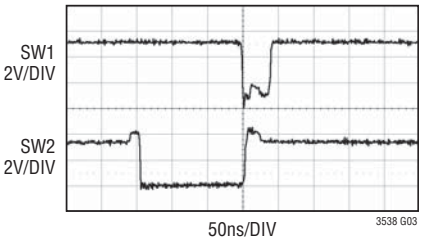
Li-Ion to 3.3V Efficiency



Efficiency and Power Loss vs Load Current



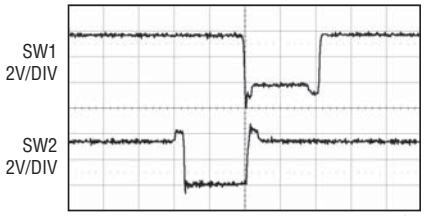
Switch Pins Before Entering Boost Mode



V_{IN} = 2.9V
V_{OUT} = 3.3V AT 500mA

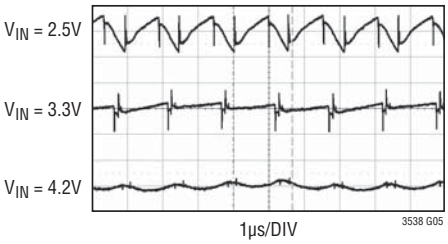
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C unless otherwise noted

Switch Pins Before Entering Buck Mode



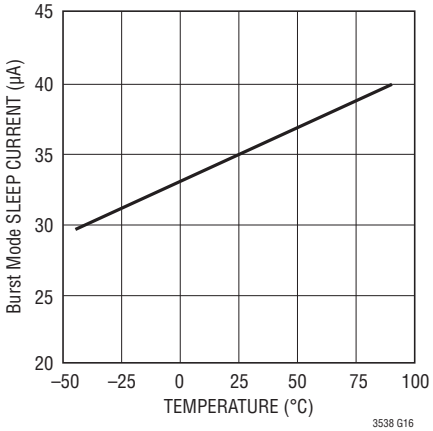
V_{IN} = 3.9V
V_{OUT} = 3.3V AT 500mA

V_{OUT} Ripple in Buck, Buck-Boost and Boost Modes at 500mA Load

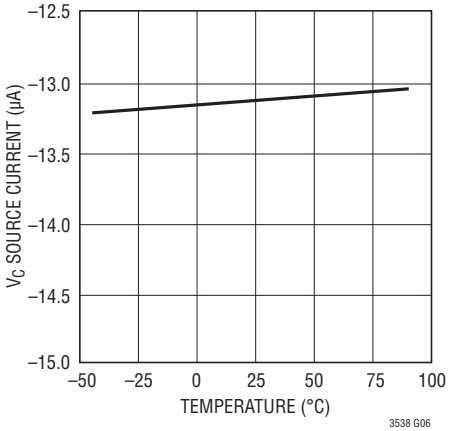


V_{OUT} = 3.3V, AC-COUPLED
20mV/DIV
C_{OUT} = 22µF
I_{LOAD} = 500mA

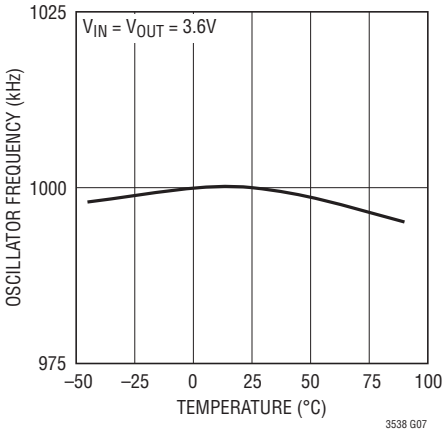
Burst Mode Sleep Current vs Temperature



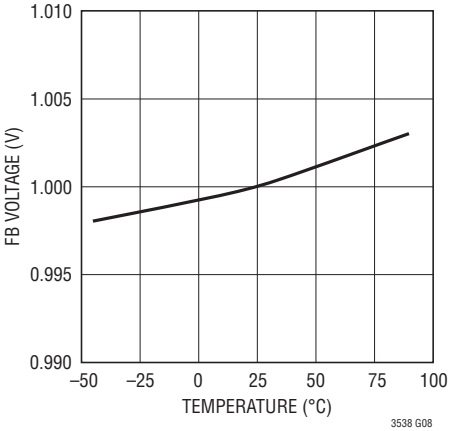
Error Amplifier Source Current vs Temperature



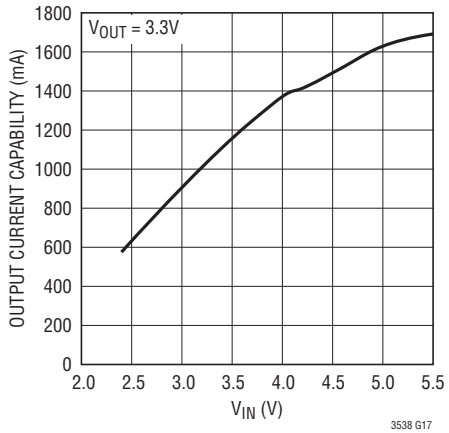
Oscillator Frequency vs Temperature



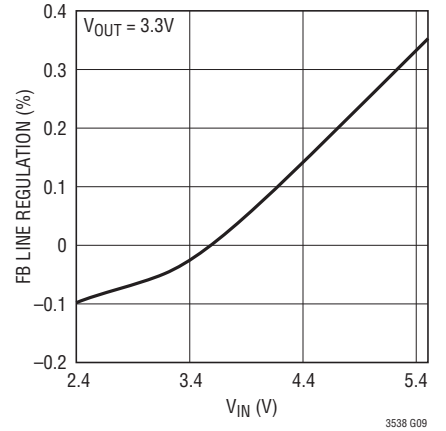
Feedback Voltage vs Temperature



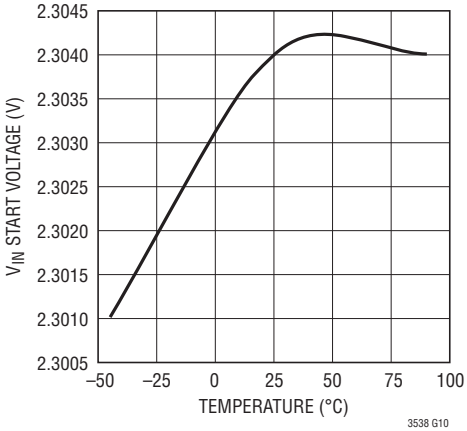
Maximum Output Current Capability vs V_{IN}



Feedback Voltage Line Regulation

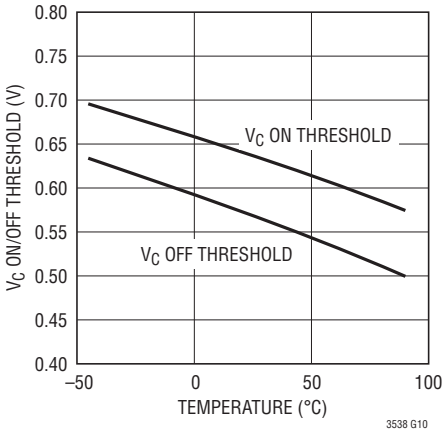


Minimum Start-Up Voltage

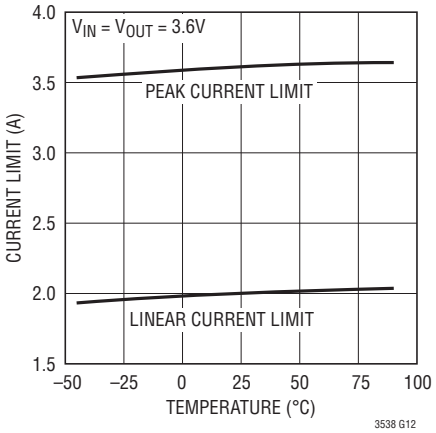


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C unless otherwise noted

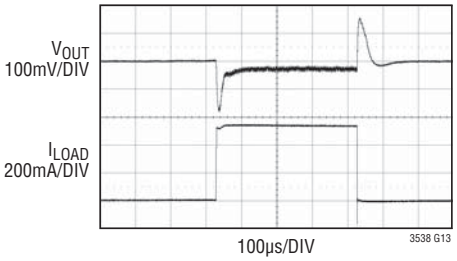
V_C On/Off Threshold vs Temperature



Current Limit vs Temperature

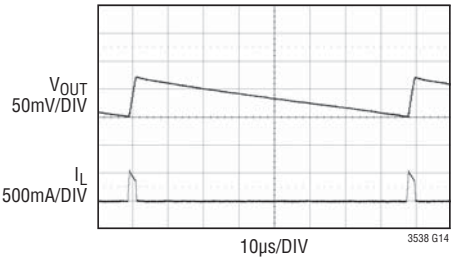


Load Transient in Fixed Frequency Mode



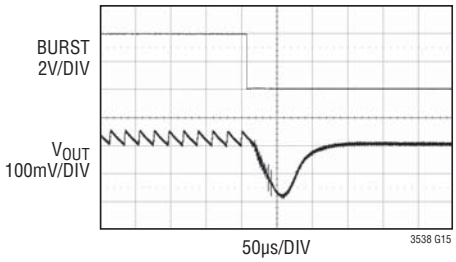
V_{IN} = 3.3V
V_{OUT} = 3.3V
I_{LOAD} = 0mA TO 500mA
C_{OUT} = 22µF X5R CERAMIC

Burst Mode Operation



V_{IN} = 3.3V
V_{OUT} = 3.3V
I_{LOAD} = 10mA
C_{OUT} = 22µF X5R CERAMIC

Transition From Burst Mode Operation to Fixed Frequency



V_{IN} = 3.3V
V_{OUT} = 3.3V
I_{LOAD} = 30mA
C_{OUT} = 22µF X5R CERAMIC

PIN FUNCTIONS

FB (Pin 1): Feedback Input to Error Amplifer. Connect resistive divider tap from V_{OUT} to this pin to set the output voltage. The output voltage can be adjusted from 1.8V to 5.25V. Referring to the Block Diagram the output voltage is given by:

$V_{OUT} = 1V \bullet (1 + R1/R2)$

V_C (Pin 2): Error Amplifier Output. A frequency compensation network should be connected between this pin and FB to compensate the loop. See Closing the Feedback Loop section of the datasheet for further information. Pulling V_C below 0.25V disables the LTC3538.

GND (Pin 3): Ground.

BURST (Pin 4): Burst Mode Select Input.

BURST = Low for fixed frequency PWM operation

BURST = High for Burst Mode operation

V_{OUT} (Pin 5): Power Supply Output. This pin should be connected to a low ESR output capacitor. The capacitor should be placed as close to the IC as possible and should have a short return to GND.

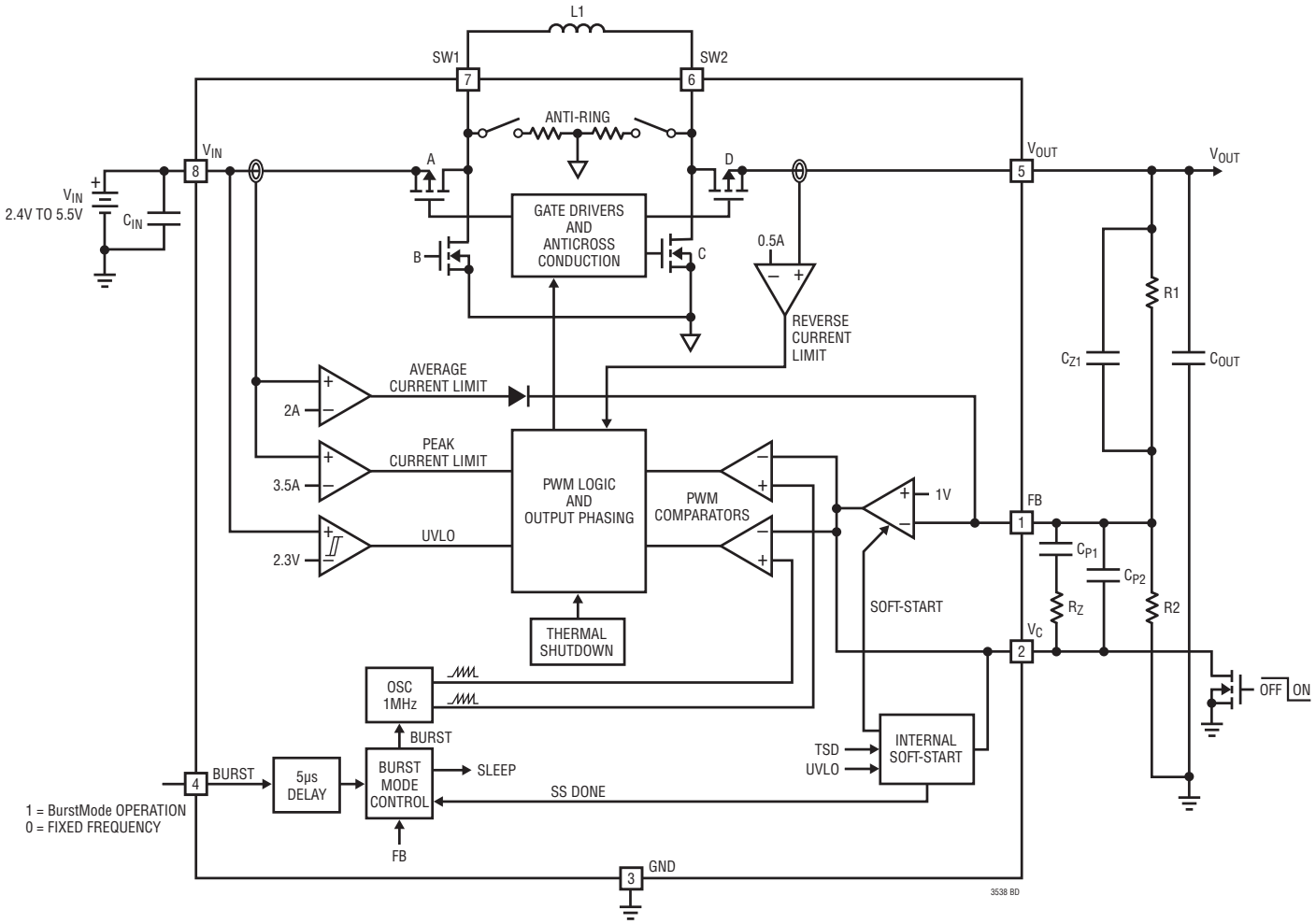
SW2 (Pin 6): Switch Pin where the Internal Switches C and D are Connected. An optional Schottky diode can be connected from SW2 to V_{OUT} for a moderate efficiency improvement. Keep the trace length as short as possible to minimize EMI.

SW1 (Pin 7): Switch Pin where the Internal Switches A and B are Connected. Connect an inductor from SW1 to SW2. An optional Schottky diode can be connected from SW1 to ground for a moderate efficiency improvement. Keep the trace length as short as possible to minimize EMI.

V_{IN} (Pin 8): Input Supply. This input provides power to the IC and also supplies current to switch A. A ceramic bypass capacitor (4.7µF or larger) is recommended as close to V_{IN} and GND as possible.

Exposed Pad (Pin 9): GND. The exposed pad must be electrically connected to the board ground for proper electrical and thermal performance.

BLOCK DIAGRAM



OPERATION

The LTC3538 provides high efficiency, low noise power for a wide variety of handheld electronic devices. The LTC proprietary topology allows input voltages above, below and equal to the output voltage through proper phasing of the four on-chip MOSFET switches. The error amplifier output voltage on V_C determines the output duty cycle of the switches. Since V_C is a filtered signal, it provides rejection of frequencies from well below the switching frequency. The low $R_{DS(ON)}$, low gate charge synchronous switches provide high frequency pulse width modulation control at high efficiency. High efficiency is achieved at light loads when Burst Mode operation is selected.

LOW NOISE FIXED FREQUENCY OPERATION

Operating Frequency

The operating frequency is internally fixed to 1MHz to maximize overall converter efficiency while minimizing external component size.

Error Amplifier

The error amplifier controls the duty cycle of the internal switches. The loop compensation components are configured around the amplifier to provide converter loop stability. Pulling down the output of the error amplifier (V_C) below 0.25V will disable the LTC3538. In shutdown the LTC3538 will draw only 1.5µA typical from the input supply. During normal operation the V_C pin should be allowed to float.

Soft-Start

The converter has an internal voltage mode soft-start circuit with a nominal duration of 1.5ms. The converter remains in regulation during soft-start and will therefore respond to output load transients that occur during this time. In addition, the output voltage risetime has minimal dependency on the size of the output capacitor or load. During soft-start, the converter is forced into PWM operation regardless of the state of the BURST pin.

Internal Current Limit

There are two current limit circuits in the LTC3538. The first is a high speed peak current limit amplifier that will shut off switch A once the input current exceeds ~ 3.5A typical. The delay to output of this amplifier is typically 50ns.

The second current limit sources current out of the FB pin to drop the output voltage once the input average current exceeds 2A typical. This method provides a closed loop means of clamping the input current. During conditions when V_{OUT} is near ground, such as during a short circuit or during start-up, this threshold is cut to 1A typical, providing a foldback feature to limit power dissipation. For this current limit feature to be most effective, the Thevenin resistance (typically the parallel combination of R1 and R2) from FB to ground should be greater than 100k.

Reverse Current Limit

During fixed frequency operation, the LTC3538 operates in forced continuous conduction mode. The reverse current limit comparator monitors the inductor current from the output through switch D. Should this negative inductor current exceed 500mA typical, the LTC3538 shuts off switch D.

Four-Switch Control

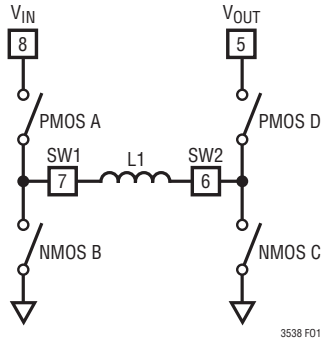


Figure 1. Simplified Diagram of Output Switches

Figure 1 shows a simplified diagram of how the four internal switches are connected to the inductor, V_{IN}, V_{OUT} and GND. Figure 2 shows the regions of operation for the LTC3538 as a function of the internal control voltage.

OPERATION

Depending on the V_C voltage, the LTC3538 will operate in either buck, buck-boost or boost mode. The four power switches are properly phased so the transfer between operating modes is continuous, smooth and transparent to the user. When V_{IN} approaches V_{OUT} the buck-boost region is entered, where the conduction time of the four-switch region is typically 150ns. Referring to Figures 1 and 2, the various regions of operation will now be described.

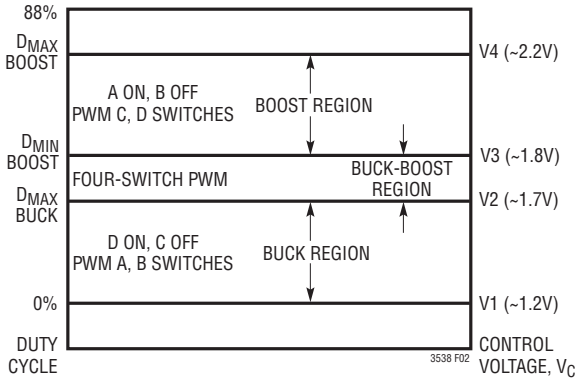


Figure 2. Switch Control vs Control Voltage, V_C

Buck Region ($V_{IN} > V_{OUT}$)

Switch D is always on and switch C is always off during this mode. When the control voltage, V_C, is above voltage V1, output A begins to switch. During the off time of switch A, synchronous switch B turns on for the remainder of the period. Switches A and B will alternate similar to a typical synchronous buck regulator. As the control voltage increases, the duty cycle of switch A increases until the maximum duty cycle of the converter in buck mode reaches D_{MAX_BUCK}, given by:

$$D_{MAX\_BUCK} = 100 - D4_{SW}\ \%$$

where $D4_{SW}$ = duty cycle % of the four switch range.

$$D4_{SW} = (150ns \bullet f) \bullet 100\ \%$$

where f = operating frequency, Hz.

Beyond this point the four switch, or buck-boost region is reached.

Buck-Boost or Four Switch ($V_{IN} \sim V_{OUT}$)

When the control voltage, V_C, is above voltage V2, switch pair AD remains on for duty cycle D_{MAX_BUCK}, and the switch pair AC begins to phase in. As switch pair AC phases in, switch pair BD phases out accordingly. When V_C reaches the edge of the buck-boost range, at voltage V3, the AC switch pair completely phase out the BD pair, and the boost phase begins at duty cycle $D4_{SW}$. The input voltage, V_{IN}, where the four switch region begins is given by:

$$V_{IN} = V_{OUT}(1 - D4_{SW}) \approx 0.85 \bullet V_{OUT}$$

The point at which the four-switch region ends is given by:

$$V_{IN} = \frac{V_{OUT}}{1 - D4_{SW}} V \approx 1.18 \bullet V_{OUT}$$

Boost Region ($V_{IN} < V_{OUT}$)

Switch A is always on and switch B is always off during this mode. When the control voltage, V_C, is above voltage V3, switch pair CD will alternately switch to provide a boosted output voltage. This operation is typical to a synchronous boost regulator. The maximum duty cycle of the converter is limited to 88% typical and is reached when V_C is above V4.

Burst Mode OPERATION

Burst Mode operation reduces quiescent current consumption of the LTC3538 at light loads and improves overall conversion efficiency, increasing battery life. During Burst Mode operation the LTC3538 delivers energy to the output until it is regulated and then goes into a sleep mode where the outputs are off and the quiescent current drops to 35µA. In this mode the output ripple has a variable frequency component that depends upon load current, and will typically be about 2% peak-to-peak. Burst Mode operation ripple can be reduced slightly by using more output capacitance. Another method of reducing Burst Mode operation ripple is to place a small feed-forward capacitor across the upper resistor in the V_{OUT} feedback divider network (as in Type III compensation).

OPERATION

During the period when the LTC3538 is delivering energy to the output, the peak inductor current will be equal to 800mA typical and the inductor current will terminate each cycle at zero current. In Burst Mode operation the maximum average output current that can be delivered while maintaining output regulation is given by:

$$I_{OUT\_BURST(BOOST)} = 0.25 \bullet \frac{V_{IN}}{V_{OUT}} A;\ V_{OUT} > V_{IN}$$

$$I_{OUT\_BURST(BUCK)} = 0.27A;\ V_{OUT} < V_{IN}$$

The maximum average Burst Mode output current that can be delivered in the four-switch buck-boost region is limited to the boost equation specified above.

INDUCTOR SELECTION

To achieve high efficiency, a low ESR inductor should be utilized for the converter. The inductor must have a saturation rating greater than the worst case average inductor current plus half the ripple current. The peak-to-peak current ripple will be larger in buck and boost mode than in the buck-boost region. The peak-to-peak inductor current ripple for each mode can be calculated from the following formulas, where f is the frequency (1MHz typical) and L is the inductance in µH.

$$\Delta I_{L,P\text{-}P,BUCK} = \frac{V_{OUT} \bullet \left(V_{IN} - V_{OUT}\right) / V_{IN}}{f \bullet L} A$$

$$\Delta I_{L,P\text{-}P,BOOST} = \frac{V_{OUT} \bullet \left(V_{OUT} - V_{IN}\right) / V_{OUT}}{f \bullet L} A$$

where f = frequency (1MHz typical), Hz

L = inductor, H

In addition to affecting output current ripple, the size of the inductor can also affect the stability of the feedback loop. In boost mode, the converter transfer function has a right half plane zero at a frequency that is inversely proportional to the value of the inductor. As a result, a large inductor can move this zero to a frequency low enough to degrade the phase margin of the feedback loop. It is recommended that the inductor value be chosen less than 10µH.

For high efficiency, choose a ferrite inductor with a high frequency core material to reduce core loses. The inductor should have low ESR (equivalent series resistance) to reduce the I^2R losses, and must be able to handle the peak inductor current without saturating. Molded chokes or chip inductors usually do not have enough core to support the peak inductor currents in the 1A to 2A region. To minimize radiated noise, use a shielded inductor. See Table 1 for a suggested list of inductor suppliers.

Output Capacitor Selection

The bulk value of the output filter capacitor is selected to reduce the ripple due to charge into the capacitor each cycle. The steady state ripple due to charge is given by:

$$\Delta V_{P\text{-}P,\ BOOST} = I_{LOAD} \bullet (V_{OUT} - V_{IN})/(C_{OUT} \bullet V_{OUT} \bullet f)V$$

$$\Delta V_{P\text{-}P,BUCK} = (V_{IN} - V_{OUT}) \bullet V_{OUT}/(8 \bullet L \bullet V_{IN} \bullet C_{OUT} \bullet f^2)V$$

where C_{OUT} = output filter capacitor, F

I_{LOAD} = Output load current, A

Table 1. Inductor Vendor Information

SUPPLIER	PHONE	FAX	WEB SITE
Coilcraft	(847) 639-6400	(847) 639-1469	www.coilcraft.com
CoEv Magnetics	(800) 227-7040	(650) 361-2508	www.tycoelectronics.com
Murata	(814) 237-1431 (800) 831-9172	(814) 238-0490	www.murata.com
Sumida	USA: (847) 956-0666 Japan: 81 (3) 3607-5111	USA: (847) 956-0702 Japan: 81(3) 3607-5144	www.sumida.com
TDK	(847) 803-6100	(847) 803-6296	www.component.tdk.com
TOKO	(847) 297-0070	(847) 699-7864	www.tokoam.com

OPERATION

Since the output current is discontinuous in boost mode, the ripple in this mode will generally be much larger than the magnitude of the ripple in buck mode.

Minimizing solution size is usually a priority. Please be aware that ceramic capacitors can exhibit a significant reduction in effective capacitance when a bias is applied. The capacitors exhibiting the highest reduction are those packaged in the smallest case size.

Input Capacitor Selection

Since V_{IN} is the supply voltage for the IC it is recommended to place at least a 4.7µF, low ESR ceramic bypass capacitor close to V_{IN} and GND. It is also important to minimize any stray resistance from the converter to the battery or other power source.

Optional Schottky Diodes

Schottky diodes across the synchronous switches B and D are not required, but do provide a lower drop during the break-before-make time (typically 15ns), thus improving efficiency. Use a surface mount Schottky diode such as an MBRM120T3 or equivalent. Do not use ordinary rectifier diodes since their slow recovery times will compromise efficiency.

Table 2. Capacitor Vendor Information

SUPPLIER	PHONE	FAX	WEB SITE
AVX	(803) 448-9411	(803) 448-1943	www.avxcorp.com
Sanyo	(619) 661-6322	(619) 661-1055	www.sanyovideo.com
Taiyo Yuden	(408) 573-4150	(408) 573-4159	www.t-yuden.com
TDK	(847) 803-6100	(847) 803-6296	www.component.tdk.com

Shutdown MOSFET Selection

A discrete external N-channel MOSFET, open-drain pull-down device or other suitable means can be used to put the part in shutdown by pulling V_C below 0.25V. Since the error amplifier sources 13µA typically when active and 1.5µA in shutdown, a relatively high resistance pull-down device can be used to pull V_C below 0.25V. More importantly, leakage and parasitic capacitance need to be minimized. During start-up, 1.5µA is typically sourced from V_C. The leakage of an external pull-down device and compensation components tied to V_C, must therefore be minimized to ensure proper start-up. Capacitance from the pull-down device should also be minimized as it can affect converter stability. An N-channel MOSFET such as the FDV301N or similar is recommended if an external discrete N-channel MOSFET is needed.

PCB Layout Considerations

The LTC3538 switches large currents at high frequencies. Special care should be given to the PCB layout to ensure stable, noise-free operation. Figure 3 depicts the recommended PCB layout to be utilized for the LTC3538. A few key guidelines follow:

1. All circulating current paths should be kept as short as possible. This can be accomplished by keeping the routes to all components (except the FB divider network) in Figure 3 as short and as wide as possible. Capacitor ground connections should via down to the ground plane in the shortest route possible. The bypass capacitor on V_{IN} should be placed as close to the IC as possible and should have the shortest possible paths to ground.

2. The small signal ground pad (GND) should have a single point connection to the power ground. A convenient way to achieve this is to short this pin directly to the Exposed Pad as shown in Figure 3.

3. The components in bold and their connections should all be placed over a complete ground plane.

4. To prevent large circulating currents from disrupting the output voltage sensing, the ground for the resistor divider should be returned directly to the small signal ground (GND) as shown.

5. Use of vias in the attach pad will enhance the thermal environment of the converter especially if the vias extend to a ground plane region on the exposed bottom surface of the PCB.

OPERATION

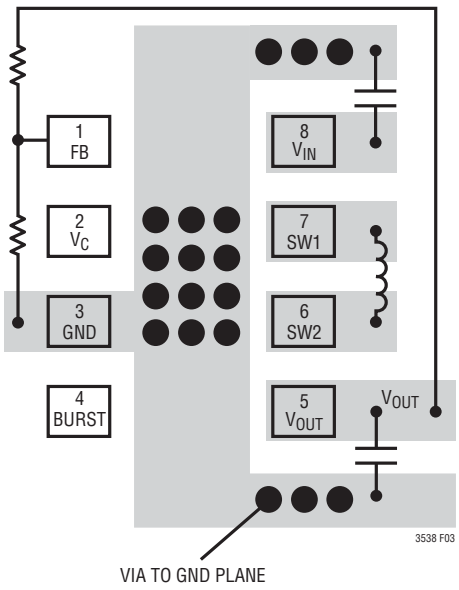


Figure 3. LTC3538 Recommended PCB Layout

Closing the Feedback Loop

The LTC3538 incorporates voltage mode PWM control. The control to output gain varies with operation region (buck, boost, buck-boost), but is usually no greater than 15. The output filter exhibits a double pole response, as given by:

$$f_{FILTER\_POLE} = \frac{1}{2 \bullet \pi \bullet \sqrt{L \bullet C_{OUT}}} Hz$$

(in buck mode)

$$f_{FILTER\_POLE} = \frac{V_{IN}}{2 \bullet V_{OUT} \bullet \pi \bullet \sqrt{L \bullet C_{OUT}}} Hz$$

(in boost mode)

where L is in Henries and C_{OUT} is in Farads.

The output filter zero is given by:

$$f_{FILTER\_ZERO} = \frac{1}{2 \bullet \pi \bullet R_{ESR} \bullet C_{OUT}} Hz$$

where R_{ESR} is the equivalent series resistance of the output capacitor.

A troublesome feature in boost mode is the right-half plane zero (RHP), given by:

$$f_{RHPZ} = \frac{V_{IN}^2}{2 \bullet \pi \bullet I_{OUT} \bullet L \bullet V_{OUT}} Hz$$

The loop gain is typically rolled off before the RHP zero frequency.

A simple Type I compensation network can be incorporated to stabilize the loop, but at a cost of reduced bandwidth and slower transient response. To ensure proper phase margin using Type I compensation, the loop must be crossed over a decade before the LC double pole. Referring to Figure 4, the unity-gain frequency of the error amplifier with the Type I compensation is given by:

$$f_{UG} = \frac{1}{2 \bullet \pi \bullet R1 \bullet C_{P1}} Hz$$

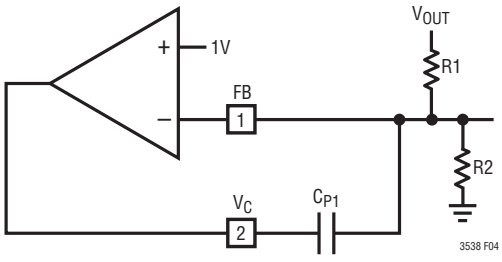


Figure 4. Error Amplifier with Type I Compensation

OPERATION

Most applications demand an improved transient response to allow a smaller output filter capacitor. To achieve a higher bandwidth, Type III compensation is required, providing two zeros to compensate for the double-pole response of the output filter. Referring to Figure 5, the location of the poles and zeros are given by:

$$f_{POLE1} \cong \frac{1}{2 \bullet \pi \bullet 32e^3 \bullet R1 \bullet C_{P1}} Hz$$

(which is extremly close to DC)

$$f_{ZERO1} = \frac{1}{2 \bullet \pi \bullet R_Z \bullet C_{P1}} Hz$$

$$f_{ZERO2} = \frac{1}{2 \bullet \pi \bullet R1 \bullet C_{Z1}} Hz$$

$$f_{POLE2} = \frac{1}{2 \bullet \pi \bullet R_Z \bullet C_{P2}} Hz$$

where resistance is in Ohms and capacitance is in Farads.

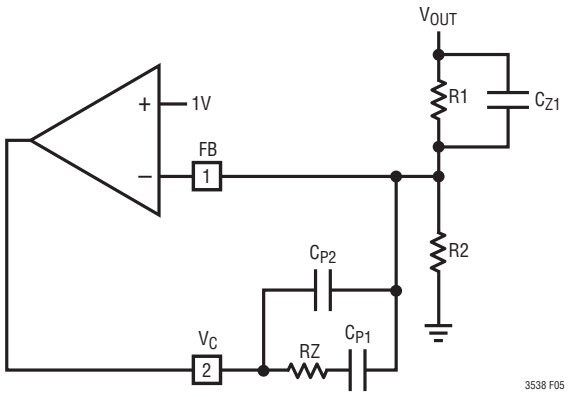
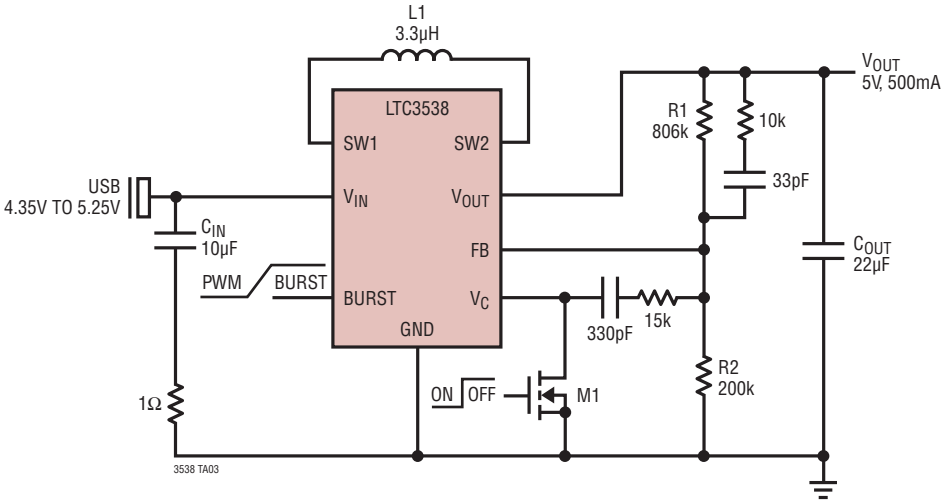


Figure 5. Error Amplifier with Type III Compensation

TYPICAL APPLICATION

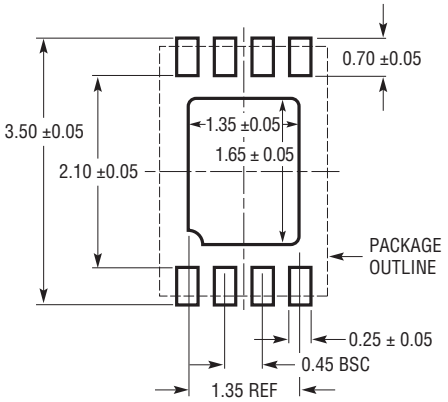
High Efficiency 5V/500mA from USB Input



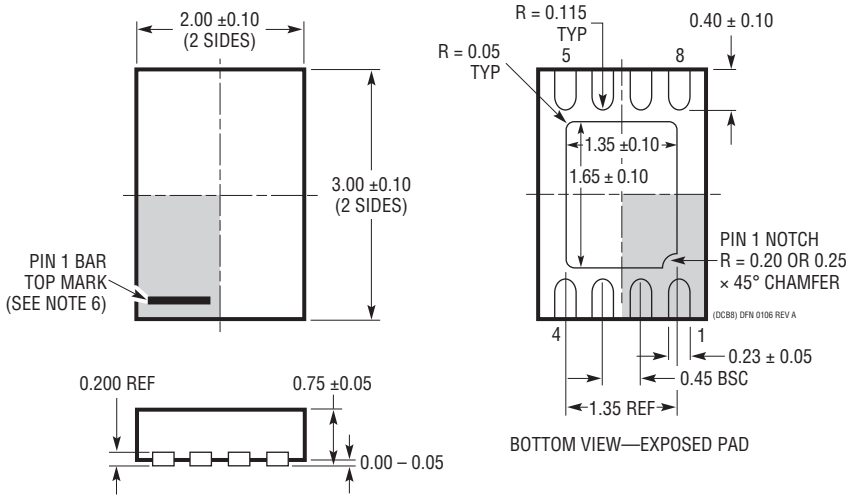
C_{IN}: TAIYO YUDEN JMK212BJ106MG
C_{OUT}: TAIYO YUDEN JMK325BJ226MM
L1: SUMIDA CDRH2D18/HP-3R3NC
M1: µP OPEN DRAIN I/O OR FAIRCHILD FDV301N

PACKAGE DESCRIPTION

DCB Package
8-Lead Plastic DFN (2mm × 3mm)
(Reference LTC DWG # 05-08-1718 Rev A)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3407	600mA (I_{OUT}), 1.5MHz Dual Synchronous Step-Up DC/DC Converter	V_{IN}: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.8V I_Q = 40µA, I_{SD} ≤1µA, SC70 Package
LTC3410	300mA (I_{SW}), 2.25MHz Synchronous Step-Down DC/DC Converter in SC70	V_{IN}: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.8V I_Q = 26µA, I_{SD} ≤1µA, MS Package
LTC3411	1.25A (I_{OUT}), 4MHz Synchronous Step-Down DC/DC Converter	V_{IN}: 2.625V to 5.5V, $V_{OUT(MIN)}$ = 0.8V I_Q = 62µA, I_{SD} ≤1µA, MS Package
LTC3412	2.5A (I_{OUT}), 4MHz Synchronous Step-Down DC/DC Converter	V_{IN}: 2.625V to 5.5V, $V_{OUT(MIN)}$ = 0.8V I_Q = 62µA, I_{SD} ≤1µA, TSSOP16E Package
LTC3421	3A (I_{SW}), 3MHz Synchronous Step-Up DC/DC Converter	V_{IN}: 0.5V to 4.5V, $V_{OUT(MAX)}$ = 5.25V I_Q = 12µA, I_{SD} <1µA, QFN Package
LTC3422	1.5A (I_{SW}), 3MHz Synchronous Step-Up DC/DC Converter with Output Disconnect	V_{IN}: 0.5V to 4.5V, $V_{OUT(MAX)}$ = 5.25V I_Q = 25µA, I_{SD} <1µA, DFN Package
LTC3425	5A (I_{SW}), 8MHz Multiphase Synchronous Step-Up DC/DC Converter	V_{IN}: 0.5V to 4.5V, $V_{OUT(MAX)}$ = 5.25V I_Q = 12µA, I_{SD} <1µA, QFN Package
LTC3427	500mA (I_{SW}), 1.25MHz Step-Up DC/DC Converter with Output Disconnect in 2mm × 2mm DFN	V_{IN}: 1.8V to 5V, $V_{OUT(MAX)}$ = 5.25V, I_Q = 350µA, I_{SD} <1µA, DFN Package
LTC3429	600mA (I_{SW}), 500KHz Synchronous Step-Up DC/DC Converter	V_{IN}: 0.5V to 4.4V, $V_{OUT(MAX)}$ = 5V I_Q = 20µA, I_{SD} <1µA, ThinSOT™ Package
LTC3440	600mA (I_{OUT}), 2MHz Synchronous Buck-Boost DC/DC Converter	V_{IN}: 2.5V to 5.5V, V_{OUT}: 2.5V to 5.5V I_Q = 25µA, I_{SD} <1µA, MS, DFN Package
LTC3441/LTC3443	1.2A (I_{OUT}), Synchronous Buck-Boost DC/DC Converters, LTC3441(1MHz), LTC3443 (600kHz)	V_{IN}: 2.5V to 5.5V, V_{OUT}: 2.4V to 5.25V I_Q = 25µA, I_{SD} <1µA, DFN Package
LTC3442	1.2A (I_{OUT}), 2MHz Synchronous Buck-Boost DC/DC Converter	V_{IN}: 2.4V to 5.5V, V_{OUT}: 2.4V to 5.25V I_Q = 28µA, I_{SD} <1µA, MS Package
LTC3522	400mA, Synchronous Buck-Boost and 200mA Buck Converters	V_{IN}: 2.4V to 5.5V, V_{OUT} Buck-Boost: 2.2V to 5.25V, I_Q = 25µA, I_{SD} <1µA, DFN Package
LTC3525	400mA (I_{SW}), Synchronous Step-Up DC/DC Converter with Output Disconnect	V_{IN}: 0.5V to 4.5V, V_{OUT} = 3, 3.3, 5V I_Q = 7µA, I_{SD} <1µA, SC70 Package
LTC3526/LTC3526B	500mA (I_{SW}), 1MHz Synchronous Step-Up DC/DC Converter with Output Disconnect in 2mm × 2mm DFN	V_{IN}: 0.5V to 4.5V, V_{OUT}: 1.6V to 5.25V I_Q = 9µA, I_{SD} <1µA, DFN Package
LTC3530	600mA (I_{OUT}), 2MHz Synchronous Buck-Boost DC/DC Converter	V_{IN}: 1.8V to 5.5V, V_{OUT}: 1.6V to 5.25V I_Q = 40µA, I_{SD} <1µA, DFN, MS Packages
LTC3531	200mA (I_{OUT}) Synchronous Buck-Boost DC/DC Converter	V_{IN}: 1.8V to 5.5V, V_{OUT}: 2V to 5V I_Q = 16µA, I_{SD} <1µA, DFN, ThinSOT Packages
LTC3532	500mA (I_{OUT}), 2MHz Synchronous Buck-Boost DC/DC Converter	V_{IN}: 2.4V to 5.5V, V_{OUT}: 2.2V to 5.25V I_Q = 35µA, I_{SD} <1µA, DFN, MS Packages
LTC3533	2A (I_{OUT}), 2MHz Synchronous Buck-Boost DC/DC Converter	V_{IN}: 1.8V to 5.5V, V_{OUT}: 1.6V to 5.25V I_Q = 40µA, I_{SD} <1µA, DFN Package

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Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900 • FAX: (408) 434-0507 • www.linear.com

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