8-BIT SHIFT REGISTER (SERIAL INPUT, 3S PARALLEL OUTPUT WITH LATCHES)

DESCRIPTION

SC74HC595 utilizes advanced CMOS technology, and has 8-bit shift register with serial input, serial/parallel output and 8-bit tri-state output flip-latch. The pin configuration is in accord with the 54LS/74LS series, and the operating speed is similar to 54LS/74LS. This circuit has the protecting circuit for all the inputs and outputs to avoid the damage caused by the static discharge. And it has the ability of driving load and features high noise immunity.
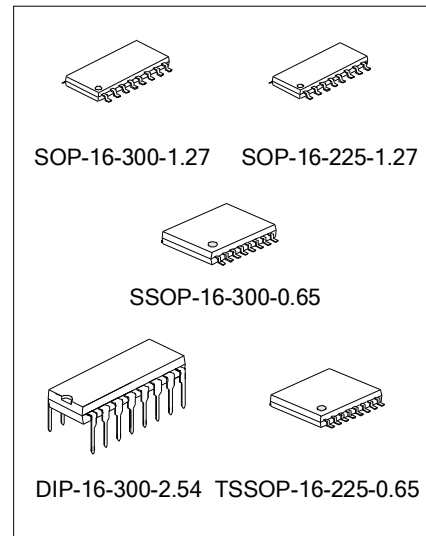
The register and flip-latch both have separate clock inputs (SCK and RCK). The serial input data (IS) is stored into register at the rising edge of SCK; the data of register is stored into flip-latch at the rising edge of RCK. The low level of clear port ($\overline{SCLR}$) only reset the register, and is no effect to flip-latch. When the control enable ($\overline{G}$) is high level, the parallel-out is level Z.

SOP-16-300-1.27   SOP-16-225-1.27

SSOP-16-300-0.65

DIP-16-300-2.54   TSSOP-16-225-0.65

FEATURES

* Wide operating voltage range   2~6V
* Low input current   1µA
* High output driving ability   15 LS-TTL loads
* High operating speed(Typical) f_{max}=55MHz (V_{CC}=5V)
* Low supply current   80µA

ORDERING INFORMATION

Device	Package
SC74HC595	DIP-16-300-2.54
SC74HC595A	SOP-16-225-1.27
SC74HC595B	SOP-16-300-1.27
SC74HC595C	TSSOP-16-225-0.65
SC74HC595D	SSOP-16-300-0.65

APPLICATIONS

* LED screen

RECOMANDED OPERATING CONDITIONS

Characteristics	Symbol	Ratings		Unit
Power Supply Voltage	V_{CC}	2~6		V
Input Voltage	V_{IN}	0~V_{CC}		V
Output Voltage	V_{OUT}	0~V_{CC}		V
Operating Temperature	T_{opr}	-40~+85		°C
Input Rise and Fall Time	T_r, T_f	V_{CC} =2.0V	0~1000	ns
		V_{CC} =4.5V	0~500	ns
		V_{CC} =6.0V	0~400	ns

DC ELECTRICAL CHARACTERISTICS (Tamb=25°C)

Characteristics	Symbol	Testing conditions		Min.	Typ.	Max.	Unit
		Vcc(V)	Conditions				
High Level Input Voltage	V_{IH}	2.0		1.5	--	--	V
		4.5		3.15	--	--	
		6.0		4.2	--		
Low Level Input Voltage	V_{IL}	2.0		--	--	0.5	V
		4.5		--	--	1.35	
		6.0		--	--	1.8	
High Level Output Voltage (OH')	V_{OH}	2.0	$V_{IN}=V_{IH}$ or V_{IL}, $I_O=-20\mu A$	1.9	2.0	--	V
		4.5		4.4	4.5	--	
		6.0		5.9	6.0	--	
		4.5	$I_O=-4.0mA$	4.18	4.31	--	
		6.0	$I_O=-5.2mA$	5.68	5.8	--	
High Level Output Voltage (QA~QH)	V_{OH}	2.0	$V_{IN}=V_{IH}$ or V_{IL}, $I_O=-20\mu A$	1.9	2.0	--	V
		4.5		4.4	4.5	--	
		6.0		5.9	6.0	--	
		4.5	$I_O=-6.0mA$	4.18	4.31	--	
		6.0	$I_O=-7.8mA$	5.68	5.8	--	
Low Level Output Voltage (OH')	V_{OL}	2.0	$V_{IN}=V_{IH}$ or V_{IL}, $I_O=20\mu A$	--	0.0	0.1	V
		4.5		--	0.0	0.1	
		6.0		--	0.0	0.1	
		4.5	$I_O=4.0mA$	--	0.17	0.26	
		6.0	$I_O=5.2mA$	--	0.18	0.26	
Low Level Output Voltage (QA~QH)	V_{OL}	2.0	$V_{IN}=V_{IH}$ or V_{IL}, $I_O=20\mu A$	--	0.0	0.1	V
		4.5		--	0.0	0.1	
		6.0		--	0.0	0.1	
		4.5	$I_O=6.0mA$	--	0.17	0.26	
		6.0	$I_O=7.8mA$	--	0.18	0.26	
Input Leakage Current	I_I	6.0	$V_{IN}=V_{CC}$ or GND	--	--	±0.1	μA
Tri-state Output Current	I_{OZ}	6.0	$V_{IN}=V_{IH}$ or V_{IL} $V_{OUT}=V_{CC}$ or GND	--	--	±0.5	μA
Quiescent Supply Current	I_{CC}	6.0	$V_{IN}=V_{CC}$ or GND	-	--	4	μA

DC ELECTRICAL CHARACTERISTICS (Tamb=-40~85℃)

Characteristics	Symbol	Testing conditions		Min.	Typ.	Max.	Unit
		Vcc(V)	Conditions				
High Level Input Voltage	V_{IH}	2.0		1.5	--	--	V
		4.5		3.15	--	--	
		6.0		4.2	--	--	
Low Level Input Voltage	V_{IL}	2.0		--	--	0.5	V
		4.5		--	--	1.35	
		6.0		--	--	1.8	
High Level Output Voltage (OH')	V_{OH}	2.0	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$	1.9	--	--	V
		4.5		4.4	--	--	
		6.0		5.9	--	--	
		4.5	$I_O=-4.0mA$	4.13	--	--	
		6.0	$I_O=-5.2mA$	5.63	--	--	
High Level Output Voltage (QA~QH)	V_{OH}	2.0	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$	1.9	--	--	V
		4.5		4.4	--	--	
		6.0		5.9	--	--	
		4.5	$I_O=-6.0mA$	4.13	--	--	
		6.0	$I_O=-7.8mA$	5.63	--	--	
Low Level Output Voltage (OH')	V_{OL}	2.0	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$	--	--	0.1	V
		4.5		--	--	0.1	
		6.0		--	--	0.1	
		4.5	$I_O=4.0mA$	--	--	0.33	
		6.0	$I_O=5.2mA$	--	--	0.33	
Low Level Output Voltage (QA~QH)	V_{OL}	2.0	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$	--	--	0.1	V
		4.5		--	--	0.1	
		6.0		--	--	0.1	
		4.5	$I_O=6.0mA$	--	--	0.33	
		6.0	$I_O=7.8mA$	--	--	0.33	
Input Leakage Current	I_I	6.0	$V_{IN}=V_{CC}$ or GND	--	--	±0.1	μA
Tri-state Output Current	I_{OZ}	6.0	$V_{IN}=V_{IH}$ or V_{IL} $V_{OUT}=V_{CC}$ or GND	--	--	±0.5	μA
Quiescent Supply Current	I_{CC}	6.0	$V_{IN}=V_{CC}$ or GND	--	--	4	μA

AC ELECTRICAL CHARACTERISTICS(C$_L$=50pF，INPUT T$_r$=Tf=6ns，T$_{amb}$=25°C)

Characteristics	Symbol	Testing conditions			Min.	Typ.	Max.	Unit
		Vcc(V)	CL(pF)					
Output Transition Time (Qn)	tTLH tTHL	2.0	50		--	25	60	ns
		4.5			--	7	12	
		6.0			--	6	10	
Output Transition Time (QH')	tTLH tTHL	2.0	50		--	30	75	ns
		4.5			--	8	15	
		6.0			--	7	13	
Propagation Delay Time(SCK-QH')	tPLH tPHL	2.0	50		--	45	125	ns
		4.5			--	15	25	
		6.0			--	13	21	
Propagation Delay Time (SCLR-QH')	tPLH tPHL	2.0	50		--	60	175	ns
		4.5			--	18	35	
		6.0			--	15	30	
Propagation Delay Time (RCK-QN)	tPLH tPHL	2.0	50		--	60	150	ns
		4.5			--	20	30	
		6.0			--	17	26	
		2.0	150		--	75	190	ns
		4.5			--	25	38	
		6.0			--	22	32	
Tri-state Output Enable Time	tPZL tPZH	2.0	50	RL=1kΩ	--	45	135	ns
		4.5			--	15	27	
		6.0			--	13	23	
		2.0	150	RL=1kΩ	--	60	175	ns
		4.5			--	20	35	
		6.0			--	17	30	
Tri-state Output Disable Time	tPLZ tPHZ	2.0	50	RL=1kΩ	--	30	150	ns
		4.5			--	15	30	
		6.0			--	14	26	
Maximum Clock	fMAX	2.0	50		6.0	17	--	ns
		4.5			30	50	--	
		6.0			35	59	--	
		2.0	150		5.2	14	--	ns
		4.5			26	40	--	
		6.0			31	45	--	

(To be continued)

(Continued)

Characteristics	Symbol	Testing conditions			Min.	Typ.	Max.	Unit
		Vcc(V)	CL(pF)					
Minimum Pulse Width (SCK, RCK)	tW(H)	2.0	50		--	17	75	ns
		4.5			--	6	15	
		6.0			--	6	13	
Minimum Pulse Width (SCLR)	tW(L)	2.0	50		--	20	75	ns
		4.5			--	6	15	
		6.0			--	6	13	
Minimum Set-up Time (SI-SCK)	ts	2.0	50		--	25	50	ns
		4.5			--	5	10	
		6.0			--	4	9	
Minimum Set-up Time (SCK-RCK)	ts	2.0	50		--	35	75	ns
		4.5			--	8	15	
		6.0			--	6	13	
Minimum Set-up Time (SCLR-RCK)	ts	2.0	50		--	40	100	ns
		4.5			--	10	20	
		6.0			--	7	17	
Minimum Hold Time	tH	2.0	50		--	--	0	ns
		4.5			--	--	0	
		6.0			--	--	0	
Minimum Clear Time	tREM	2.0	50		--	15	50	ns
		4.5			--	3	10	
		6.0			--	3	9	
Input Capacitance	CIN				--	5	10	pF
Power Dissipation Capacitance	CPD(*)				--	184		pF

(*): CPD is defined as the internal equivalent capacitance of the IC. It is calculated from the operating current without load; and the average operating current can be obtained by the equation: I_{CC} (opr) =$C_{PD}*V_{CC}*f_{IN}+I_{CC}$.

AC ELECTRICAL CHARACTERISTICS(C$_L$=50pF，INPUT T$_r$=Tf=6ns，Tamb=-40~85°C)

Characteristics	Symbol	Testing conditions			Min.	Typ.	Max.	Unit
		Vcc(V)	CL(pF)					
Output Transition Time (Qn)	tTLH tTHL	2.0	50		--	--	75	ns
		4.5			--	--	15	
		6.0			--	--	13	
Output Transition Time (QH')	tTLH tTHL	2.0	50		--	--	95	ns
		4.5			--	--	19	
		6.0			--	--	16	
Propagation Delay Time (SCK-QH')	tPLH tPHL	2.0	50		--	--	155	ns
		4.5			--	--	31	
		6.0			--	--	66	
Propagation Delay Time (SCLR-QH')	tPLH tPHL	2.0	50		--	--	220	ns
		4.5			--	--	44	
		6.0			--	--	37	
Propagation Delay Time (RCK-QN)	tPLH tPHL	2.0	50		--	--	190	ns
		4.5			--	--	38	
		6.0			--	--	32	
		2.0	150		--	--	240	ns
		4.5			--	--	48	
		6.0			--	--	41	
Tri-state Output Enable Time	tPZL tPZH	2.0	50	R$_L$=1kΩ	--	--	170	ns
		4.5			--	--	34	
		6.0			--	--	29	
		2.0	150	R$_L$=1kΩ	--	--	220	ns
		4.5			--	--	44	
		6.0			--	--	37	
Tri-state Output Disable Time	tPLZ tPHZ	2.0	50	R$_L$=1kΩ	--	--	190	ns
		4.5			--	--	38	
		6.0			--	--	32	
Maximum Clock	fMAX	2.0	50		4.8	--	--	ns
		4.5			24	--	--	
		6.0			28	--	--	
		2.0	150		4.2	--	--	ns
		4.5			21	--	--	
		6.0			25	--	--	

(To be continued)

Silan
Microelectronics

(Continued)

Characteristics	Symbol	Testing conditions			Min.	Typ.	Max.	Unit
		Vcc(V)	CL(pF)					
Minimum Pulse Width (SCK, RCK)	tW(H)	2.0	50		--	--	95	ns
		4.5			--	--	19	
		6.0			--	--	16	
Minimum Pulse Width ($\overline{SCLR}$)	tW(L)	2.0	50		--	--	95	ns
		4.5			--	--	19	
		6.0			--	--	16	
Minimum Set-up Time (SI-RCK)	ts	2.0	50		--	--	65	ns
		4.5			--	--	13	
		6.0			--	--	11	
Minimum Set-up Time (SCK-RCK)	ts	2.0	50		--	--	95	ns
		4.5			--	--	19	
		6.0			--	--	16	
Minimum Set-up Time ($\overline{SCLR}$-RCK)	ts	2.0	50		--	--	125	ns
		4.5			--	--	25	
		6.0			--	--	21	
Minimum Hold Time	tH	2.0	50		--	--	0	ns
		4.5			--	--	0	
		6.0			--	--	0	
Minimum Clear Time	tREM	2.0	50		--	--	65	ns
		4.5			--	--	13	
		6.0			--	--	11	
Input Capacitance	CIN				--	--	10	pF
Power Dissipation Capacitance	CPD(*)				--	--	--	pF

(*): CPD is defined as the internal equivalent capacitance of the IC. It is calculated from the operating current without load; and the average operating current can be obtained by the equation: I_{CC} (opr) $= C_{PD} * V_{CC} * f_{IN} + I_{CC}$.
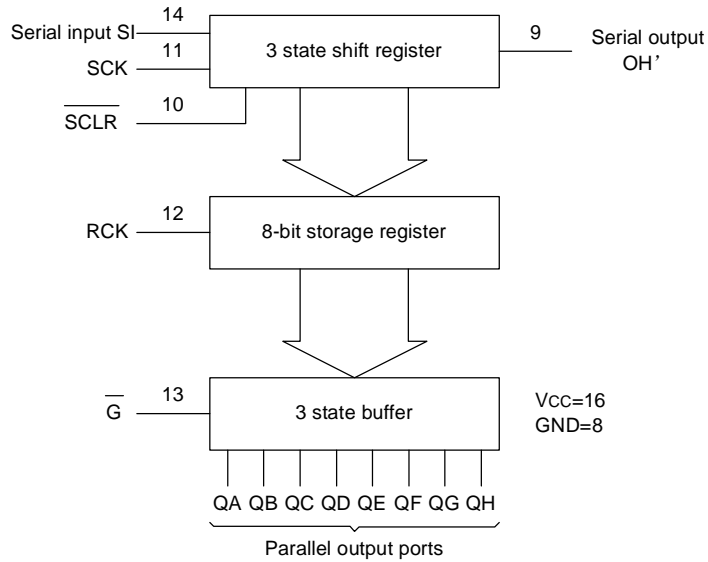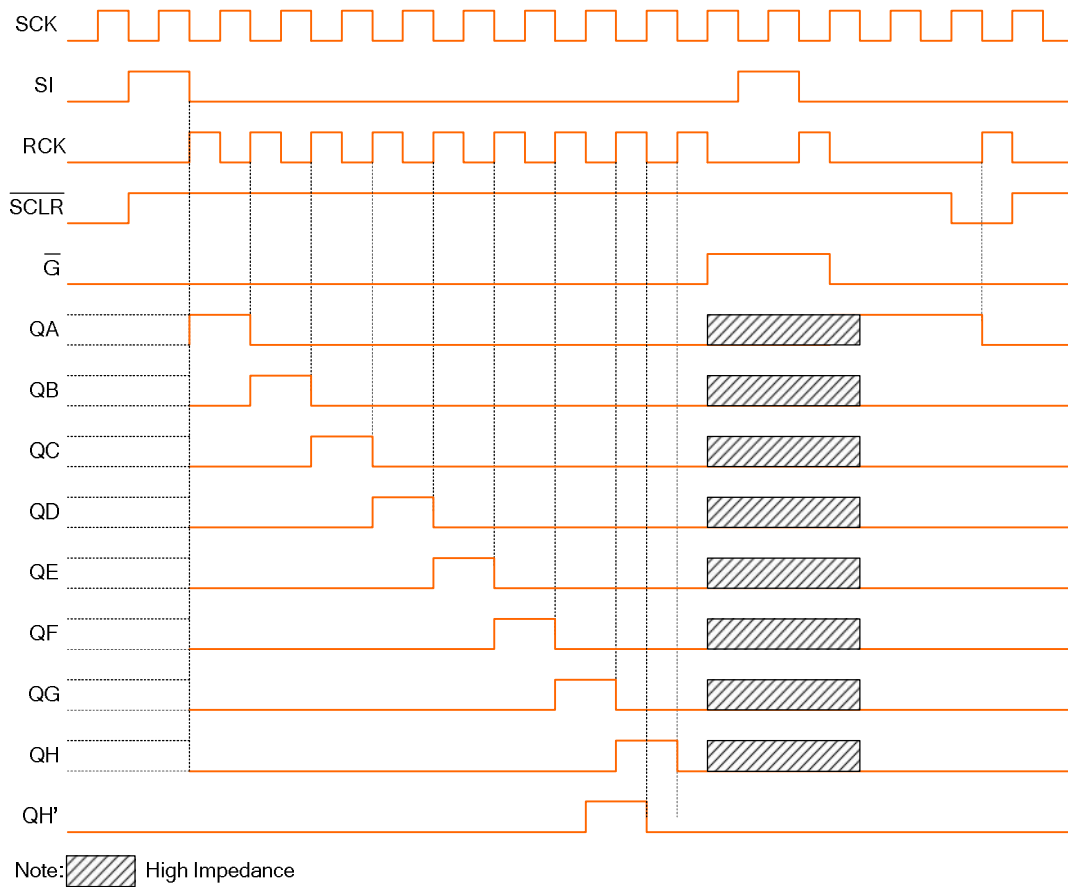
PIN CONFIGURATION

```
        ┌───┐ ┌───┐
   QB ─(1)       (16)─ VCC
   QC ─(2)       (15)─ QA
   QD ─(3)       (14)─ SI
   QE ─(4)  S    (13)─ G̅
   QF ─(5)  C    (12)─ RCK
   QG ─(6)  7    (11)─ SCK
            4
   QH ─(7)  H    (10)─ S̅C̅L̅R̅
           C
  GND ─(8)  5    (9)─ QH'
        └────────┘
        9
        5
```
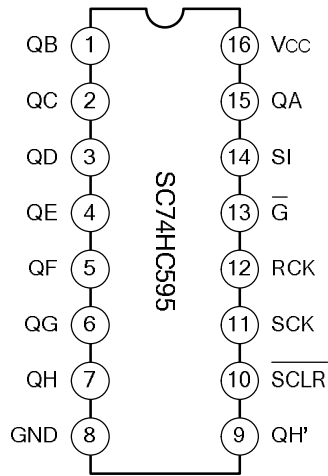
PIN DESCRIPTION

Pin no.	Name	I/O	Pin description
1~7, 15	QA ~ QH	O	Parallel data output
9	QH'	O	Serial data output
10	S̅C̅L̅R̅	I	Reset signal of register
11	SCK	I	Register clock
13	G̅	I	Data output enable
14	SI	I	Serial data input
12	RCK	I	Flip-latch clock
8	GND	I/O	Ground
16	VCC	I/O	Power supply

LOGIC DIAGRAM

Serial input SI — 14	
SCK — 11	**3 state shift register** → 9 — Serial output OH'
$\overline{SCLR}$ — 10	

RCK — 12 — **8-bit storage register**

$\overline{G}$ — 13 — **3 state buffer** — Vcc=16, GND=8

QA QB QC QD QE QF QG QH

Parallel output ports

TIMING CHART

SCK

SI

RCK

$\overline{SCLR}$

$\overline{G}$

QA

QB

QC

QD

QE

QF

QG

QH

QH'

Note: ▨ High Impedance

TRUTH TABLE

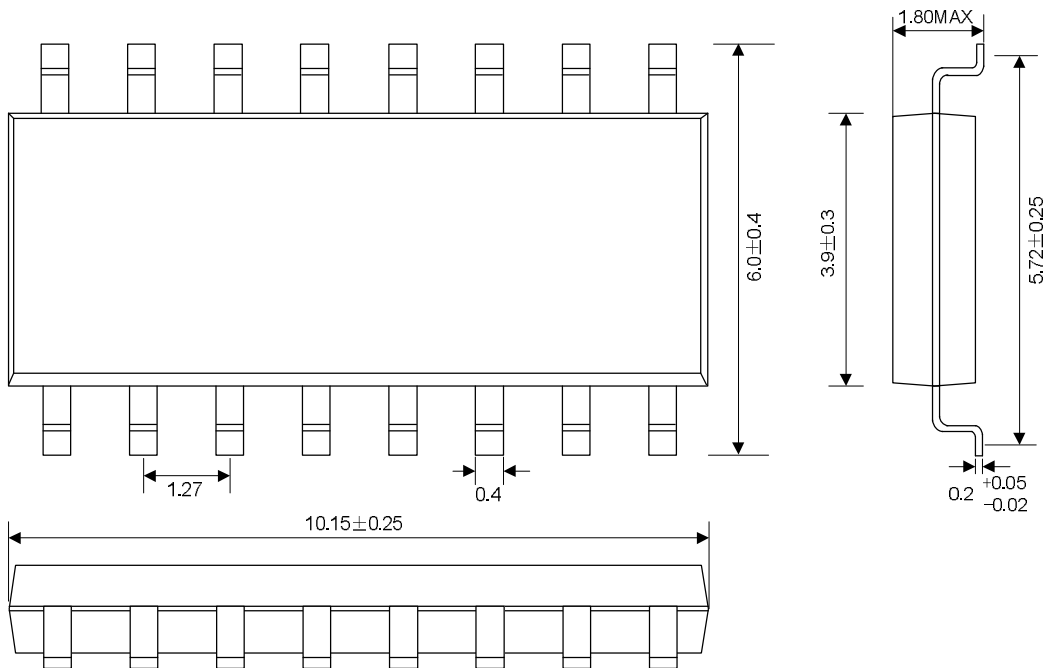| Input					Output
SI	**SCK**	$\overline{\text{SCLR}}$	**RCK**	$\overline{\text{G}}$	
X	X	X	X	H	QA ~QH outputs disable
X	X	X	X	L	QA ~QH outputs enable
X	X	L	X	X	Register reset
X	⌐	H	X	X	Storage the data into register at the rising edge of SCK
X	⌐	H	X	X	The state of register is unchangeable
X	X	X	⌐	X	Storage the data into flip-latch at the rising edge of RCK
X	X	X	⌐	X	The state of flip-latch is unchangeable

X: irrelevant

PACKAGE OUTLINE

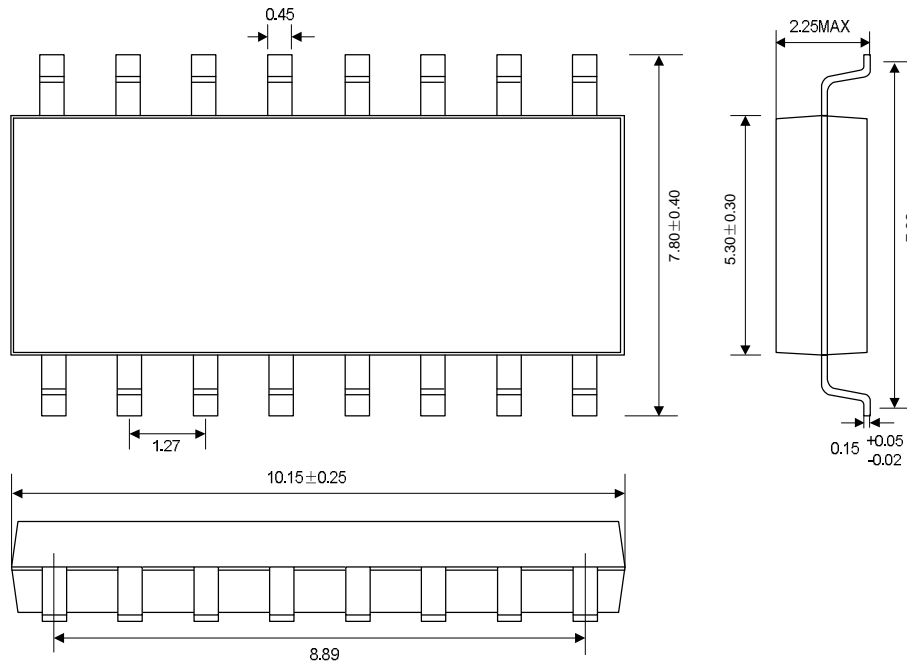**DIP-16-300-2.54**   **UNIT: mm**

2.54

6.35±0.25

7.62

0.25±0.05

1.52

15 degree

19.55±0.30

4.36MAX

0.5MIN

3.00MIN

0.46

1.27MAX

SOP-16-225-1.27   **UNIT: mm**

1.80MAX

6.0±0.4

3.9±0.3

5.72±0.25

1.27

0.4

0.2 +0.05 −0.02

10.15±0.25
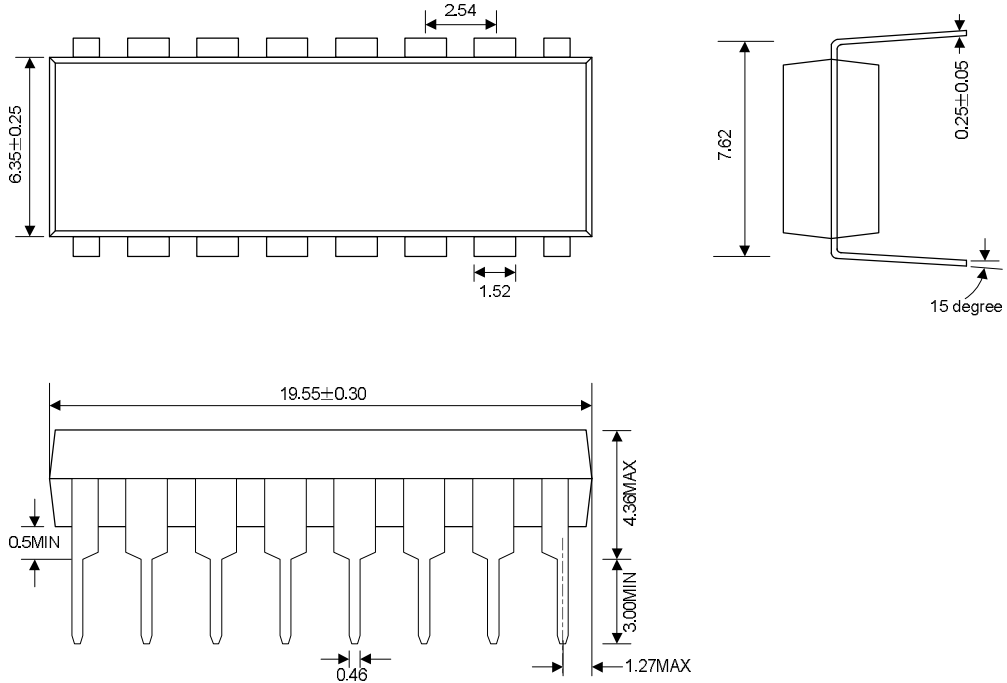
PACKAGE OUTLINE

SOP-16-300-1.27   **UNIT: mm**

0.45

2.25MAX

7.80±0.40

5.30±0.30

7.62

1.27

0.15 +0.05 -0.02

10.15±0.25

8.89

TSSOP-16-225-0.65   **UNIT: mm**

0°~8°

4.40±0.10

6.40±0.20

0.25

0.127±0.08

0.60±0.10

5.127±0.15

1.20MAX

0.10 +0.05 -0.08

0.65   0.22
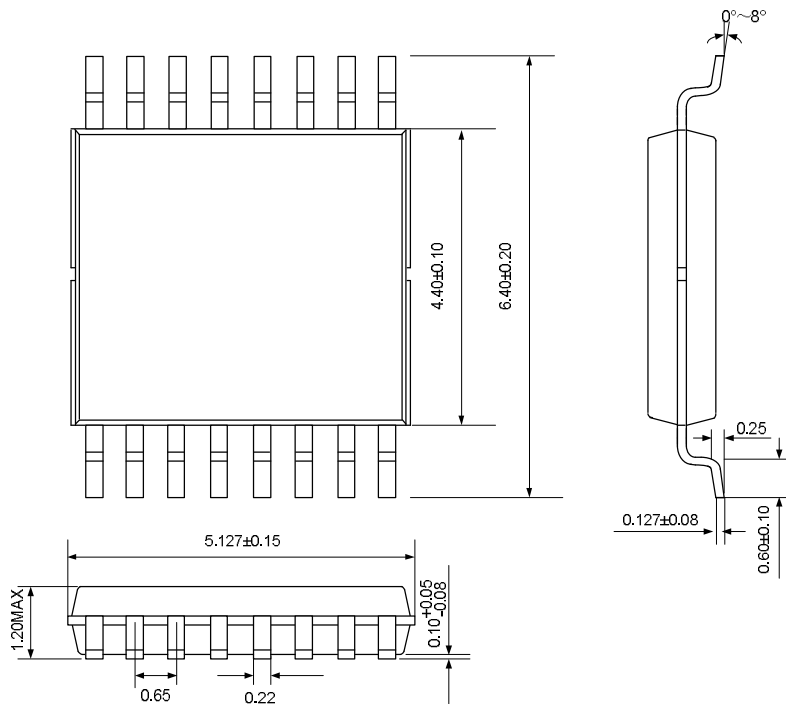
PACKAGE OUTLINE

SSOP-16-300-0.65   UNIT: mm

7.80±0.20

0.33   0.65

0.825±0.200

0~8°

5.25±0.20

7.62±0.20

0.18±0.015

6.15±0.20

1.50±0.20

1.65±0.20

0.15±0.05

CAUTION
ELECTROSTATIC
SENSITIVE DEVICE
DO NOT OPEN OR HANDLE
EXPECT AT A STATIC FREE
WORKSTATION
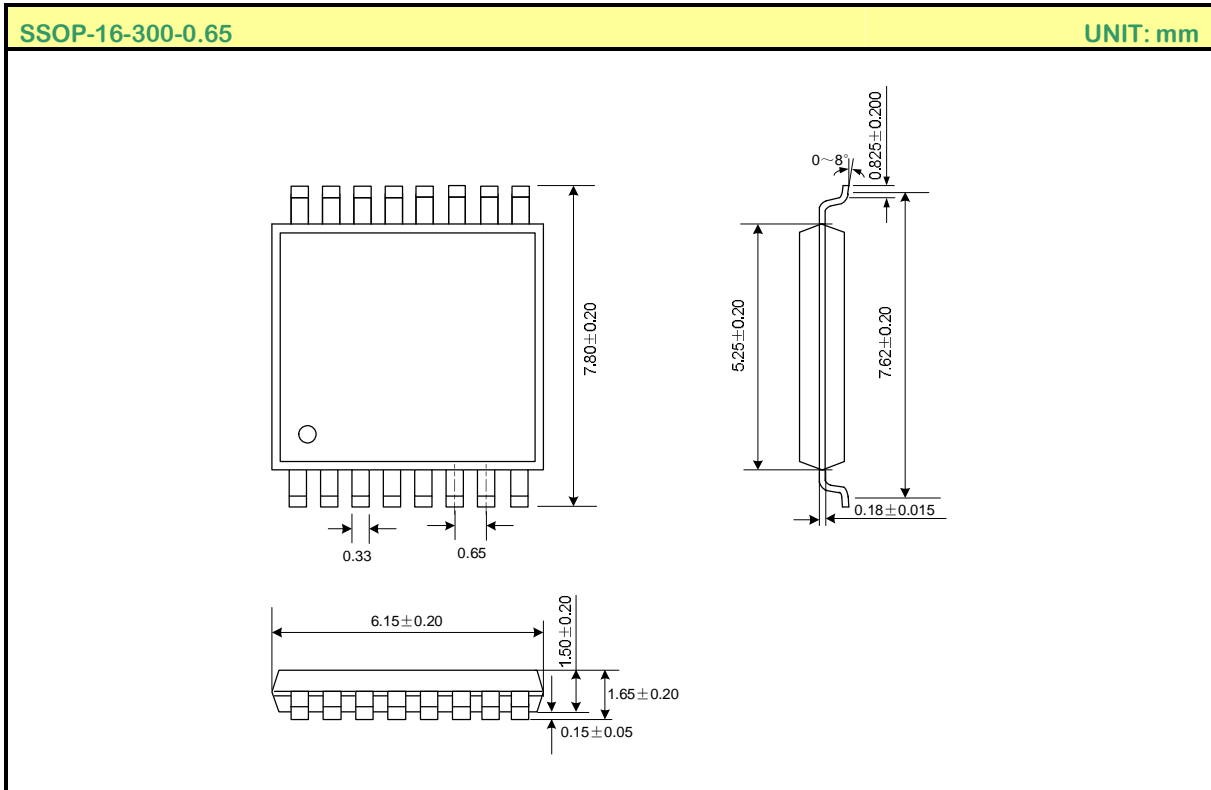
HANDLING MOS DEVICES:

    Electrostatic charges can exist in many things. All of our MOS devices are internally protected against electrostatic discharge but they can be damaged if the following precautions are not taken:

- Persons at a work bench should be earthed via a wrist strap.
- Equipment cases should be earthed.
- All tools used during assembly, including soldering tools and solder baths, must be earthed.
- MOS devices should be packed for dispatch in antistatic/conductive containers.