

Low Vcesat PNP Epitaxial Planar Transistor

BTB1205I3

BV_{CEO}	-20V
I_C	-5A
R_{CESAT}	127mΩ typ.

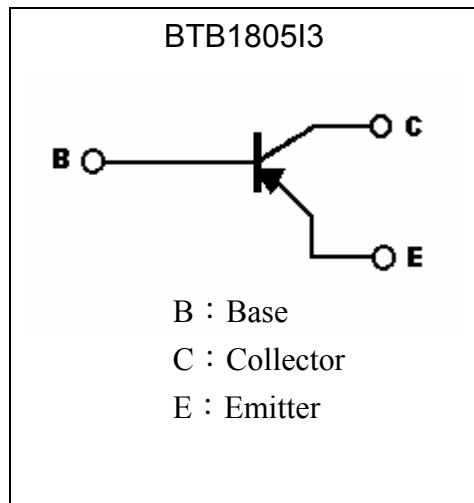
Features

- Low $V_{CE(sat)}$, $V_{CE(sat)}=-0.38$ V (typical), at $I_C / I_B = -3A / -60mA$
- Excellent DC current gain characteristics
- Fast switching speed
- Large current capacity
- RoHS compliant package

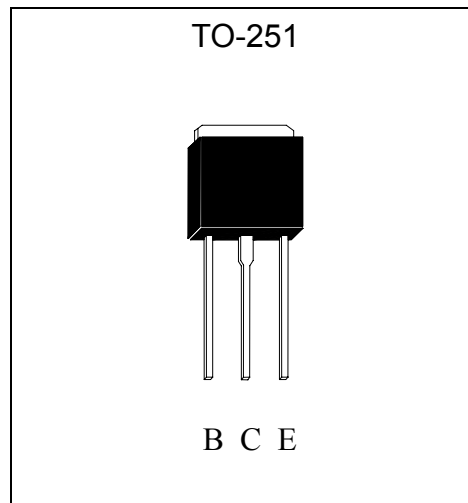
Applications

- Strobe, voltage regulators, relay drivers, lamp drivers

Symbol



Outline



**Absolute Maximum Ratings** (Ta=25°C)

Parameter	Symbol	Limits	Unit
Collector-Base Voltage	V _{CBO}	-25	V
Collector-Emitter Voltage	V _{CEO}	-20	V
Emitter-Base Voltage	V _{EBO}	-5	V
Collector Current(DC)	I _C	-5	A
Collector Current(Pulse)	I _{CP}	-8 (Note 1)	
Base Current	I _B	-0.5	A
Power Dissipation (T _A =25°C)	P _d	1	W
Power Dissipation (T _C =25°C)	P _d	10	
Junction Temperature	T _j	150	°C
Storage Temperature	T _{stg}	-55~+150	°C

Note : 1. Single Pulse Pw=10ms

Characteristics (Ta=25°C)

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
BV _{CBO}	-25	-	-	V	I _C =-10μA, I _E =0
BV _{CEO}	-20	-	-	V	I _C =-1mA, I _B =0
BV _{EBO}	-5	-	-	V	I _E =-10μA, I _C =0
I _{CBO}	-	-	-0.5	μA	V _{CB} =-20V, I _E =0
I _{EBO}	-	-	-0.5	μA	V _{EB} =-4V, I _C =0
*V _{CE(sat)}	-	-380	-500	mV	I _C =-3A, I _B =-60mA
*V _{BE(sat)}	-	-1.0	-1.3	V	I _C =-3A, I _B =-60mA
*h _{FE}	190	-	380	-	V _{CE} =-2V, I _C =-0.5A
*h _{FE}	60	-	-	-	V _{CE} =-2V, I _C =-4A
f _T	-	320	-	MHz	V _{CE} =-5V, I _C =-200mA, f=100MHz
C _{ob}	-	60	-	pF	V _{CB} =-10V, f=1MHz

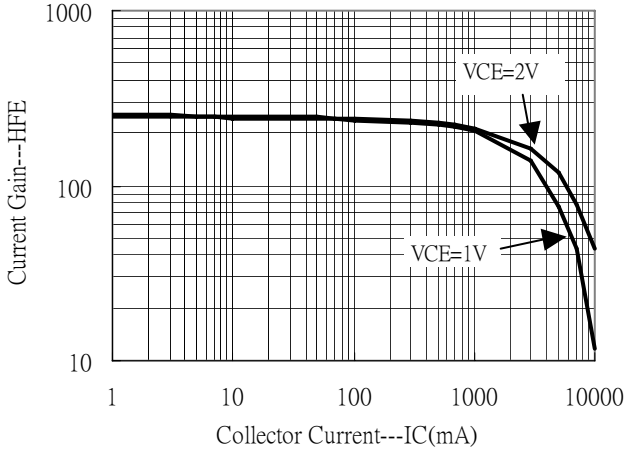
*Pulse Test : Pulse Width ≤380μs, Duty Cycle≤2%

Ordering Information

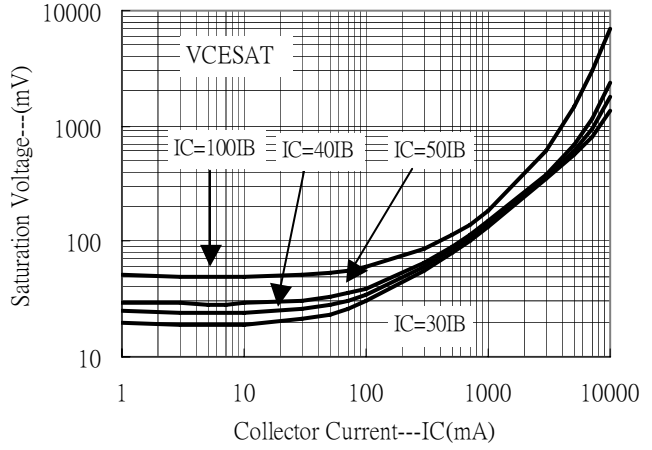
Device	Package	Shipping	Marking
BTB1205I3	TO-251 (RoHS compliant)	80 pcs / tube, 50 tubes / box	B1205

Characteristic Curves

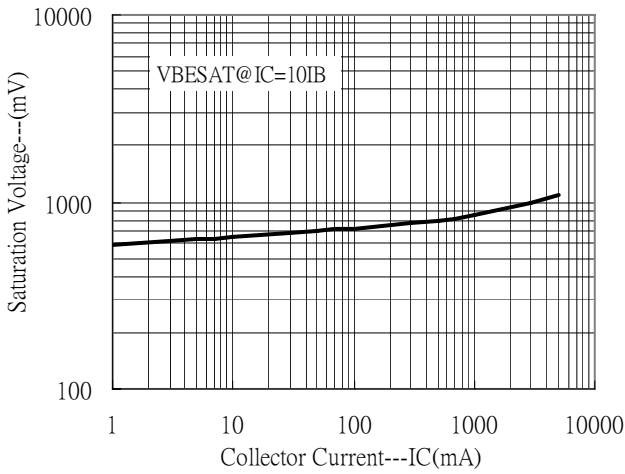
Current Gain vs Collector Current



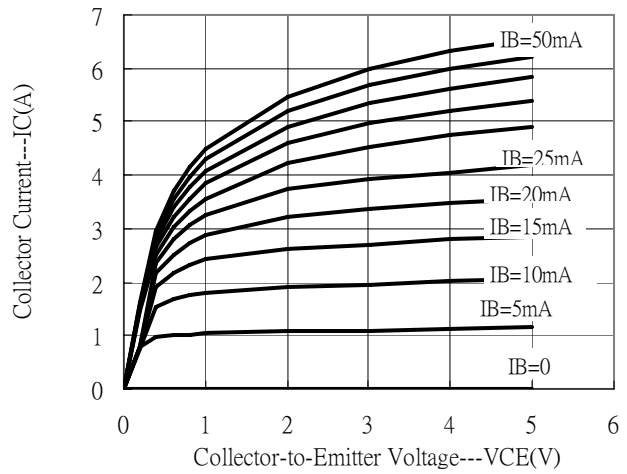
Saturation Voltage vs Collector Current



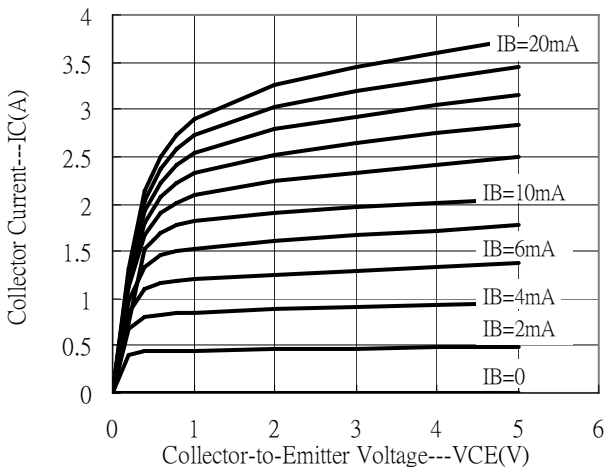
Saturation Voltage vs Collector Current



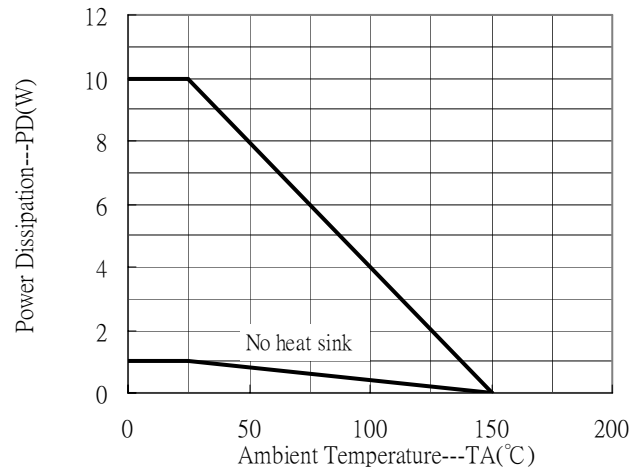
Output Characteristics



Output Characteristics



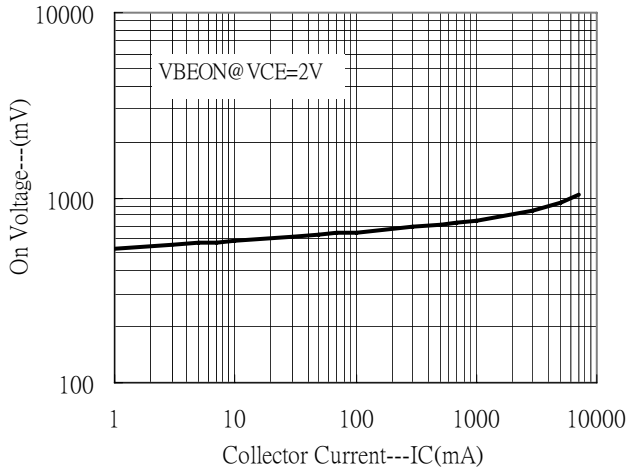
Power Derating Curves





Characteristic Curves(Cont.)

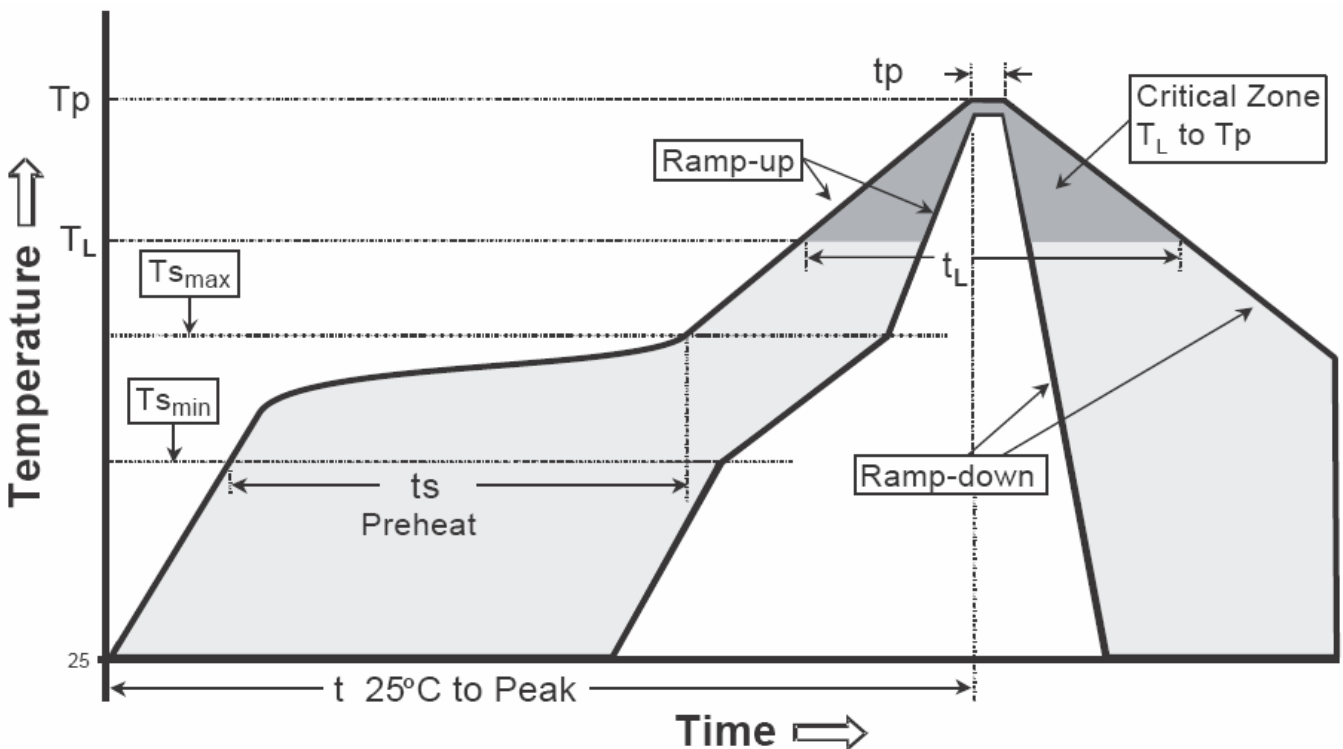
On Voltage vs Collector Current



Recommended wave soldering condition

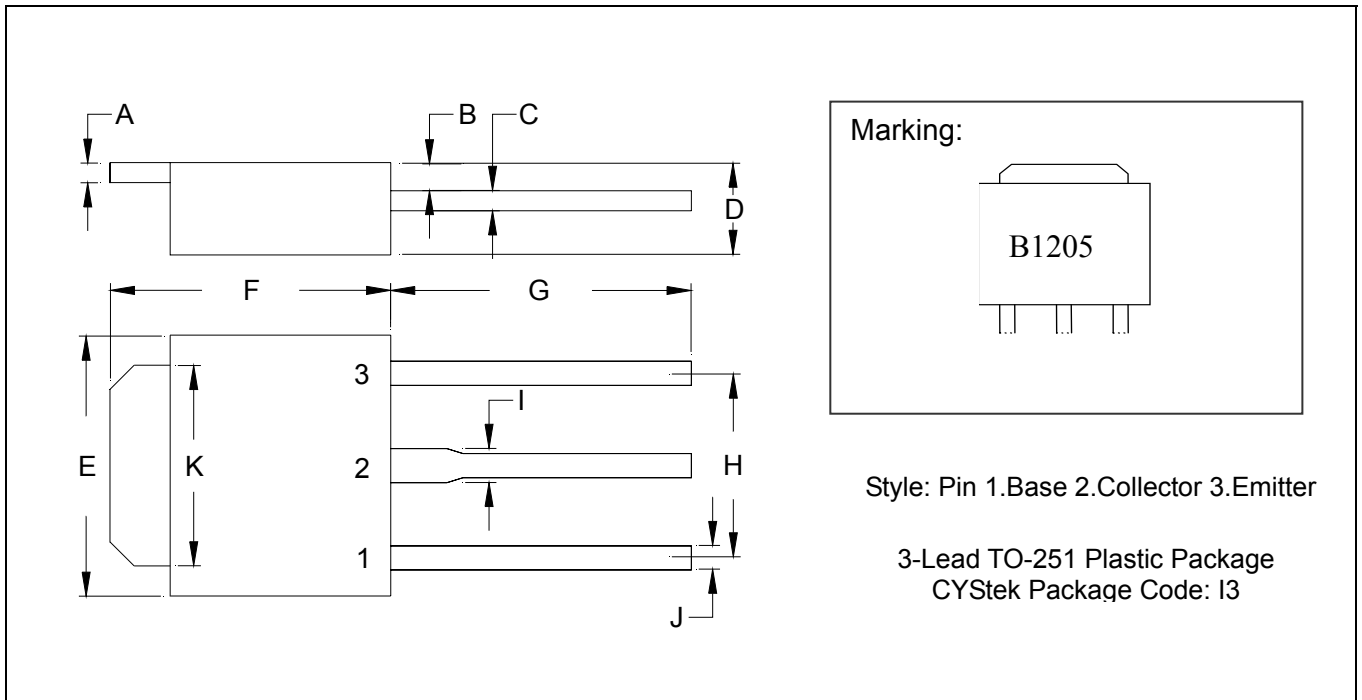
Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

Recommended temperature profile for IR reflow



Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (T _{smax} to T _p)	3°C/second max.	3°C/second max.
Preheat		
-Temperature Min(T _{s min})	100°C	150°C
-Temperature Max(T _{s max})	150°C	200°C
-Time(t _{s min} to t _{s max})	60-120 seconds	60-180 seconds
Time maintained above:		
-Temperature (T _L)	183°C	217°C
- Time (t _L)	60-150 seconds	60-150 seconds
Peak Temperature(T _P)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(t _p)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

TO-251 Dimension



Style: Pin 1.Base 2.Collector 3.Emitter

3-Lead TO-251 Plastic Package
 CYStek Package Code: I3

*: Typical

DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.0177	0.0217	0.45	0.55	G	0.2559	-	6.50	-
B	0.0354	0.0591	0.90	1.50	H	-	*0.1811	-	*4.60
C	0.0177	0.0236	0.45	0.60	I	-	0.0449	-	1.14
D	0.0866	0.0945	2.20	2.40	J	-	0.0346	-	0.88
E	0.2441	0.2677	6.20	6.80	K	0.2047	0.2165	5.20	5.50
F	0.2677	0.2835	6.80	7.20					

Notes: 1.Controlling dimension: millimeters.
 2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
 3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material:

- Lead :KFC ; pure tin plated
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0

Important Notice:

- All rights are reserved. Reproduction in whole or in part is prohibited without the prior written approval of CYStek.
- CYStek reserves the right to make changes to its products without notice.
- CYStek **semiconductor products are not warranted to be suitable for use in Life-Support Applications, or systems.**
- CYStek assumes no liability for any consequence of customer product design, infringement of patents, or application assistance.