TriQuint SEMICONDUCTOR

AGR21180EF
180 W, 2.110 GHz—2.170 GHz, N-Channel E-Mode, Lateral MOSFET

Introduction

The AGR21180EF is a high-voltage, gold-metalized, laterally diffused metal oxide semiconductor (LDMOS) RF power transistor suitable for wideband code division multiple access (W-CDMA), single and multicarrier class AB wireless base station power amplifier applications.

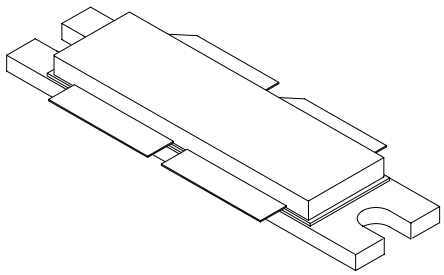


Figure 1. AGR21180EF (flanged) Package

Features

Typical performance for two carrier 3GPP W-CDMA systems. F1 = 2135 MHz and F2 = 2145 MHz with 3.84 MHz channel bandwidth (BW), adjacent channel BW = 3.84 MHz at F1 – 5 MHz and F2 + 5 MHz. Third-order distortion is measured over 3.84 MHz BW at F1 – 10 MHz and F2 + 10 MHz. Typical peak-to-average (P/A) ratio of 8.5 dB at 0.01% (probability) CCDF:

- Output power: 38 W.
- Power gain: 14 dB.
- Efficiency: 26%.
- IM3: –36 dBc.
- ACPR: –39 dBc.
- Return loss: –12 dB.

High-reliability, gold-metalization process.

Hot carrier injection (HCI) induced bias drift of <5% over 20 years.

Internally matched.

High gain, efficiency, and linearity.

Integrated ESD protection.

Device can withstand a 10:1 voltage standing wave ratio (VSWR) at 28 Vdc, 2140 MHz, 180 W output power pulsed 4 μs at 10% duty.

Large signal impedance parameters available.

Table 1. Thermal Characteristics

Parameter	Sym	Value	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.35	°C/W

Table 2. Absolute Maximum Ratings*

Parameter	Sym	Value	Unit
Drain-source Voltage	V_{DSS}	65	Vdc
Gate-source Voltage	V_{GS}	–0.5, 15	Vdc
Total Dissipation at T_C = 25 °C	P_D	500	W
Derate Above 25 ˚C	—	2.86	W/°C
Operating Junction Temperature	T_J	200	°C
Storage Temperature Range	T_{STG}	–65, 150	°C

* Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

Table 3. ESD Rating*

AGR21180EF	Minimum (V)	Class
HBM	500	1B
MM	50	A
CDM	1000	4

* Although electrostatic discharge (ESD) protection circuitry has been designed into this device, proper precautions must be taken to avoid exposure to ESD and electrical overstress (EOS) during all handling, assembly, and test operations. PEAK Devices employs a human-body model (HBM), a machine model (MM), and a charged-device model (CDM) qualification requirement in order to determine ESD-susceptibility limits and protection design evaluation. ESD voltage thresholds are dependent on the circuit parameters used in each of the models, as defined by JEDEC's JESD22-A114B (HBM), JESD22-A115A (MM), and JESD22-C101A (CDM) standards.

Caution: MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

Electrical Characteristics

Recommended operating conditions apply unless otherwise specified: T_C = 30 °C.

Table 4. dc Characteristics

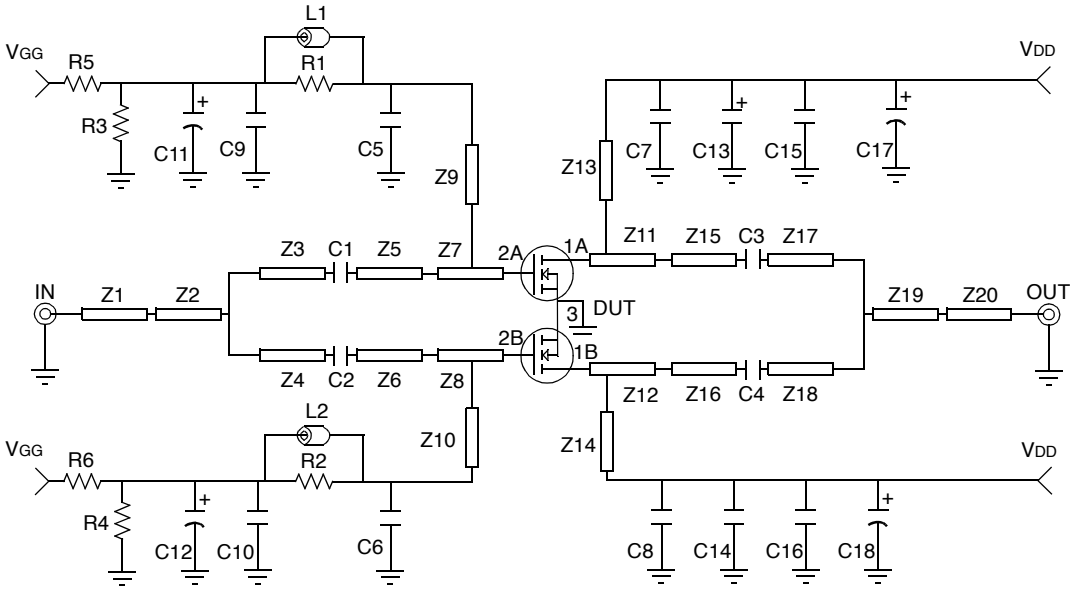
Parameter	Symbol	Min	Typ	Max	Unit
Off Characteristics					
Drain-source Breakdown Voltage (V_{GS} = 0, I_D = 400 μA)	$V_{(BR)DSS}$	65	—	—	Vdc
Gate-source Leakage Current (V_{GS} = 5 V, V_{DS} = 0 V)	I_{GSS}	—	—	6	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 28 V, V_{GS} = 0 V)	I_{DSS}	—	—	200	μAdc
On Characteristics					
Forward Transconductance (V_{DS} = 10 V, I_D = 1 A)	G_{FS}	—	12	—	S
Gate Threshold Voltage (V_{DS} = 10 V, I_D = 600 μA)	$V_{GS(TH)}$	2.8	3.4	4.0	Vdc
Gate Quiescent Voltage (V_{DS} = 28 V, I_D = 2 x 800 mA)	$V_{GS(Q)}$	3.0	3.7	4.6	Vdc
Drain-source On-voltage (V_{GS} = 10 V, I_D = 1 A)	$V_{DS(ON)}$	—	0.08	—	Vdc

Table 5. RF Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Dynamic Characteristics					
Reverse Transfer Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz) (This part is internally matched on both the input and output.)	C_{RSS}	—	4.0	—	pF
Functional Tests (in Supplied Test Fixture)					
Common-source Amplifier Power Gain*	G_{PS}	13	14	—	dB
Drain Efficiency*	η	23	26	—	%
Third-order Intermodulation Distortion* (IM3 distortion measured over 3.84 MHz BW @ f1 – 10 MHz and f2 + 10 MHz)	IM3	—	–36	–33	dBc
Adjacent Channel Power Ratio* (ACPR measured over BW of 3.84 MHz @ f1 – 5 MHz and f2 + 5 MHz)	ACPR	—	–39	–36	dBc
Input Return Loss*	IRL	—	–13	–10	dB
Power Output, 1 dB Compression Point, pulsed 4 μs at 10% duty. (V_{DD} = 28 V, f_C = 2140.0 MHz)	P_{1dB}	160	200	—	W
Output Mismatch Stress (V_{DD} = 28 V, P_{OUT} = 180 W (pulsed 4 μs at 10% duty), I_{DQ} = 2 x 800 mA, f_C = 2140.0 MHz VSWR = 10:1; [all phase angles])	ψ	No degradation in output power.			

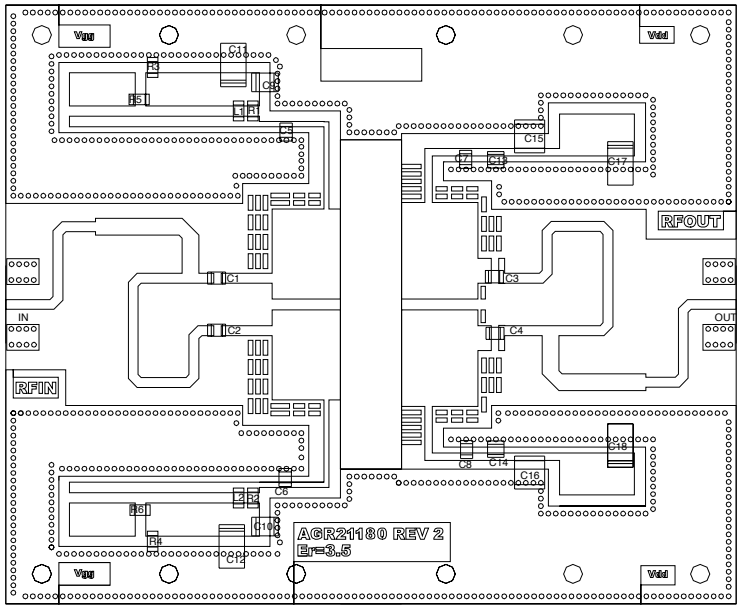
* 3GPP W-CDMA, typical P/A ratio of 8.5 dB at 0.01% CCDF, f1 = 2135.0 MHz, and f2 = 2145 MHz.
V_{DD} = 28 Vdc, I_{DQ} = 2 x 800 mA, and P_{OUT} = 38 W average.
Nominal operating voltage 28 Vdc. Qualified for a maximum operating voltage of 32 Vdc ±0.5 V.

Test Circuit Illustrations



PINS:
1A. DRAIN
1B. DRAIN
2A. GATE
2B. GATE
3. SOURCE

A. Schematic



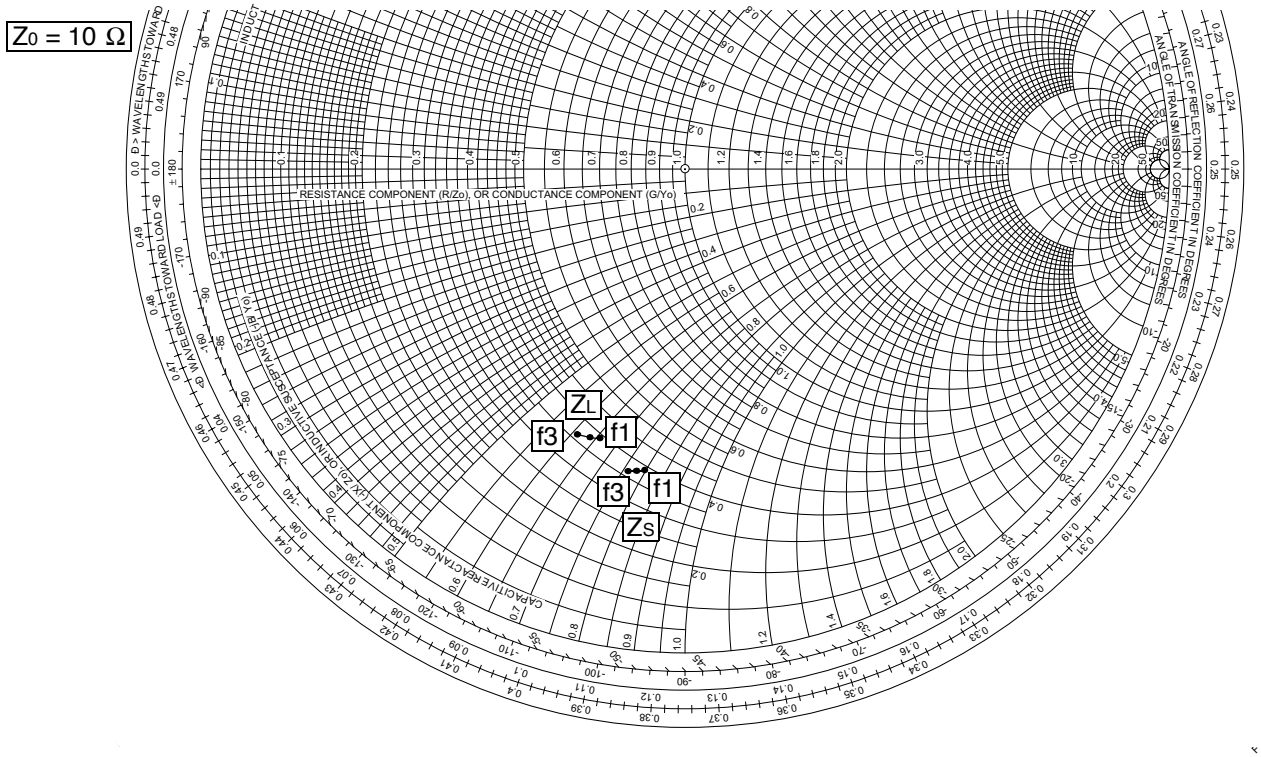
Parts List:

- Microstrip line: Z1, Z20: 1.079 in. x 0.065 in.; Z2, Z19: 0.914 in. x 0.112 in.; Z3: 0.100 in. x 0.065 in.; Z4: 1.814 in. x 0.065 in.; Z5, Z6: 0.340 in. x 0.065 in.; Z7, Z8: 0.455 in. x 0.600 in.; Z9, Z10: 0.835 in. x 0.035 in.; Z11, Z12: 0.510 in. x 0.645 in.; Z13, Z14: 0.585 in. x 0.050 in.; Z15, Z16: 0.089 in. x 0.166 in.; Z17: 2.006 in. x 0.065 in.; Z18: 0.292 in. x 0.065 in.
- *ATC*® chip capacitor: C1, C2, C3, C4: 20 pF 100B200JW500X; C5, C6, C7, C8: 5.6 pF 100B5R6BW500X (side mounted); C13, C14: 1000 pF 100B102JCA500X.
- *Murata®* capacitor: C9, C10: 2.2 μF, 50 V GRM43ER71H225KA01L C15, C16: 4.7 μF, 50 V GRM55ER7H475KA01
- *Sprague*® tantalum surface-mount chip capacitor: C11, C12, C17, C18: 15 μF, 35 V.
- 1206 size chip resistor: R1, R2: 4.7 Ω; R3, R4: 560 kΩ; R5, R6 470 kΩ.
- *Fair-Rite*® ferrite bead: L1, L2 2743019447.
- *Taconic*® ORCER RF-35: board material, 1 oz. copper, 30 mil thickness, εr = 3.5.

B. Component Layout

Figure 2. Test Circuit

Typical Performance Characteristics



(Optimally tuned for 28 Vds, 2 x 800 mA IDQ, POUT = 2 W-CDMA 38 W average operation.)

MHz (f)	ZS Ω (Complex Source Impedance)	ZL Ω (Complex Optimum Load Impedance)
2110 (f1)	4.02 – j7.92	3.92 – j6.59
2140 (f2)	3.98 – j7.73	3.79 – j6.32
2170 (f3)	3.80 – j7.63	3.67 – j6.12

ZS = Test circuit impedance as measured from gate to gate, balanced configuration.

ZL = Test circuit impedance as measured from drain to drain, balanced configuration.

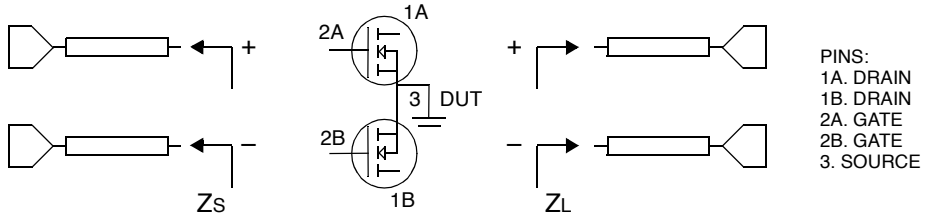
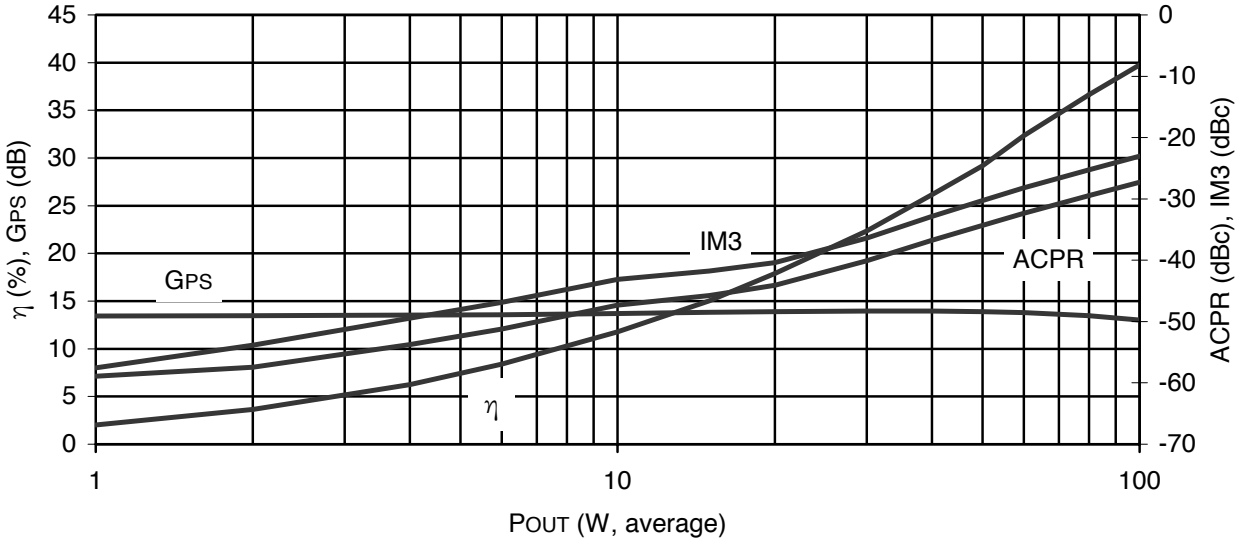


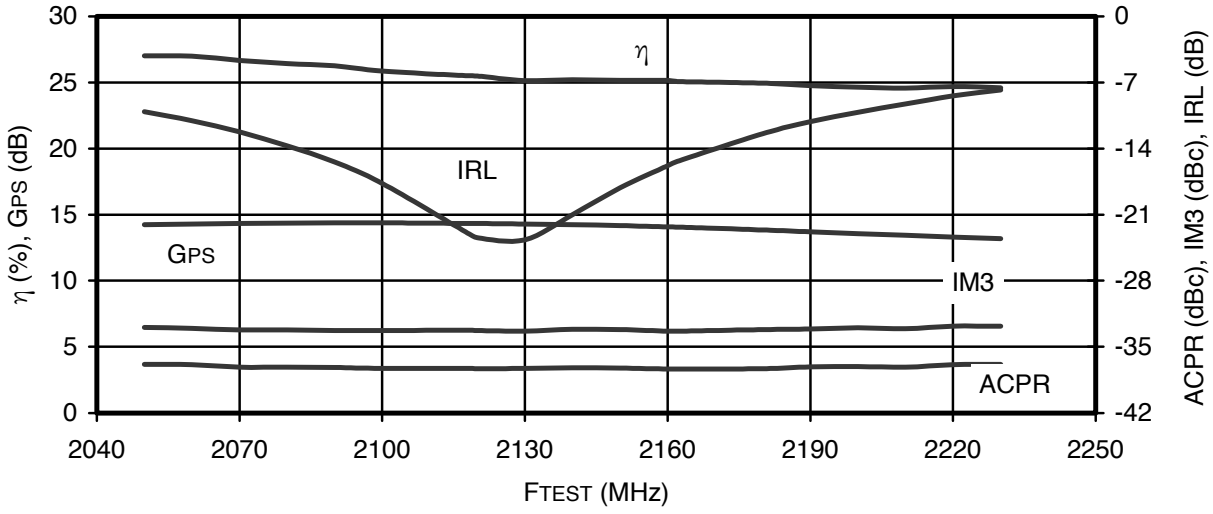
Figure 3. Series Equivalent Balanced Input and Output Impedances

Typical Performance Characteristics (continued)



Test Conditions:
28 VDS, IDQ = 1600 mA.
Two W-CDMA carriers, F1 = 2135 MHz and F2 = 2145 MHz each carrier has 8.98 dB P/A ratio @ 0.01% CCDF, 3.84 MHz channel BW (CBW).

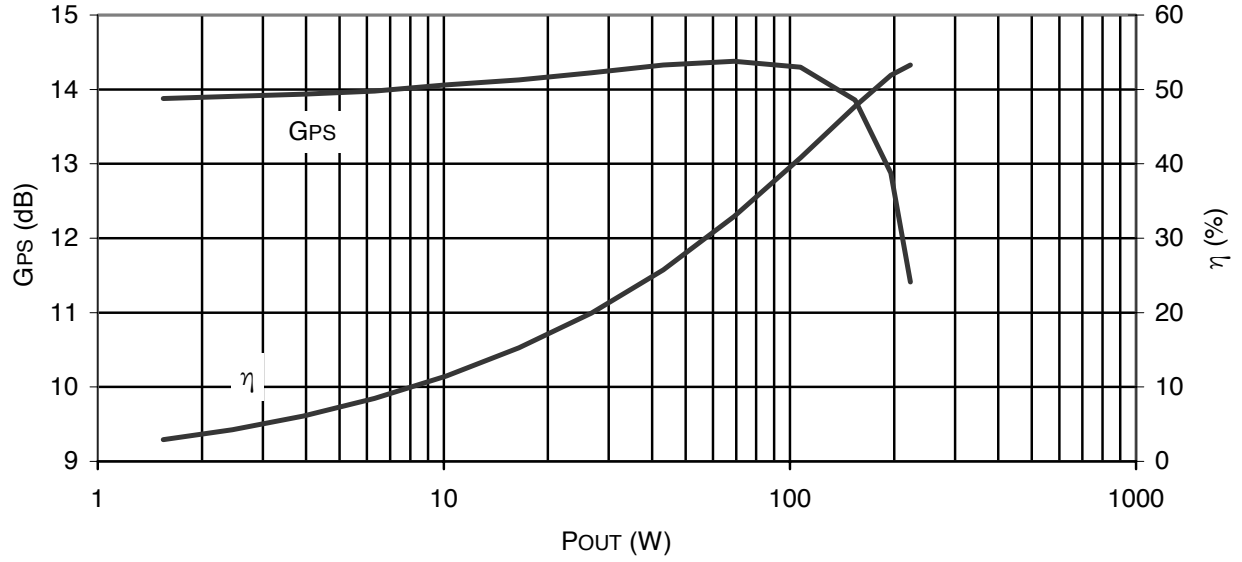
Figure 4. Power Gain, Drain Efficiency, ACPR, and IM3 vs. Output Power (2 W-CDMA carrier data)



Test Conditions:
28 VDS, IDQ = 1600 mA, POUT = 38 W (average).
Two W-CDMA carriers, each carrier has 8.98 dB P/A @ 0.01% probability (CCDF), F1 = FTEST - 5 MHz and F2 = FTEST + 5 MHz , 3.84 MHz CBW.

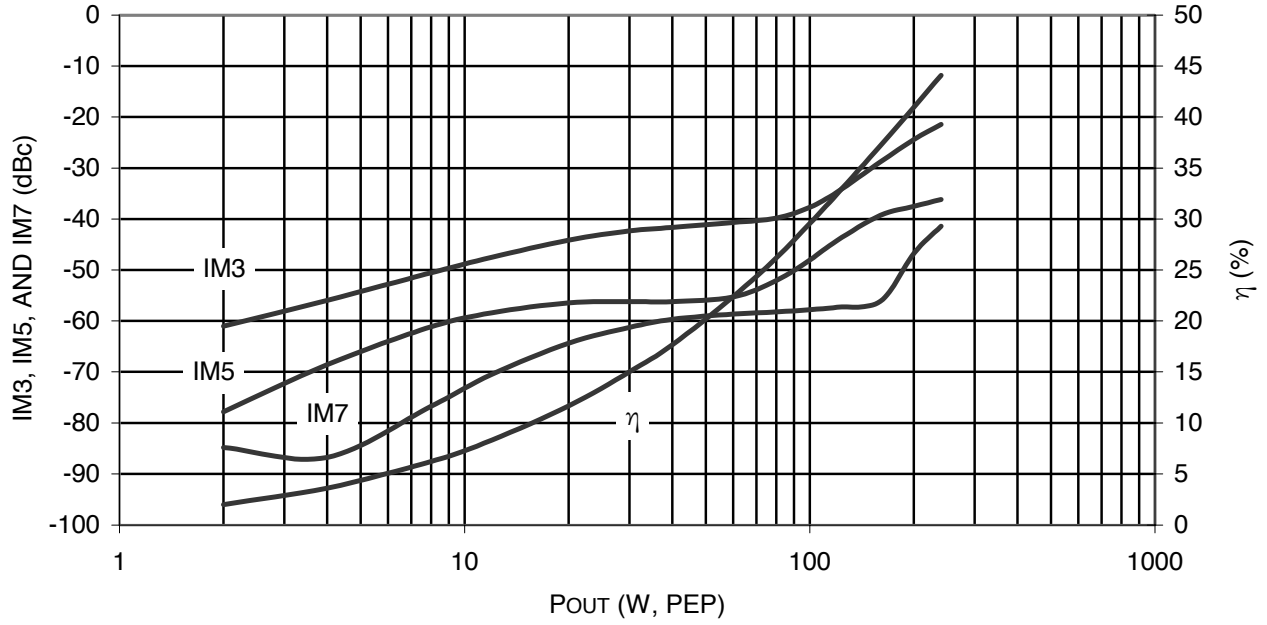
Figure 5. Power Gain, Drain Efficiency, ACPR, IM3, and IRL vs. Frequency (2 W-CDMA signal data)

Typical Performance Characteristics (continued)



Test Conditions:
28 VDS, IDQ = 1600 mA, 2140 MHz.

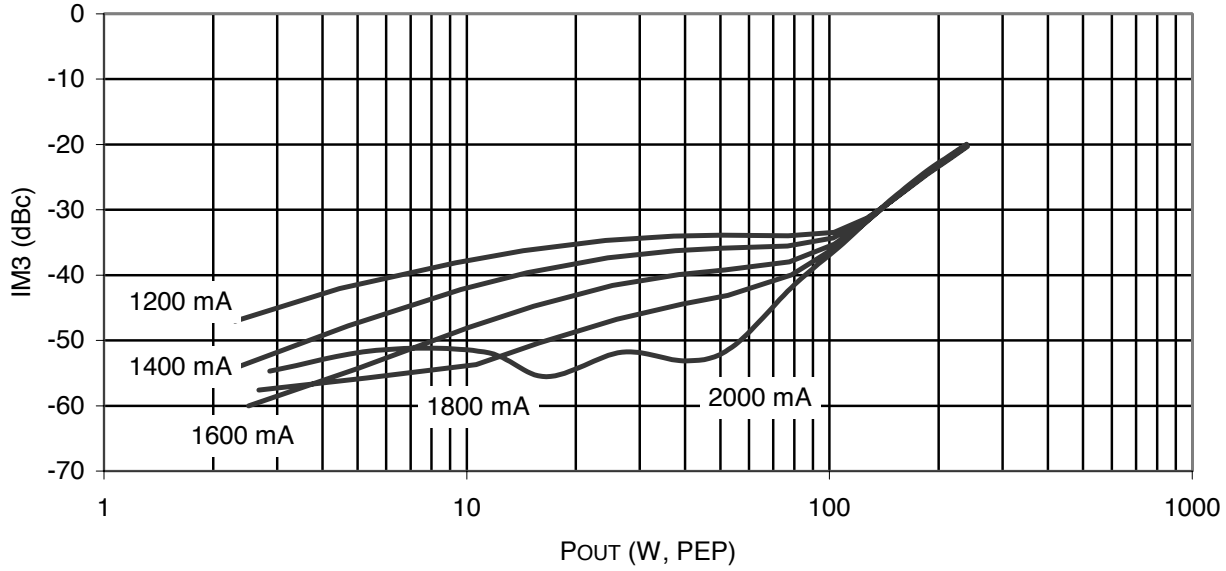
Figure 6. Power Gain and Drain Efficiency vs. Output Power (CW signal data)



Test Conditions:
28 VDS, IDQ = 1600 mA.
F1 = 2135 MHz and F2 = 2145 MHz.

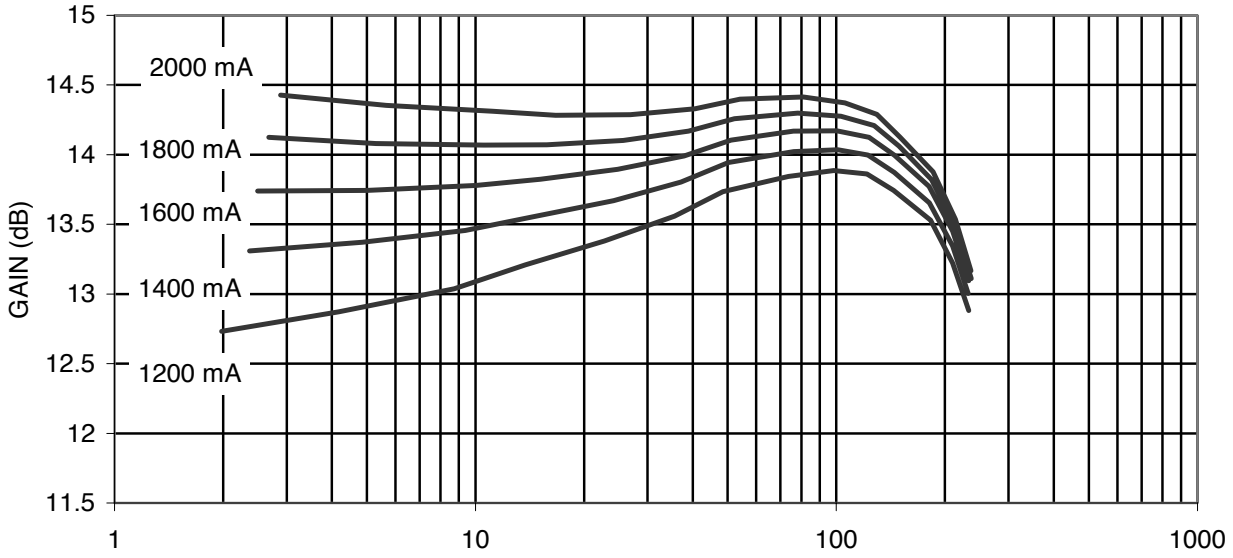
Figure 7. IM3, IM5, and IM7 vs. Output Power (2 CW signal data)

Typical Performance Characteristics (continued)



Test Conditions:
28 VDS, IDQ = 1200 mA to 2000 mA in 200 mA steps.
F1 = 2135 MHz and F2 = 2145 MHz.

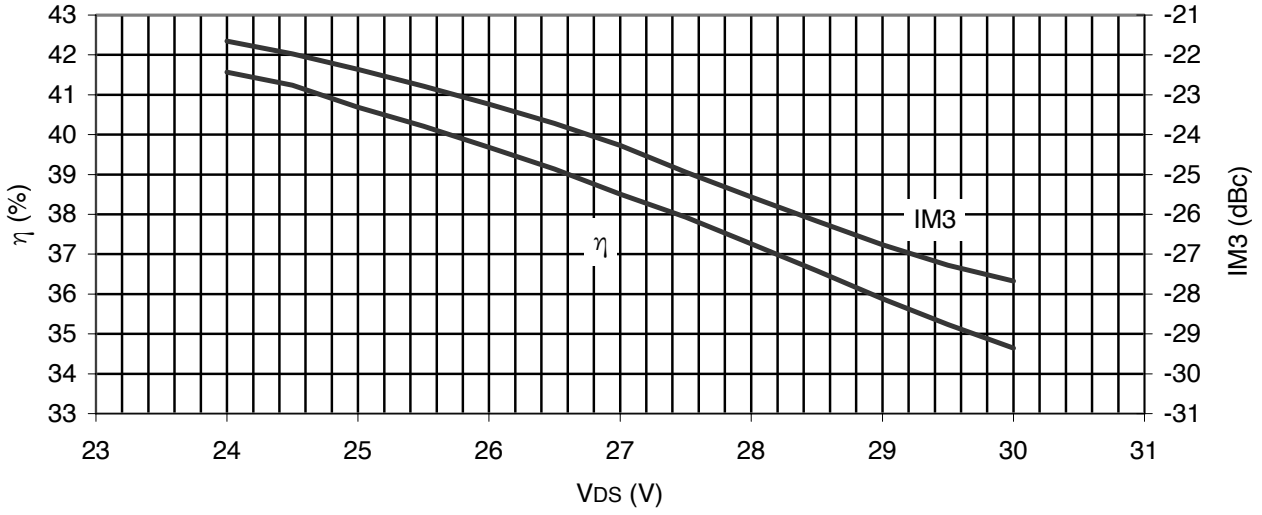
Figure 8. IM3 vs. Output Power at 1200 mA to 2000 mA, 200 mA Steps (2 CW signal data)



Test Conditions:
28 VDS, IDQ = 1200 mA to 2000 mA in 200 mA steps.
F1 = 2135 MHz and F2 = 2145 MHz.

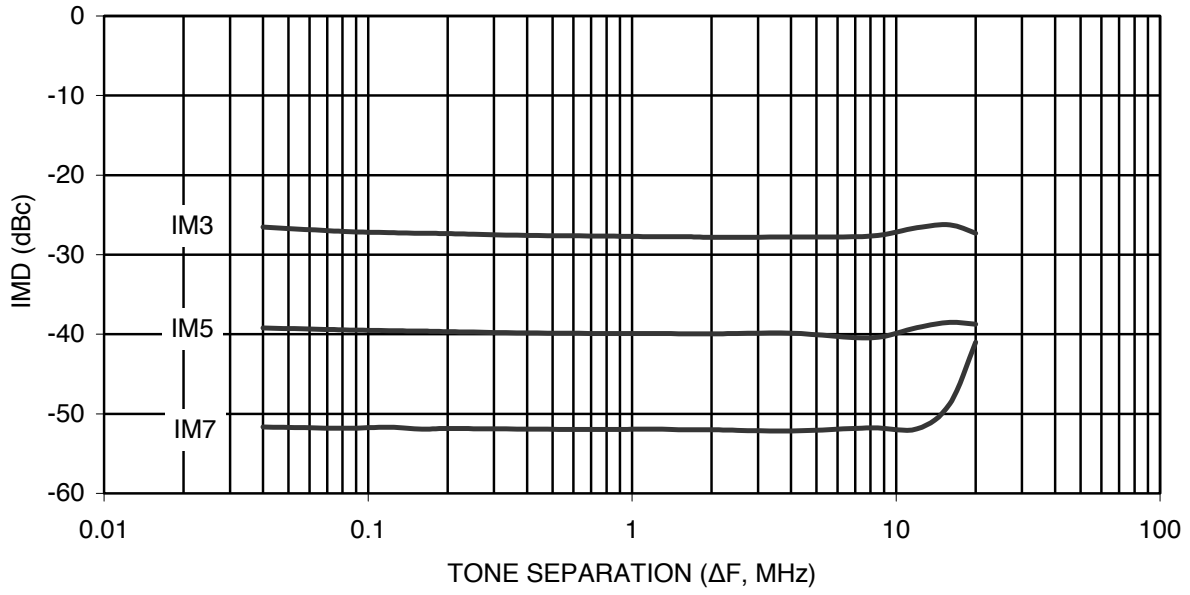
Figure 9. Power Gain vs. Output Power at 1200 mA to 2000 mA, 200 mA Steps (2 CW signal data)

Typical Performance Characteristics (continued)



Test Conditions:
IDQ = 1600 mA, POUT = 170 W peak envelope power (PEP).
F1 = 2135 MHz and F2 = 2145 MHz.

Figure 10. IM3 and Drain Efficiency vs. VDS (2 CW signal data)



Test Conditions:
28 VDS, IDQ = 1600 mA, POUT = 170 W (PEP).
FCENTER = 2140 MHz, F1 = FCENTER - ΔF/2 MHz, F2 = FCENTER - ΔF/2 MHz.

Figure 11. Intermodulation Products vs. Tone Separation (2 CW signal data)

Typical Performance Characteristics (continued)

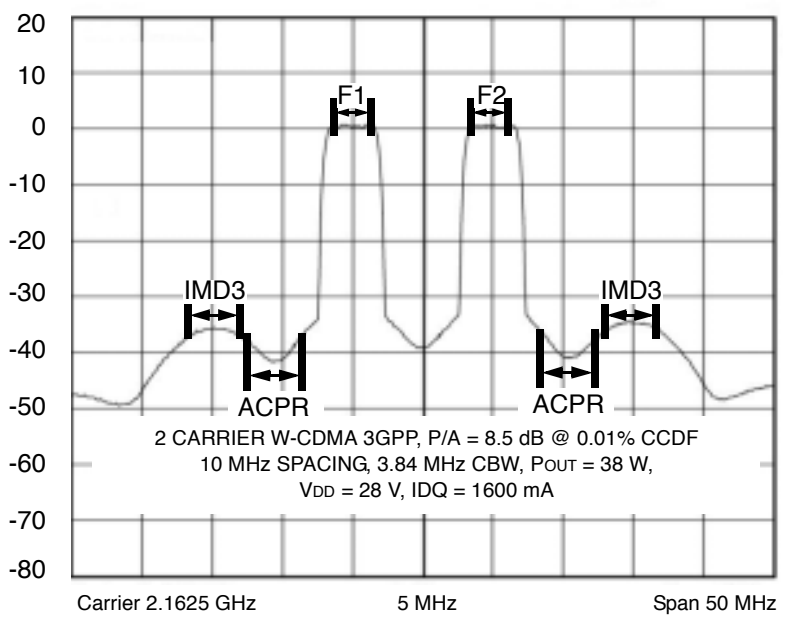
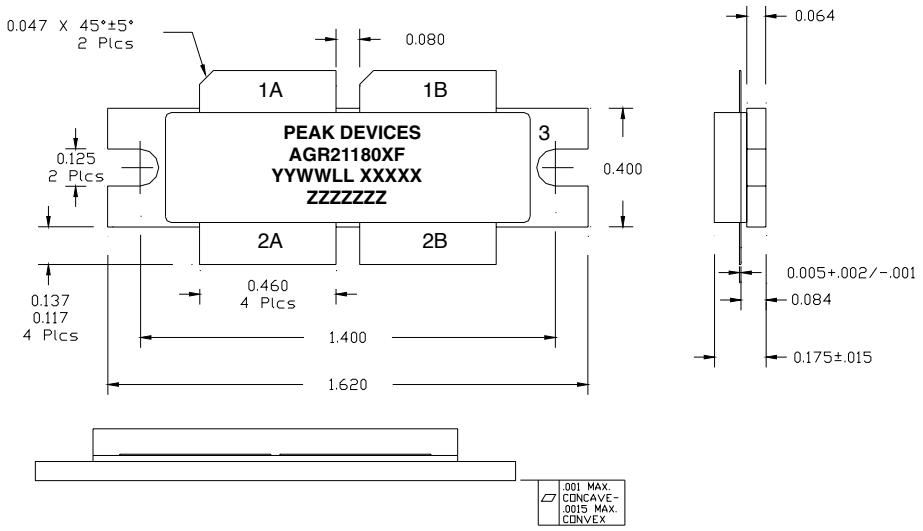


Figure 12. Spectral Plot

Package Dimensions

All dimensions are in inches. Tolerances are ±0.005 in. unless specified.



PINS:
1A. DRAIN
1B. DRAIN
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3. SOURCE

Label Notes:

- M before the part number denotes model program. X before the part number denotes engineering prototype.
- The last two letters of the part number denote wafer technology and package type.
- YYWWLL is the date code including place of manufacture: year year work week (YYWW), LL = location (AL = Allentown, PA; BK = Bangkok, Thailand). XXXXX = five-digit wafer lot number.
- ZZZZZZZ = seven-digit assembly lot number on production parts.
- ZZZZZZZZZZZZ = 12-digit (five-digit lot, two-digit wafer, and five-digit serial number) on models and engineering prototypes.