5.0 or 3.3V, 4 Mbit (512 Kbit x 8) TIMEKEEPER NVSRAM

**Part No. HMNR5128D(V)**

## GENERAL DESCRIPTION

The HMNR5128D(V) TIMEKEEPER SRAM is a 512Kb x 8 non-volatile static RAM and real time clock organized as 524,280 words by 8 bits. The special DIP package provides a fully integrated battery back-up memory and real time clock solution. The HMNR5128D(V) directly replaces industry standard 512Kbit x 8 SRAMs. It also provides the non-volatility of Flash without any requirement for special WRITE timing or limitations on the number of WRITEs that can be performed.

## FEATURES

■ INTEGRATED LOW POWER SRAM, REAL TIME CLOCK, POWER-FAIL CONTROL CIRCUIT, BATTERY and CRYSTAL

■ BCD CODED YEAR, MONTH, DAY, DATE, HOURS, MINUTES, and SECONDS

■ AUTOMATIC POWER-FAIL CHIP DESELECT and WRITE PROTECTION VOLTAGES :

($V_{PFD}$ = Power-fail Deselect Voltage)

– HMNR5128D : $V_{CC}$ = 4.5 to 5.5V

4.2V ≤ $V_{PFD}$ ≤ 4.5V

– HMNR5128DV: $V_{CC}$ = 3.0 to 3.6V

2.7V ≤ $V_{PFD}$ ≤ 3.0V

■ CONVENTIONAL SRAM OPERATION : UNLIMITED WRITE CYCLES

■ SOFTWARE CONTROLLED CLOCK CALIBRATION FOR HIGH ACCURACY APPLICATIONS

■ 10 YEARS OF DATA RETENTION and CLOCK OPERATION IN THE ABSENCE OF POWER PIN and FUNCTION COMPATIBLE WITH INDUSTRY STANDARD 512K x 8 SRAMS

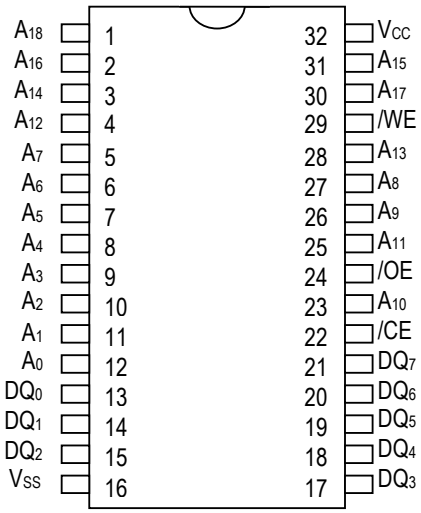
■ SELF-CONTAINED BATTERY and CRYSTAL IN DIP PACKAGE

## OPTIONS

## MARKING

| OPTIONS | MARKING |
|---|---|
| • Timing | |
| 70 ns | -70 |
| 85 ns | -85 |

## PIN ASSIGNMENT

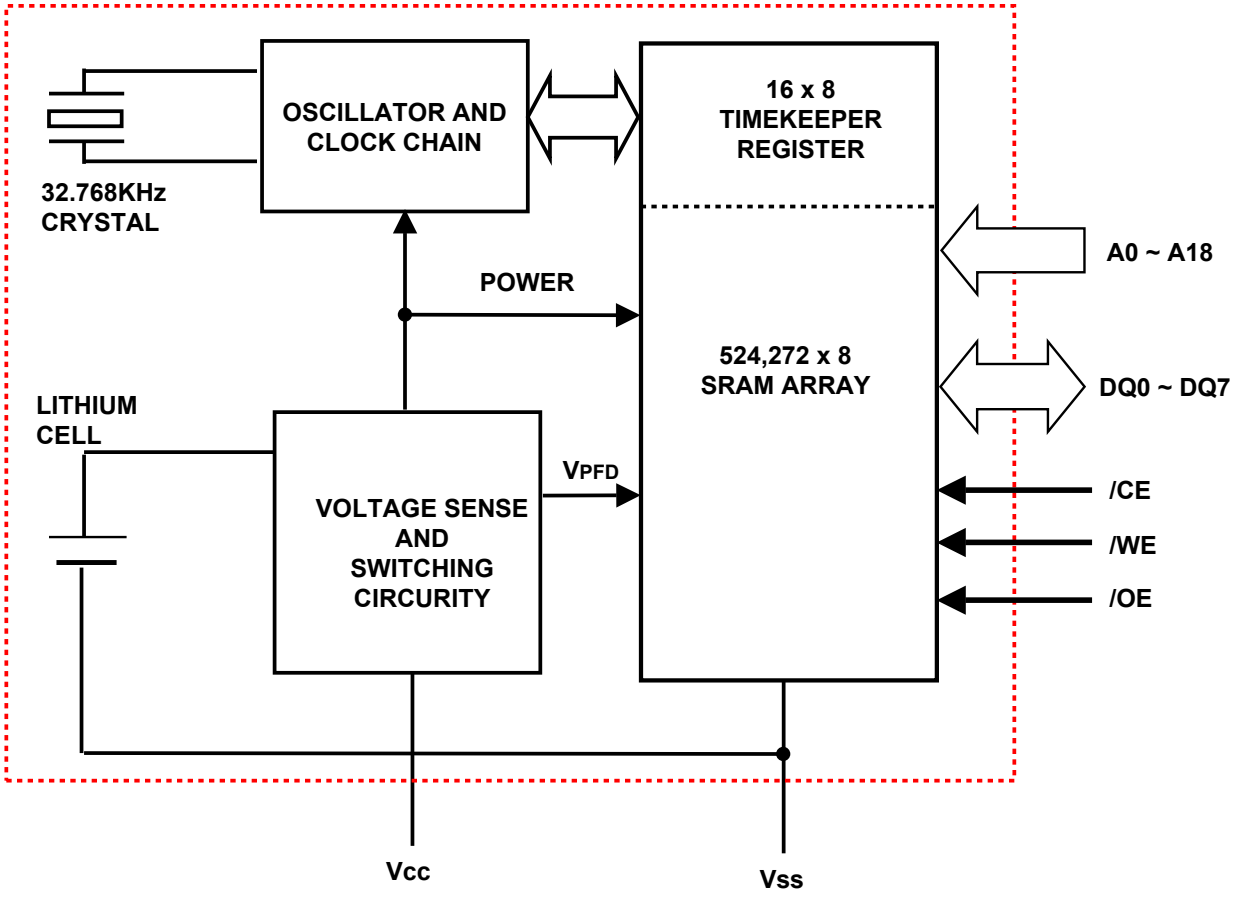



32-pin Encapsulated Package

## FUNCTIONAL DESCRIPTION

The HMNR5128D(V) is a full function, year 2000 compliant (Y2KC), real–time clock/calendar (RTC) and 512k x 8 non-volatile static RAM. User access to all registers within the HMNR5128D(V) is accomplished with a bytewide interface . The Real-time clock (RTC) information and control bits reside in the eight upper most RAM locations. The RTC registers contain century, year, month, date, day, hours, minutes, and seconds data in 24-hour BCD format. Corrections for the date of each month and leap year are made automatically. The RTC clock registers are double buffered to avoid access of incorrect data that can occur during clock update cycles. The double buffered system also prevents time loss as the timekeeping countdown continues unabated by access to time register data. The HMNR5128D(V) also contains its own power-fail circuitry which deselects the device when the $V_{CC}$ supply is in an out of tolerance condition. This feature prevents loss of data from unpredictable system operation brought on by low $V_{CC}$ as errant access and update cycles are avoided.

## BLOCK DIAGRAM




A0-A18 : Address Input

/CE : Chip Enable

$V_{ss}$ : Ground

DQ0-DQ7 : Data In / Data Out

/WE : Write Enable

/OE : Output Enable

$V_{CC}$ : Power (+5V or +3.3V)

NC : No Connection

## Absolute Maximum Ratings

| Symbol | Parameter | | Value | Unit |
|---|---|---|---|---|
| $T_A$ | AmbientOperatingTemperature | | 0 to 70 | °C |
| $T_{STG}$ | Storage Temperature(Vcc Off, Oscillator Off) | | -40 to 70 | °C |
| $T_{SLD}$(1) | Lead Solder Temperature for 10 seconds | | 260 | °C |
| $V_{IO}$ | Input or Output Voltage | | -0.3 to Vcc+0.3 | V |
| $V_{CC}$ | Supply Voltage | HMNR5128D | 4.5 to 5.5 | V |
| | | HMNR5128DV | 3.0 to 3.6 | V |
| $I_O$ | Output Current | | 20 | mA |
| $P_D$ | Power Dissipation | | 1 | W |

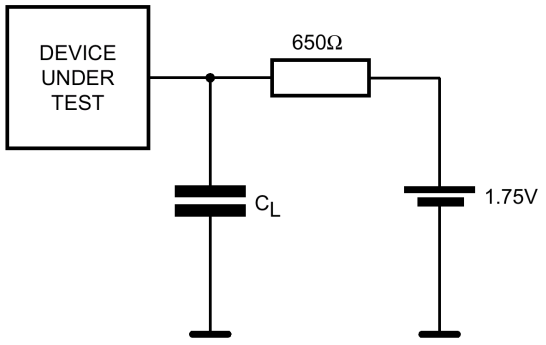
**Note** : Permanent device damage may occur if Absolute Maximum Ratings are exceeded.
Functional operation should be restricted to the Recommended DC Operating Conditions detailed in this data sheet.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.
(1) Soldering temperature not to exceed 260°C for 10 seconds (Total thermal budget not to exceed 150°C for longer than 30 seconds).

**Caution** : Negative undershoots below –0.3V are not allowed on any pin while in the Battery Back-up mode.

## Operating and AC Measurement Conditions

| Parameter | HMNR5128D | HMNR5128DV | Unit |
|---|---|---|---|
| $V_{CC}$ Supply Voltage | 4.5 to 5.5 | 3.0 to 3.6 | V |
| Ambient Operating Temperature | 0 to 70 | 0 to 70 | °C |
| Load Capacitance ($C_L$) | 100 | 50 | pS |
| Input Rise and Fall Times | ≤ 5 | ≤ 5 | nS |
| Input Pulse Voltages | 0 to 3 | 0 to 3 | V |
| Input and Output Timing Ref. Voltages | 1.5 | 1.5 | V |

## AC Measurement Load Circuit




$C_L$ includes JIG capacitance

**Note** : 50pF for HMNR5128DV

## Capacitance

| Symbol | Parameter[1,2] | Min | Max | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | | 10 | pF |
| $C_{OUT}$[3] | Input/Output Capacitance | | 10 | pF |

**Note** :

1. Effective capacitance measured with power supply at 5V (HMNR5128D) or 3.3V (HMNR5128DV). Sampled only, not 100% tested.
2. At 25°C, f = 1MHz.
3. Outputs deselected.

## DC Characteristics

| Symbol | Parameter | Test Condition [1] | HMNR5128D | | | HMN5128DV | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | |
| $I_{LI}$ | Input Leakage Current | $0V \le V_{IN} \le V_{CC}$ | | | ±1 | | | ±1 | uA |
| $I_{LO}$[2] | Output Leakage Current | $0V \le V_{OUT} \le V_{CC}$ | | | ±1 | | | ±1 | uA |
| $I_{CC}$ | Supply Current | Outputs open | | 8 | 15 | | 4 | 10 | mA |
| $I_{CC1}$ | Supply Current (Standby) TTL | /CE=$V_{IH}$ | | | 5 | | | 3 | mA |
| $I_{CC2}$ | Supply Current (Standby) CMOS | /CE=$V_{CC}$-0.2 | | | 3 | | | 2 | mA |
| $I_{BAT}$ | Battery Current OSC ON | | | 575 | 800 | | 575 | 800 | nA |
| | Battery Current OSC OFF | | | 100 | | | | 100 | nA |
| $V_{IL}$ | Input Low Voltage | | -0.3 | | 0.8 | -0.3 | | 0.8 | V |
| $V_{IH}$ | Input High Voltage | | 2.2 | | VCC+ 0.3 | 2.0 | | VCC+ 0.3 | V |
| $V_{OL}$ | Output Low Voltage | $I_{OL}$=2.1mA | | | 0.4 | | | 0.4 | V |
| | Output Low Voltage (open drain) [4] | $I_{OL}$=10mA | | | 0.4 | | | 0.4 | V |
| $V_{OH}$ | Output High Voltage | $I_{OH}$=-1.0mA | 2.4 | | | 2.4 | | | V |
| $V_{OHB}$ | $V_{OH}$ Battery Back-up | $I_{OUT2}$=-1.0uA | 2.0 | | 3.6 | 2.0 | | 3.6 | V |
| $I_{OUT1}$ | $V_{OUT}$ Current (Active) | $V_{OUT1} > V_{CC}$-0.3 | | | 100 | | | 70 | mA |
| $I_{OUT2}$ | $V_{OUT}$ Current (Battery Back-up) | $V_{OUT2} > V_{BAT}$-0.3 | | | 100 | | | 100 | uA |
| $V_{PFD}$ | Power-fail Deselect Voltage | | 4.1 | 4.35 | 4.5 | 2.7 | 2.9 | 3.0 | V |
| $V_{SO}$ | Battery Back-up Switchover Voltage | | | 3.0 | | | $V_{PFD}$- 100 mV | | V |
| $V_{BAT}$ | Battery Voltage | | | 3.0 | | | 3.0 | | V |

**Note**: 1. Valid for Ambient Operating Temperature: TA =0 to 70°C or 40 to 85°C ;
VCC = 4.5 to 5.5V or 3.0 to 3.6V (except where noted).
2. Outputs deselected.

## OPERATING MODES

The 32-pin, 600mil DIP Hybrid houses a controller chip, SRAM, quartz crystal, and a long life lithium button cell in a single package. The clock locations contain the year, month, date, day, hour, minute, and second in 24 hour BCD format. Corrections for 28, 29 (leap year-compliant until the year 2100), 30, and 31 day months are made automatically. Byte 7FFF8h is the clock control register. This byte controls user access to the clock information and also stores the clock calibration setting. The seven clock bytes (7FFFFh-7FFF9h) are not the actual clock counters, they are memory locations consisting of READ/WRITE memory cells within the static RAM array. The HMNR5128D(V) includes a clock control circuit which updates the clock bytes with current information once per second. The information can be accessed by the user in the same manner as any other location in the static memory array. The HMNR5128D(V) also has its own Power-Fail Detect circuit. This control circuitry constantly monitors the supply voltage for an out of tolerance condition.
When $V_{CC}$ is out of tolerance, the circuit write protects the TIMEKEEPER register data and SRAM, providing data security in the midst of unpredictable system operation. As $V_{CC}$ falls, the control circuitry automatically switches to the battery, maintaining data and clock operation until valid power is restored.

## Operating Modes

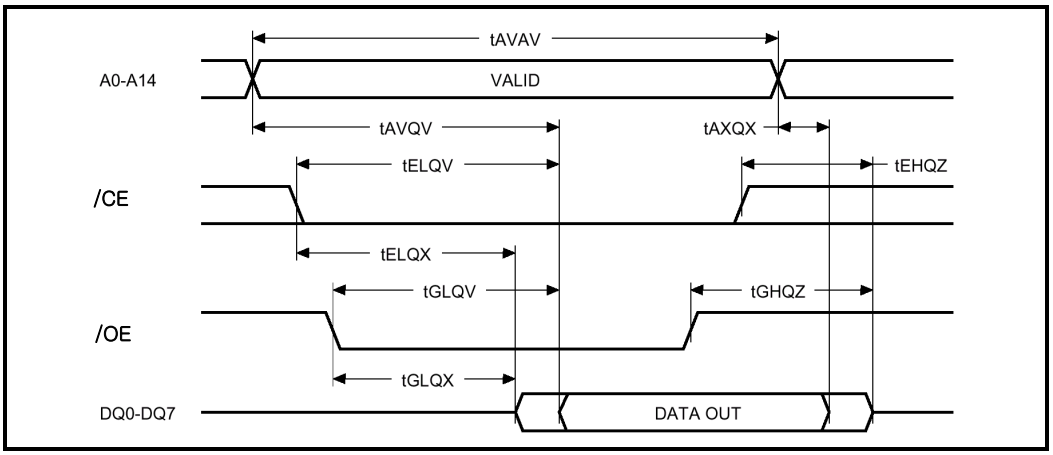
| Mode | VCC | /CE | /OE | /WE | DQ7 – DQ0 | Power |
|---|---|---|---|---|---|---|
| Deselect | 4.5V to 5.5V or 3.0V to 3.6V | VIH | X | X | High-Z | Standby |
| WRITE | | VIL | X | VIL | DIN | Active |
| READ | | VIL | VIL | VIH | DOUT | Active |
| READ | | VIL | VIH | VIH | High | Active |
| Deselect | $V_{SO}$ to $V_{PFD}$ (min) | X | X | X | High | CMOS Standby |
| Deselect | $\leq V_{SO}$ (1) | X | X | X | High | Battery Back-up |

Note : X = $V_{IH}$ or $V_{IL}$; $V_{SO}$ = Battery Back-up Switchover Voltage.

## READ Mode

The HMNR5128D(V) is in the READ Mode whenever /WE (WRITE Enable) is high and /CE (Chip Enable) is low. The unique address specified by the 15 Address Inputs defines which one of the 32,768 bytes of data is to be accessed. Valid data will be available at the Data I/O pins within Address Access Time ($t_{AVQV}$) after the last address input signal is stable, providing the /CE and /OE access times are also satisfied. If the /CE and /OE access times are not met, valid data will be available after the latter of the Chip Enable Access Times ($t_{ELQV}$) or Output Enable Access Time ($t_{GLQV}$). The state of the eight three-state Data I/O signals is controlled by /CE and /OE. If the outputs are activated before $t_{AVQV}$, the data lines will be driven to an indeterminate state until $t_{AVQV}$. If the Address Inputs are changed while /CE and /OE remain active, output data will remain valid for Output Data Hold Time ($t_{AXQX}$) but will go indeterminate until the next Address Access.

## READ Mode AC Waveforms




**Note** : /WE = High.

## READ Mode AC Characteristics

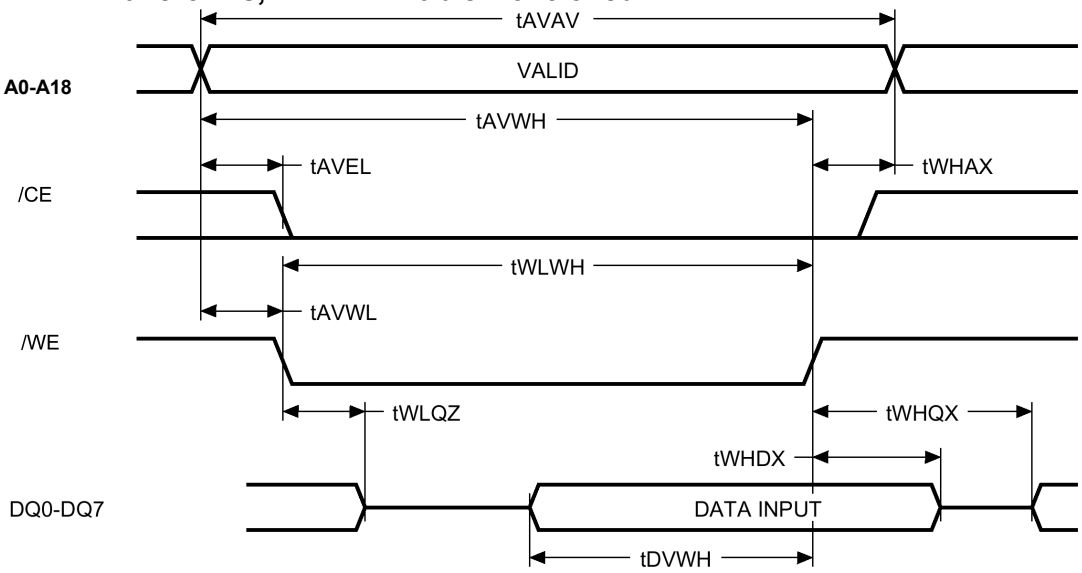
| Symbol | Parameter | HMN5128D -70 | | HMNR5128DV -85 | | Unit |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| $t_{AVAV}$ | READ Cycle Time | 70 | | 85 | | nS |
| $t_{AVQV}$ | Address Valid to Output Valid | | 70 | | 85 | nS |
| $t_{ELQV}$ | Chip Enable Low to Output Valid | | 70 | | 85 | nS |
| $t_{GLQV}$ | Output Enable Low to Output Valid | | 25 | | 35 | nS |
| $t_{ELQX}^{(2)}$ | Chip Enable Low to Output Transition | 5 | | 5 | | nS |
| $t_{GLQX}^{(2)}$ | Output Enable Low to Output Transition | 0 | | 0 | | nS |
| $t_{EHQZ}^{(2)}$ | Chip Enable High to Output Hi-Z | | 20 | | 25 | nS |
| $t_{GHQZ}^{(2)}$ | Output Enable High to Output Hi-Z | | 20 | | 25 | nS |
| $t_{AXQX}$ | Address Transition to Output Transition | 5 | | 5 | | nS |

Note: 1.Valid for Ambient Operating Temperature: TA = 0 to 70°C; VCC = 4.5 to 5.5V or 3.0 to 3.6V (except where noted).
2. CL = 5pF.

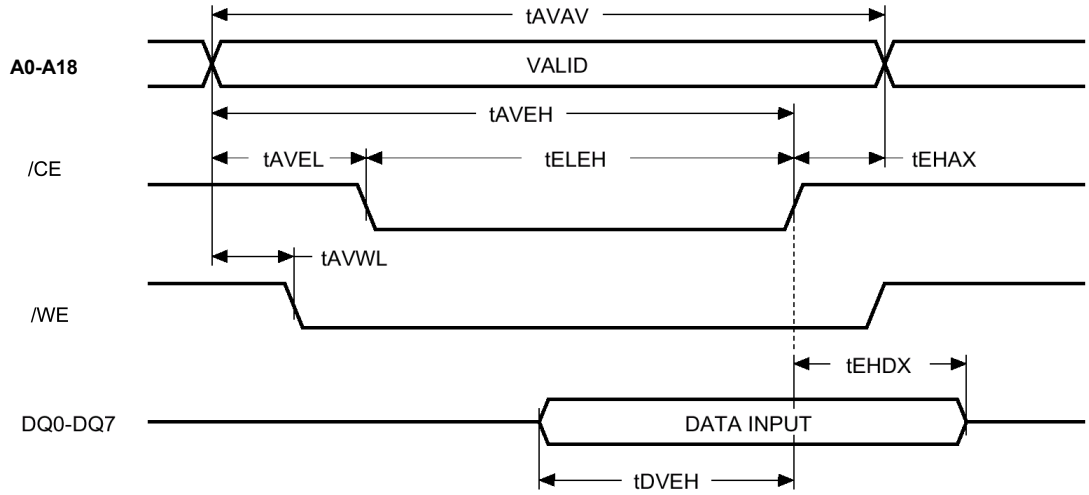
## WRITE Mode

The HMNR5128D(V) is in the WRITE Mode whenever /WE (WRITE Enable) and /CE (Chip Enable) are low state after the address inputs are stable. The start of a WRITE is referenced from the latter occurring falling edge of /WE or /CE. A WRITE is terminated by the earlier rising edge of /WE or /CE. The addresses must be held valid throughout the cycle. /CE or /WE must return high for a minimum of $t_{EHAX}$ from Chip Enable or $t_{WHAX}$ from WRITE Enable prior to the initiation of another READ or WRITE cycle. Data-in must be valid $t_{DVWH}$ prior to the end of WRITE and remain valid for $t_{WHDX}$ afterward. /OE should be kept high during WRITE cycles to avoid bus contention; although, if the output bus has been activated by a low on /CE and /OE a low on /WE will disable the outputs $t_{WLQZ}$ after /WE falls.

## WRITE AC Waveforms, WRITE Enable Controlled




## WRITE AC Waveforms, Chip Enable Controlled



## WRITE Mode AC Characteristics

| Symbol | Parameter[1] | HMN5128D -70 | | HMNR5128DV -85 | | Unit |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| $t_{AVAV}$ | WRITE Cycle Time | 70 | | 85 | | nS |
| $t_{AVWL}$ | Address Valid to WRITE Enable Low | 0 | | 0 | | nS |
| $t_{AVEL}$ | Address Valid to Chip Enable Low | 0 | | 0 | | nS |
| $t_{WLWH}$ | WRITE Enable Pulse Width | 45 | | 55 | | nS |
| $t_{ELEH}$ | Chip Enable Low to Chip Enable High | 50 | | 60 | | nS |
| $t_{WHAX}$ | WRITE Enable High to Address Transition | 0 | | 0 | | nS |
| $t_{EHAX}$ | Chip Enable High to Address Transition | 0 | | 0 | | nS |
| $t_{DVWH}$ | Input Valid to WRITE Enable High | 25 | | 30 | | nS |
| $t_{DVEH}$ | Input Valid to Chip Enable High | 25 | | 30 | | nS |
| $t_{WHDX}$ | WRITE Enable High to Input Transition | 0 | | 0 | | nS |
| $t_{EHDX}$ | Chip Enable High to Input Transition | 0 | | 0 | | nS |
| $t_{WLQZ}$[2,3] | WRITE Enable Low to Output High-Z | | 20 | | 25 | nS |
| $t_{AVWH}$ | Address Valid to WRITE Enable High | 55 | | 65 | | nS |
| $t_{AVEH}$ | Address Valid to Chip Enable High | 55 | | 65 | | nS |
| $t_{WHQX}$[2,3] | WRITE Enable High to Output Transition | 5 | | 5 | | nS |

**Note** : 1. Valid for Ambient Operating Temperature: TA = 0 to 70°C; VCC = 4.5 to 5.5V or 3.0 to 3.6V (except where noted).

2. CL = 5pF.

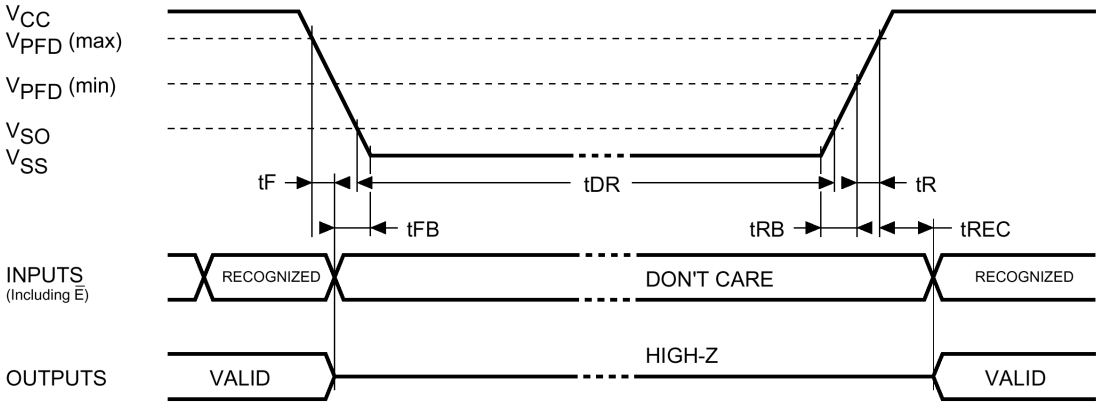
3. If /CE goes low simultaneously with /WE going low, the outputs remain in the high impedance state.

## Data Retention Mode

With valid $V_{CC}$ applied, the HMNR5128D(V) operates as a conventional Bytewide static RAM. Should the supply voltage decay, the RAM will automatically deselect, write protecting itself when $V_{CC}$ falls between $V_{PFD}$ (max), $V_{PFD}$ (min) window. All outputs become high impedance and all inputs are treated as "Don't care."

Note : A power failure during a WRITE cycle may corrupt data at the current addressed location, but does not jeopardize the rest of the RAM's content. At voltages below $V_{PFD}$ (min), the memory will be in a write protected state, provided the $V_{CC}$ fall time is not less than $t_F$. The HMNR5128D(V) may respond to transient noise spikes on $V_{CC}$ that cross into the deselect window during the time the device is sampling $V_{CC}$. Therefore, decoupling of the power supply lines is recommended. When $V_{CC}$ drops below $V_{SO}$, the control circuit switches power to the internal battery, preserving data and powering the clock. The internal energy source will maintain data in the HMNR5128D(V) for an accumulated period of at least 10 years at room temperature. As system power rises above $V_{SO}$, the battery is disconnected, and the power supply is switched to external $V_{CC}$ . Write protection continues until $V_{CC}$ reaches $V_{PFD}$ (min) plus $t_{REC}$ (min). Normal RAM operation can resume $t_{REC}$ after $V_{CC}$ exceeds $V_{PFD}$ (max).

## Power Down/Up Mode AC Waveforms




## Power Down/Up AC Characteristics

| Symbol | Parameter | | Min | Max | Unit |
|---|---|---|---|---|---|
| $t_F$ (2) | $V_{PFD}$ (max) to $V_{PFD}$ (min) $V_{CC}$ Fall Time | | 300 | | uS |
| $t_{FB}$ (3) | $V_{PFD}$ (min) to $V_{SS}$ $V_{CC}$ Fall Time | HMNR5128D | 10 | | uS |
| | | HMNR5128DV | 150 | | uS |
| $t_R$ | $V_{PFD}$ (min) to $V_{PFD}$ (max) $V_{CC}$ Rise Time | | 10 | | uS |
| $t_{REC}$ (4) | $V_{PFD}$ (max) to RST High | | 40 | 200 | uS |
| $t_{RB}$ | $V_{SS}$ to $V_{PFD}$ (min) $V_{CC}$ Rise Time | | 5 | | uS |

**Note** :

1. Valid for Ambient Operating Temperature: $T_A$ = 0 to 70°C; $V_{CC}$ = 4.5 to 5.5V or 3.0 to 3.6V (except where noted).
2. $V_{PFD}$ (max) to $V_{PFD}$ (min) fall time of less than tF may result in deselection/write protection not occurring until 200μs after $V_{CC}$ passes $V_{PFD}$ (min).
3. $V_{PFD}$ (min) to $V_{SS}$ fall time of less than $t_{FB}$ may cause corruption of RAM data.

## Power Down/Up Trip Points DC Characteristics

| Symbol | Parameter(1,2) | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{PFD}$ | Power-fail Deselect Voltage | HMNR5128D | 4.2 | 4.35 | 4.5 | V |
| | | HMNR5128DV | 2.7 | 2.9 | 3.0 | V |
| $V_{SO}$ | Battery Back-up Switchover Voltage | HMNR5128DV | | 3.0 | | V |
| | | HMNR5128DV | | $V_{PFD}$-100mV | | V |
| $T_{DR}$ (3) | Expected Data Retention Time | | 10 | | | YEARS |

Note: 1. All voltages referenced to $V_{SS}$ .

2. Valid for Ambient Operating Temperature: $T_A$ = 0 to 70°C; $V_{CC}$ = 4.5 to 5.5V or 3.0 to 3.6V (except where noted).

3. At 25°C.

## Register Map

| Address | Data | | | | | | | | Funtion / Range BCD Format | |
|---|---|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | | |
| 7FFFF | 10Years | | | | Year | | | | Year | 00-99 |
| 7FFFE | 0 | 0 | 0 | 10M | Month | | | | Month | 01-12 |
| 7FFFD | 0 | 0 | 10 Date | | Date : Day of Month | | | | Date | 01-31 |
| 7FFFC | 0 | FT | 0 | 0 | 0 | Day | | | Day | 01-07 |
| 7FFFB | 0 | 0 | 10 Hours | | Hours(24 Hour Format) | | | | Hours | 00-23 |
| 7FFFA | 0 | 10 Minutes | | | Minutes | | | | Minutes | 00-59 |
| 7FFF9 | ST | 10 Seconds | | | Seconds | | | | Seconds | 00-59 |
| 7FFF8 | W | R | S | Calibration | | | | | Control | |
| 7FFF7 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | |
| 7FFF6 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | |
| 7FFF5 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | |
| 7FFF4 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | |
| 7FFF3 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | |
| 7FFF2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | |
| 7FFF1 | 1000 Years | | | | 100 Years | | | | Century | 00-99 |
| 7FFF0 | 0 | 0 | 0 | BL | 0 | 0 | 0 | 0 | Flag | |

**Keys** :

R = READ Bit

W = WRITE Bit

ST = Stop Bit

0 = Must be set to ’0’

BL = Battery Low Flag

S = Sign Bit

## CLOCK OPERATIONS

The HMNR5128D(V) offers 16 internal registers which contain TIMEKEEPER, and Control data. These registers are memory locations which contain external (user accessible) and internal copies of the data. The external copies are independent of internal functions except that they are updated periodically by the simultaneous transfer of the incremented internal copy. TIMEKEEPER Registers store data in BCD. Control Registers store data in Binary Format.

### Reading the Clock

Updates to the TIMEKEEPER registers should be halted before clock data is read to prevent reading data in transition. The TIMEKEEPER cells in the RAM array are only data registers and not the actual clock counters, so updating the registers can be halted without disturbing the clock itself. Updating is halted when a ’1’ is written to the READ Bit, D6 in the Control Register (7FFF8h). As long as a ’1’ remains in that position, updating is halted. After a halt is issued, the registers reflect the count; that is, the day, date, and time that were current at the moment the halt command was is-sued. All of the TIMEKEEPER registers are updated simultaneously. A halt will not interrupt an update in progress. Updating occurs approximately 1 second after the READ Bit is reset to a ’0.’

## Setting the Clock

Bit D7 of the Control Register (7FFF8h) is the WRITE Bit. Setting the WRITE Bit to a ’1,’ like the READ Bit, halts updates to the TIMEKEEPER reg-isters. The user can then load them with the correct day, date, and time data in 24-hour BCD format. Resetting the WRITE Bit to a ’0’ then transfers the
values of all time registers (7FFFh-7FFF9h, 7FFF1h) to the actual TIMEKEEPER counters and allows normal operation to resume. After the WRITE Bit is reset, the next clock update will occur approximately one second later.
Note: Upon power-up following a power failure, both the WRITE Bit and the READ Bit will be reset to ’0.’

## Stopping and Starting the Oscillator

The oscillator may be stopped at any time. If the device is going to spend a significant amount of time on the shelf, the oscillator can be turned off to minimize current drain on the battery. The STOP Bit is located at Bit D7 within the Seconds Register (7FFF9h). Setting it to a ’1’ stops the oscillator. When reset to a ’0,’ the HMNR5128D(V) oscillator starts within one second.

Note : It is not necessary to set the WRITE Bit when setting or resetting the STOP Bit (ST).

## Calibrating the Clock

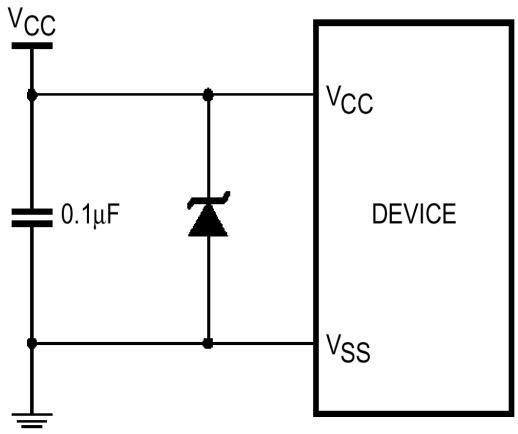
The HMNR5128D(V) is driven by a quartz controlled oscillator with a nominal frequency of 32,768Hz. The devices are factory calibrated at 25°C and tested for accuracy. Clock accuracy will not exceed 35 ppm (parts per million) oscillator frequency error at 25°C, which equates to about ±1.53 minutes per month. When the Calibration circuit is properly employed, accuracy improves to better than +1/-2 ppm at 25°C. The oscillation rate of crystals changes with temperature. The HMNR5128D(V) design employs periodic counter correction. The calibration circuit adds or subtracts counts from the oscillator divider circuit at the divide by 256 stage. The number of times pulses are blanked (subtracted, negative calibration) or split (added, positive calibration) depends upon the value loaded into the five Calibration bits found in the Control Register.
Adding counts speeds the clock up, subtracting counts slows the clock down. The Calibration bits occupy the five lower order bits (D4-D0) in the Control Register 7FFF8h. These bits can be set to represent any value between 0 and 31 in binary form. Bit D5 is a Sign bit; '1' indicates positive calibration, '0' indicates negative calibration. Calibration occurs within a 64 minute cycle. The first 62 minutes in the cycle may, once per minute, have one second either shortened by 128 or lengthened by 256 oscillator cycles. If a binary '1' is loaded into the register, only the first 2 minutes in the 64 minute cycle will be modified; if a binary 6 is loaded, the first 12 will be affected, and so on. Therefore, each calibration step has the effect of adding 512 or subtracting 256 oscillator cycles for every 125, 829, 120 actual oscillator cycles; that is, +4.068 or -2.034 ppm of adjustment per calibration step in the calibration register. Assuming that the oscillator is running at exactly 32,768Hz, each of the 31 increments in the Calibration byte would represent +10.7 or -5.35 seconds per month which corresponds to a total range of +5.5 or -2.75 minutes per month. One method for ascertaining how much calibration a given HMNR5128D(V) may require involves setting the clock, letting it run for a month and comparing it to a known accurate reference and recording deviation over a fixed period of time. This allows the designer to give the end user the ability to calibrate the clock as the environment requires, even if the final product is packaged in a nonuser serviceable enclosure. The designer could provide a simple utility that accesses the Calibration bits.

## Battery Low Warning

The HMNR5128D(V) automatically performs battery voltage monitoring upon power-up and at factory-programmed time intervals of approximately 24 hours. The Battery Low (BL) Bit, Bit D4 of Flags Register 7FFF0h, will be asserted if the battery voltage is found to be less than approximately 2.5V. The BL Bit will remain asserted until completion of battery replacement and subsequent battery low monitoring tests, either during the next power-up sequence or the next scheduled 24hour interval. If a battery low is generated during a power-up sequence,
this indicates that the battery is below approximately 2.5V and may not be able to maintain
data integrity in the SRAM. Data should be considered suspect and verified as correct. A fresh battery should be installed.
If a battery low indication is generated during the 24-hour interval check, this indicates that the battery is near end of life. However, data is not compromised
due to the fact that a nominal $V_{CC}$ is supplied. In order to insure data integrity during

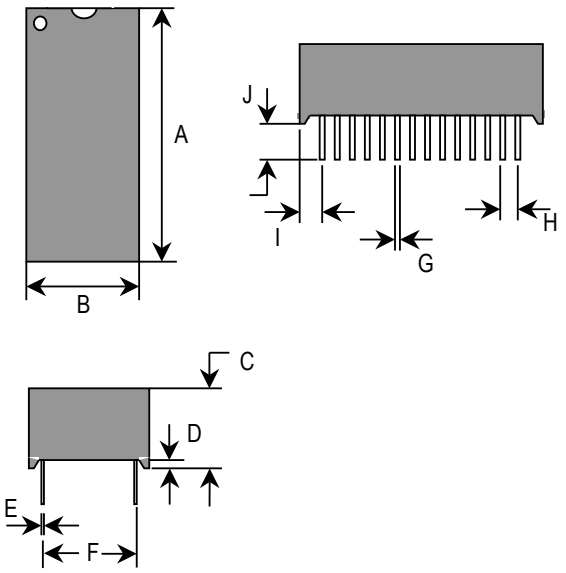
## Power Supply Decoupling and Undershoot Protection

Note: $I_{CC}$ transients, including those produced by output switching, can produce voltage fluctuations, resulting in spikes on the $V_{CC}$ bus. These transients can be reduced if capacitors are used to store energy which stabilizes the $V_{CC}$ bus. The energy stored in the bypass capacitors will be released as low going spikes are generated or energy will be absorbed when overshoots occur. A ceramic bypass capacitor value of 0.1uF is recommended in order to provide the needed filtering. In addition to transients that are caused by normal
SRAM operation, power cycling can generate negative voltage spikes on $V_{CC}$ that drive it to values below $V_{SS}$ by as much as one volt. These negative spikes can cause data corruption in the SRAM while in battery backup mode. To protect from these voltage spikes, ST recommends
connecting a schottky diode from $V_{CC}$ to $V_{SS}$ (cathode connected to $V_{CC}$, anode to $V_{SS}$). (Schottky diode 1N5817 is recommended for through hole and MBRS120T3 is recommended for surface mount).



## PACKAGE DIMENSION

| Dimension | Min | Max |
|---|---|---|
| A | 1.470 | 1.500 |
| B | 0.710 | 0.740 |
| C | 0.365 | 0.375 |
| D | 0.012 | - |
| E | 0.008 | 0.013 |
| F | 0.590 | 0.630 |
| G | 0.017 | 0.023 |
| H | 0.090 | 0.110 |
| I | 0.075 | 0.110 |
| J | 0.120 | 0.150 |




## ORDERING INFORMATION

**HM NR 5128 D V - 70 I**

- **Operating Temp. :** Blank = Commercial (0 to 70 °C )
  **I** = Industrial (-40 to 85°C)
- **Speed options :** 70 = 70 ns
  85 = 85 ns
- **Operating Voltage** : Blank = 5V
  **V** = 3.3V
- **Dip type package**
- **Device :** 512K x 8
- **Nonvolatile Timekeeping SRAM**
- **HANBit Memory Module**