128Mb DDR SDRAM

H5DU1262GTR

Revision History

Revision No.	History	Draft Date	Remark
0.1	First version	Feb. 2009	
1.0	Release	May 2009	

DESCRIPTION

The H5DU1262GTR is a 134,217,728-bit CMOS Double Data Rate(DDR) Synchronous DRAM, ideally suited for the main memory applications which requires large memory density and high bandwidth.

This Hynix 128Mb DDR SDRAMs offer fully synchronous operations referenced to both rising and falling edges of the clock. While all addresses and control inputs are latched on the rising edges of the CK (falling edges of the /CK), Data, Data strobes and Write data masks inputs are sampled on both rising and falling edges of it. The data paths are internally pipelined and 2-bit prefetched to achieve very high bandwidth. All input and output voltage levels are compatible with SSTL_2.

FEATURES

- V_{DD}, V_{DDQ} = 2.3V min ~ 2.7V max
  (Typical 2.5V Operation +/- 0.2V for DDR266, 333 ,400 and 500)
- All inputs and outputs are compatible with SSTL_2 interface
- Fully differential clock inputs (CK, /CK) operation
- Double data rate interface
- Source synchronous - data transaction aligned to bidirectional data strobe (DQS)
- x16 device has two bytewide data strobes (UDQS, LDQS) per each x8 I/O
- Data outputs on DQS edges when read (edged DQ) Data inputs on DQS centers when write (centered DQ)
- On chip DLL align DQ and DQS transition with CK transition
- DM mask write data-in at the both rising and falling edges of the data strobe
- All addresses and control inputs except data, data strobes and data masks latched on the rising edges of the clock
- Programmable CAS latency 2/2.5 (DDR266, 333) and 3/4 (DDR400, 500) supported
- Programmable burst length 2/4/8 with both sequential and interleave mode
- Internal four bank operations with single pulsed /RAS
- Auto refresh and self refresh supported
- t_{RAS} lock out function supported
- 4096 refresh cycles/64ms
- 66pin TSOP-II Lead-free and Halogen-free
- ROHS Compliant

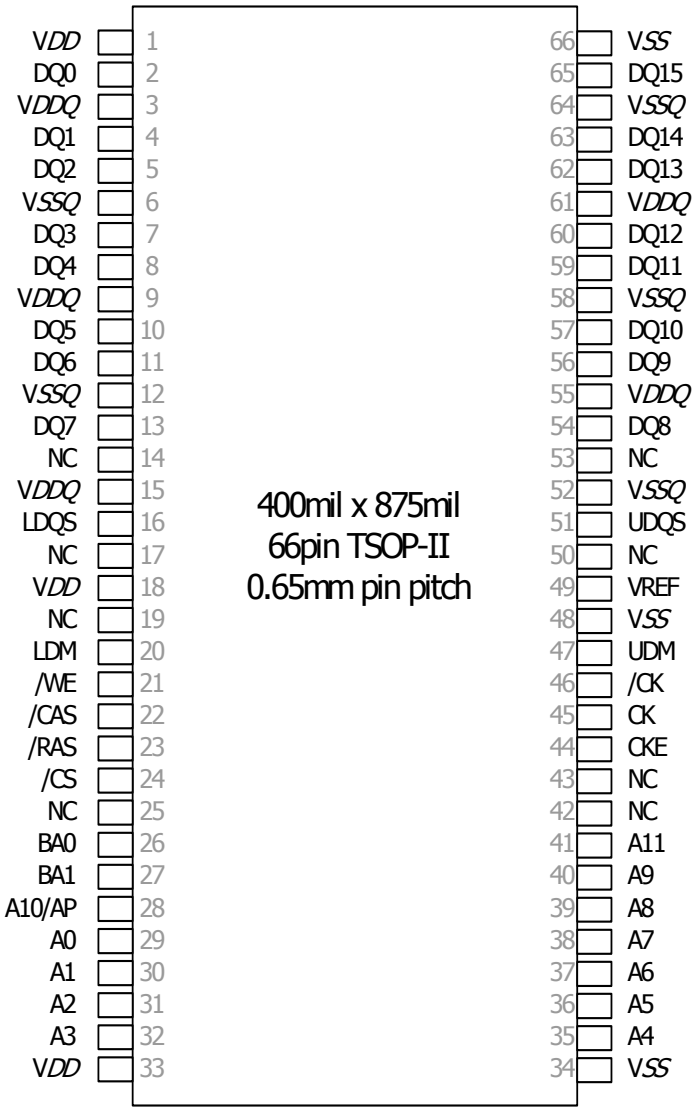
ORDERING INFORMATION

Part No.	Configuration	Package
H5DU1262GTR-XXX	8Mx16	66TSOP-II

OPERATING FREQUENCY

Grade	Clock Rate	Remark
- FA	250MHz@CL4	DDR500 (4-4-4)
- FB	250MHz@CL4	DDR500 (4-3-3)
- E3	200MHz@CL3	DDR400 (3-3-3)
- E4	200MHz@CL3	DDR400 (3-4-4)
- J3	166MHz@CL2.5	DDR333 (2.5-3-3)
- K2	133MHz@CL2	DDR266A (2-3-3)
- K3	133MHz@CL2.5	DDR266B (2.5-3-3)

PIN CONFIGURATION



ROW AND COLUMN ADDRESS INFORMATION

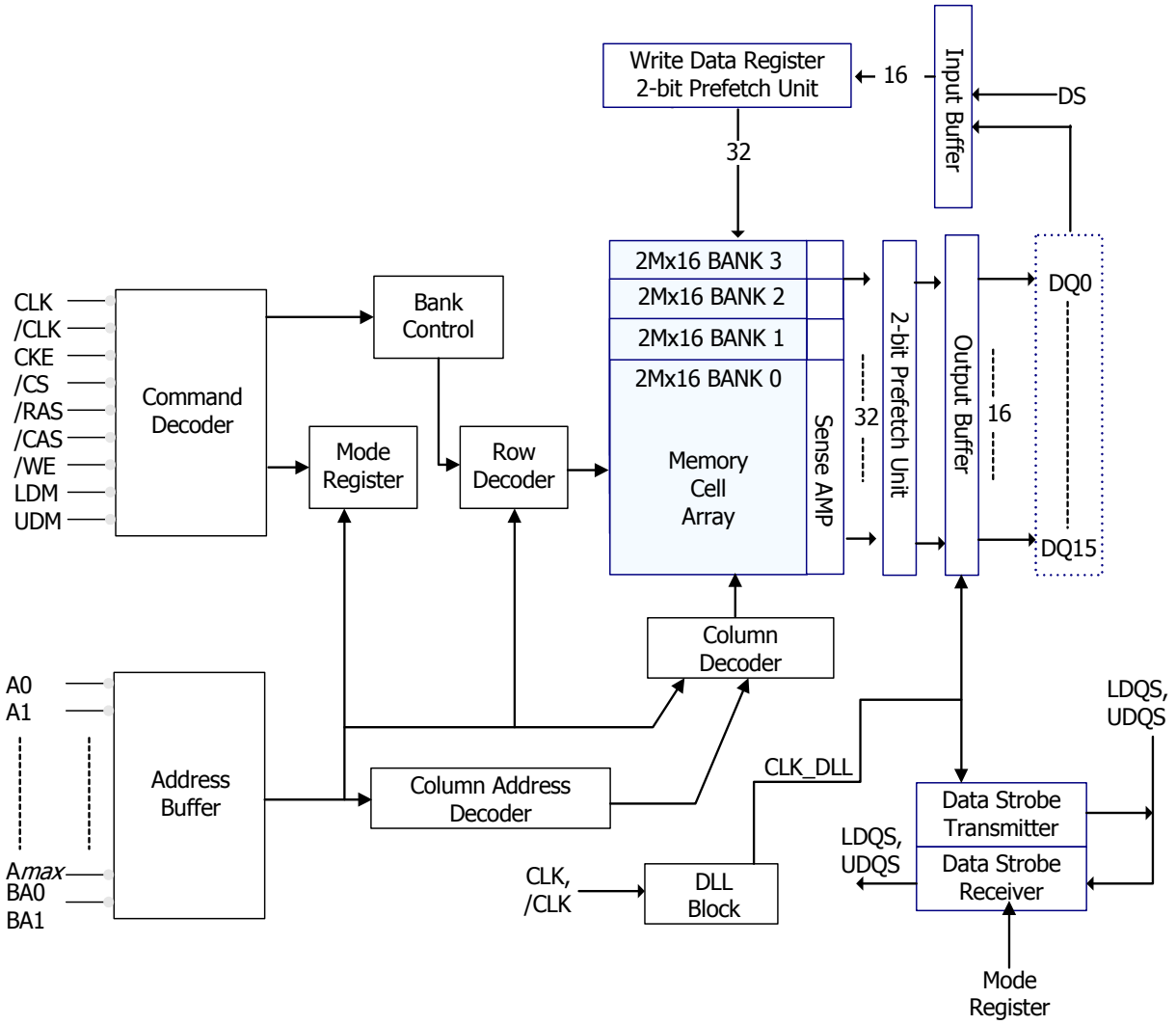
- Organization : 2M x 16 x 4banks
- Row Address : A0 - A11
- Column Address : A0 - A8
- Bank Address : BA0, BA1
- Auto Precharge Flag : A10
- Refresh : 4K

PIN DESCRIPTION

PIN	TYPE	DESCRIPTION
CK, /CK	Input	Clock: CK and /CK are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of /CK. Output (read) data is referenced to the crossings of CK and /CK (both directions of crossing).
CKE	Input	Clock Enable: CKE HIGH activates, and CKE LOW deactivates internal clock signals, and device input buffers and output drivers. Taking CKE LOW provides PRECHARGE POWER DOWN and SELF REFRESH operation (all banks idle), or ACTIVE POWER DOWN (row ACTIVE in any bank). CKE is synchronous for POWER DOWN entry and exit, and for SELF REFRESH entry. CKE is asynchronous for SELF REFRESH exit, and for output disable. CKE must be maintained high throughout READ and WRITE accesses. Input buffers, excluding CK, /CK and CKE are disabled during POWER DOWN. Input buffers, excluding CKE are disabled during SELF REFRESH. CKE is an SSTL_2 input, but will detect an LVCMOS LOW level after V*DD* is applied.
/CS	Input	Chip Select: Enables or disables all inputs except CK, /CK, CKE, DQS and DM. All commands are masked when Chip Select is registered high. Chip Select provides for external bank selection on systems with multiple banks. Chip Select is considered part of the command code.
BA0, BA1	Input	Bank Address Inputs: BA0 and BA1 define to which bank an ACTIVE, Read, Write or PRECHARGE command is being applied.
A0 ~ A11	Input	Address Inputs: Provide the row address for ACTIVE commands, and the column address and AUTO PRECHARGE bit for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 is sampled during a precharge command to determine whether the PRECHARGE applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by BA0, BA1. The address inputs also provide the op code during a MODE REGISTER SET command. BA0 and BA1 define which mode register is loaded during the MODE REGISTER SET command (MRS or EMRS).
/RAS, /CAS, /WE	Input	Command Inputs: /RAS, /CAS and /WE (along with /CS) define the command being entered.
DM (LDM,UDM)	Input	Input Data Mask: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with that input data during a WRITE access. DM is sampled on both edges of DQS. Although DM pins are input only, the DM loading matches the DQ and DQS loading. For the x16, LDM corresponds to the data on DQ0-Q7; UDM corresponds to the data on DQ8-Q15.
DQS (LDQS,UDQS)	I/O	Data Strobe: Output with read data, input with write data. Edge aligned with read data, centered in write data. Used to capture write data. For the x16, LDQS corresponds to the data on DQ0-Q7; UDQS corresponds to the data on DQ8-Q15.
DQ	I/O	Data input / output pin: Data bus
V*DD* / V*SS*	Supply	Power supply for internal circuits and input buffers.
V*DDQ* / V*SSQ*	Supply	Power supply for output buffers for noise immunity.
V*REF*	Supply	Reference voltage for inputs for SSTL interface.
NC	NC	No connection.

Functinal Block Diagram (8M x16)

4Banks x 2Mbit x 16I/O Double Data Rate Syncronous DRAM



SIMPLIFIED COMMAND TRUTH TABLE

Command		CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ADDR	A10 /AP	BA	Note
Extended Mode Register Set		H	X	L	L	L	L	OP code			1,2
Mode Register Set		H	X	L	L	L	L	OP code			1,2
Device Deselect		H	X	H	X	X	X	X			1
No Operation				L	H	H	H				
Bank Active		H	X	L	L	H	H	RA		V	1
Read		H	X	L	H	L	H	CA	L	V	1
Read with Autoprecharge									H		1,3
Write		H	X	L	H	L	L	CA	L	V	1
Write with Autoprecharge									H		1,4
Precharge All Banks		H	X	L	L	H	L	X	H	X	1,5
Precharge selected Bank									L	V	1
Read Burst Stop		H	X	L	H	H	L	X			1
Auto Refresh		H	H	L	L	L	H	X			1
Self Refresh	Entry	H	L	L	L	L	H	X			1
	Exit	L	H	H	X	X	X				1
				L	H	H	H				
Precharge Power Down Mode	Entry	H	L	H	X	X	X	X			1
				L	H	H	H				1
	Exit	L	H	H	X	X	X				1
				L	H	H	H				1
Active Power Down Mode	Entry	H	L	H	X	X	X	X			1
				L	V	V	V				1
	Exit	L	H	X							1

(H=Logic High Level, L=Logic Low Level, X=Don't Care, V=Valid Data Input, OP Code=Operand Code, NOP=No Operation)

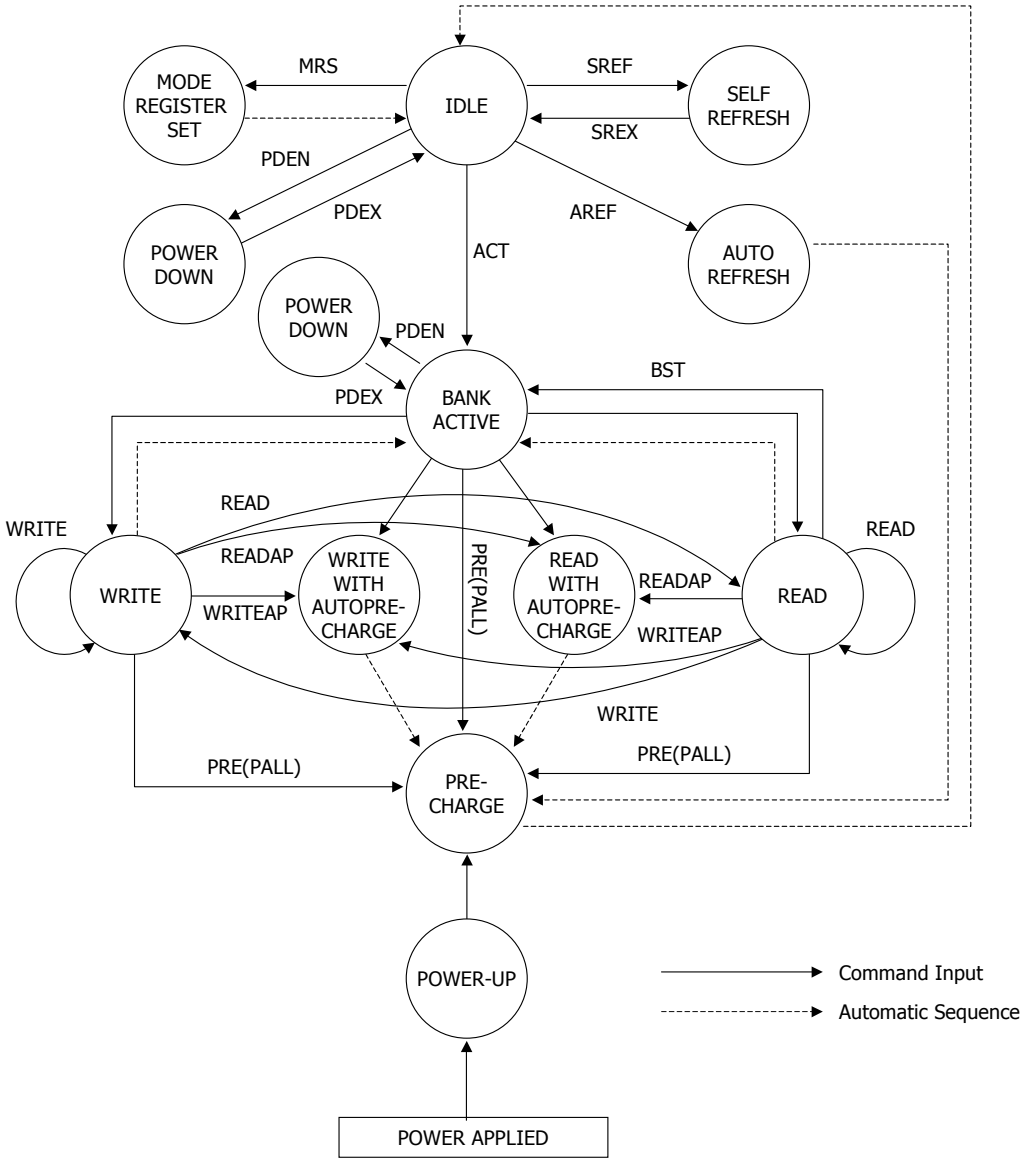
Note :
1. UDM, LDM states are Don't Care. Refer to below Write Mask Truth Table.(note 6)
2. OP Code(Operand Code) consists of A0~A11 and BA0~BA1 used for Mode Register setting during Extended MRS or MRS. Before entering Mode Register Set mode, all banks must be in a precharge state and MRS command can be issued after tRP period from Prechagre command.
3. If a Read with Auto-precharge command is detected by memory component in CK(n), then there will be no command presented to activate bank until CK(n+BL/2+tRP).
4. If a Write with Auto-precharge command is detected by memory component in CK(n), then there will be no command presented to activate bank until CK(n+BL/2+1+tDPL+tRP). Last Data-In to Prechage delay(tDPL) which is also called Write Recovery Time(tWR) is needed to guarantee that the last data have been completely written.
5. If A10/AP is High when Precharge command being issued, BA0/BA1 are ignored and all banks are selected to be precharged.
6. In here, Don't Care means logical value only, it doesn't mean 'Don't care for DC level of each signals'. DC level should be out of V_{IHmin} ~ V_{ILmax}

WRITE MASK TRUTH TABLE

Function	CKEn-1	CKEn	/CS, /RAS, /CAS, /WE	DM	ADDR	A10/AP	BA	Note
Data Write	H	X	X	L	X			1,2
Data-In Mask	H	X	X	H	X			1,2

Note :
1. Write Mask command masks burst write data with reference to LDQS/UDQS(Data Strobes) and it is not related with read data. In case of x16 data I/O, LDM and UDM control lower byte(DQ0~7) and Upper byte(DQ8~15) respectively.
2. In here, Don't Care means logical value only, it doesn't mean 'Don't care for DC level of each signals'. DC level should be out of V_{IHmin} ~ V_{ILmax}

SIMPLIFIED STATE DIAGRAM



POWER-UP SEQUENCE AND DEVICE INITIALIZATION

DDR SDRAMs must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation. Power must first be applied to V*DD*, then to V*DDQ*, and finally to VREF (and to the system VTT). VTT must be applied after V*DDQ* to avoid device latch-up, which may cause permanent damage to the device. VREF can be applied anytime after V*DDQ*, but is expected to be nominally coincident with VTT. Except for CKE, inputs are not recognized as valid until after VREF is applied. CKE is an SSTL_2 input, but will detect an LVCMOS LOW level after V*DD* is applied. Maintaining an LVCMOS LOW level on CKE during power-up is required to guarantee that the DQ and DQS outputs will be in the High-Z state, where they will remain until driven in normal operation (by a read access). After all power supply and reference voltages are stable, and the clock is stable, the DDR SDRAM requires a 200us delay prior to applying an executable command.

Once the 200us delay has been satisfied, a DESELECT or NOP command should be applied, and CKE should be brought HIGH. Following the NOP command, a PRECHARGE ALL command should be applied. Next a EXTENDED MODE REGISTER SET command should be issued for the Extended Mode Register, to enable the DLL, then a MODE REGISTER SET command should be issued for the Mode Register, to reset the DLL, and to program the operating parameters. After the DLL reset, tXSRD(DLL locking time) should be satisfied for read command. After the Mode Register set command, a PRECHARGE ALL command should be applied, placing the device in the all banks idle state.

Once in the idle state, two AUTO REFRESH cycles must be performed. Additionally, a MODE REGISTER SET command for the Mode Register, with the reset DLL bit deactivated low (i.e. to program operating parameters without resetting the DLL) must be performed. Following these cycles, the DDR SDRAM is ready for normal operation.

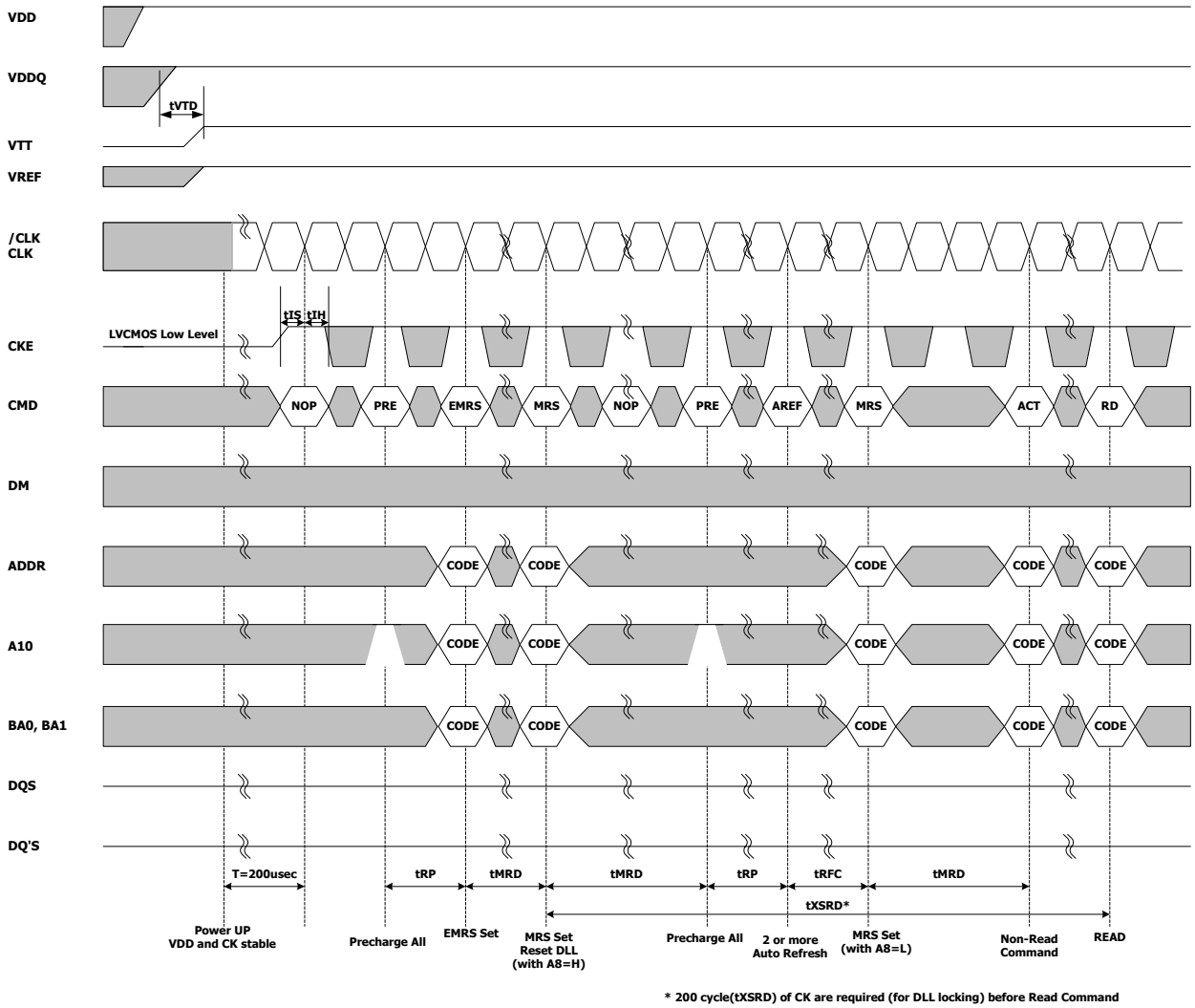
1. Apply power - V*DD*, V*DDQ*, VTT, VREF in the following power up sequencing and attempt to maintain CKE at LVCMOS low state. (All the other input pins may be undefined.)

   - V*DD* and V*DDQ* are driven from a single power converter output.
   - VTT is limited to 1.44V (reflecting V*DDQ*(max)/2 + 50mV VREF variation + 40mV VTT variation.
   - VREF tracks V*DDQ*/2.
   - If the above criteria cannot be met by the system design, then the following sequencing and voltage relationship must be adhered to during power up.

Voltage description	Sequencing	Voltage relationship to avoid latch-up
V*DDQ*	After or with V*DD*	< V*DD* + 0.3V
VTT	After or with V*DDQ*	< V*DDQ* + 0.3V
VREF	After or with V*DDQ*	< V*DDQ* + 0.3V

2. Start clock and maintain stable clock for a minimum of 200usec.
3. After stable power and clock, apply NOP condition and take CKE high.
4. Issue Extended Mode Register Set (EMRS) to enable DLL.
5. Issue Mode Register Set (MRS) to reset DLL and set device to idle state with bit A8=high. (An additional 200 cycles(tXSRD) of clock are required for locking DLL)
6. Issue Precharge commands for all banks of the device.
7. Issue 2 or more Auto Refresh commands.
8. Issue a Mode Register Set command to initialize the mode register with bit A8 = Low

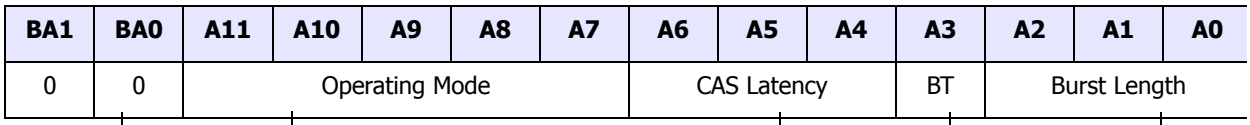
Power-Up Sequence



* 200 cycle(tXSRD) of CK are required (for DLL locking) before Read Command

MODE REGISTER SET (MRS)

The mode register is used to store the various operating modes such as /CAS latency, addressing mode, burst length, burst type, test mode, DLL reset. The mode register is programed via MRS command. This command is issued by the low signals of /RAS, /CAS, /CS, /WE and BA0. This command can be issued only when all banks are in idle state and CKE must be high at least one cycle before the Mode Register Set Command can be issued. Two cycles are required to write the data in mode register. During the MRS cycle, any command cannot be issued. Once mode register field is determined, the information will be held until reset by another MRS command.



BA1	BA0	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	0	Operating Mode					CAS Latency			BT	Burst Length		

BA0	MRS Type
0	MRS
1	EMRS

A6	A5	A4	CAS Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	1.5
1	1	0	2.5
1	1	1	Reserved

A3	Burst Type
0	Sequential
1	Interleave

A12~A9	A8	A7	A6~A0	Operating Mode
0	0	0	Valid	Normal Operation
0	1	0	Valid	Normal Operation/ Reset DLL
0	0	1	VS	Vendor specific Test Mode
-	-	-	-	All other states reserved

A2	A1	A0	Burst Length	
			Sequential	Interleave
0	0	0	Reserved	Reserved
0	0	1	2	2
0	1	0	4	4
0	1	1	8	8
1	0	0	Reserved	Reserved
1	0	1	Reserved	Reserved
1	1	0	Reserved	Reserved
1	1	1	Reserved	Reserved

BURST DEFINITION

Burst Length	Starting Address (A2,A1,A0)	Sequential	Interleave
2	XX0	0, 1	0, 1
	XX1	1, 0	1, 0
4	X00	0, 1, 2, 3	0, 1, 2, 3
	X01	1, 2, 3, 0	1, 0, 3, 2
	X10	2, 3, 0, 1	2, 3, 0, 1
	X11	3, 0, 1, 2	3, 2, 1, 0
8	000	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7
	001	1, 2, 3, 4, 5, 6, 7, 0	1, 0, 3, 2, 5, 4, 7, 6
	010	2, 3, 4, 5, 6, 7, 0, 1	2, 3, 0, 1, 6, 7, 4, 5
	011	3, 4, 5, 6, 7, 0, 1, 2	3, 2, 1, 0, 7, 6, 5, 4
	100	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3
	101	5, 6, 7, 0, 1, 2, 3, 4	5, 4, 7, 6, 1, 0, 3, 2
	110	6, 7, 0, 1, 2, 3, 4, 5	6, 7, 4, 5, 2, 3, 0, 1
	111	7, 0, 1, 2, 3, 4, 5, 6	7, 6, 5, 4, 3, 2, 1, 0

BURST LENGTH & TYPE

Read and write accesses to the DDR SDRAM are burst oriented, with the burst length being programmable. The burst length determines the maximum number of column locations that can be accessed for a given Read or Write command. Burst lengths of 2, 4 or 8 locations are available for both the sequential and the interleaved burst types. Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

When a Read or Write command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within this block, meaning that the burst wraps within the block if a boundary is reached. The block is uniquely selected by A1-Ai when the burst length is set to two, by A2 -Ai when the burst length is set to four and by A3 -Ai when the burst length is set to eight (where Ai is the most significant column address bit for a given configuration). The remaining (least significant) address bit(s) is (are) used to select the starting location within the block. The programmed burst length applies to both Read and Write bursts.

Accesses within a given burst may be programmed to be either sequential or interleaved; this is referred to as the burst type and is selected via bit A3. The ordering of accesses within a burst is determined by the burst length, the burst type and the starting column address, as shown in Burst Definition Table

CAS LATENCY

The Read latency or CAS latency is the delay in clock cycles between the registration of a Read command and the availability of the first burst of output data. The latency can be programmed 2 or 2.5 clocks for DDR266/333 and 3 or 4 clocks for DDR400 and DDR500 product.

If a Read command is registered at clock edge n, and the latency is m clocks, the data is available nominally coincident with clock edge n + m.

Reserved states should not be used as unknown operation or incompatibility with future versions may result.

DLL RESET

The DLL must be enabled for normal operation. DLL enable is required during power up initialization, and upon returning to normal operation after having disabled the DLL for the purpose of debug or evaluation. The DLL is automatically disabled when entering self refresh operation and is automatically re-enabled upon exit of self refresh operation. Any time the DLL is enabled, 200 clock cycles must occur to allow time for the internal clock to lock to the externally applied clock before an any command can be issued.

OUTPUT DRIVER IMPEDANCE CONTROL

The normal drive strength for all outputs is specified to be SSTL_2, Class II. Hynix also supports a half strength driver option, intended for lighter load and/or point-to-point environments. Selection of the half strength driver option will reduce the output drive strength by 50% of that of the full strength driver. I-V curves for both the full strength driver and the half strength driver are included in this document.

EXTENDED MODE REGISTER SET (EMRS)

The Extended Mode Register controls functions beyond those controlled by the Mode Register; these additional functions include DLL enable/disable, output driver strength selection(optional). These functions are controlled via the bits shown below. The Extended Mode Register is programmed via the Mode Register Set command (BA0=1 and BA1=0) and will retain the stored information until it is programmed again or the device loses power.

The Extended Mode Register must be loaded when all banks are idle and no bursts are in progress, and the controller must wait the specified time before initiating any subsequent operation. Violating either of these requirements will result in unspecified operation.

BA1	BA0	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	1	Operating Mode									0*	DS	DLL

BA0	MRS Type
0	MRS
1	EMRS

A0	DLL enable
0	Enable
1	Disable

A1	Output Driver Impedance Control
0	Full Strength Driver
1	Half Strength Driver

An~A3	A2~A0	Operating Mode
0	Valid	Normal Operation
_	_	All other states reserved

* This part do not support/QFC function, A2 must be programmed to Zero.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Operating Temperature (Ambient)	TA	0 ~ 70	°C
Storage Temperature	TSTG	-55 ~ 150	°C
Voltage on VDD relative to VSS	VDD	-1.0 ~ 3.6	V
Voltage on VDDQ relative to VSS	VDDQ	-1.0 ~ 3.6	V
Voltage on inputs relative to VSS	VINPUT	-1.0 ~ 3.6	V
Voltage on I/O pins relative to VSS	VIO	-0.5 ~3.6	V
Output Short Circuit Current	IOS	50	mA
Soldering Temperature · Time	TSOLDER	260 · 10	°C · Sec

Note: Operation at above absolute maximum rating can adversely affect device reliability

DC OPERATING CONDITIONS (TA=0 to 70 °C, Voltage referenced to VSS = 0V)

Parameter		Symbol	Min	Typ.	Max	Unit
Power Supply Voltage (DDR266, 333, 400, 500)		VDD	2.3	2.5	2.7	V
Power Supply Voltage (DDR266, 333, 400, 500)[1]		VDDQ	2.3	2.5	2.7	V
Input High Voltage		VIH	VREF + 0.15	-	VDDQ + 0.3	V
Input Low Voltage[2]		VIL	-0.3	-	VREF - 0.15	V
Termination Voltage		VTT	VREF - 0.04	VREF	VREF + 0.04	V
Reference Voltage[3]		VREF	0.49*VDDQ	0.5*VDDQ	0.51*VDDQ	V
Input Voltage Level, CK and $\overline{CK}$ inputs		VIN(DC)	-0.3	-	VDDQ+0.3	V
Input Differential Voltage, CK and $\overline{CK}$ inputs[4]		VID(DC)	0.36	-	VDDQ+0.6	V
V-I Matching: Pullup to Pulldown Current Ratio[5]		VI(RATIO)	0.71	-	1.4	-
Input Leakage Current[6]		ILI	-2	-	2	uA
Output Leakage Current[7]		ILO	-5	-	5	uA
Normal Strength Output Driver (VOUT=VTT ± 0.84)	Output High Current (min VDDQ, min VREF, min VTT)	IOH	-16.8	-	-	mA
	Output Low Current (min VDDQ, max VREF, max VTT)	IOL	16.8	-	-	mA
Half Strength Output Driver (VOUT=VTT ± 0.68)	Output High Current (min VDDQ, min VREF, min VTT)	IOH	-13.6	-	-	mA
	Output Low Current (min VDDQ, max VREF, max VTT)	IOL	13.6	-	-	mA

Note:
1. VDDQ must not exceed the level of VDD.
2. VIL (min) is acceptable -1.5V AC pulse width with ≤ 5ns of duration.
3. V*REF* is expected to be equal to 0.5*VDDQ of the transmitting device, and to track variations in the dc level of the same. Peak to peak noise on VREF may not exceed ± 2% of the DC value.
4. VID is the magnitude of the difference between the input level on CK and the input level on /CK.

5. The ratio of the pullup current to the pulldown current is specified for the same temperature and voltage, over the entire temperature and voltage range, for device drain to source voltages from 0.25V to 1.0V. For a given output, it represents the maximum difference between pullup and pulldown drivers due to process variation. The full variation in the ratio of the maximum to minimum pullup and pulldown current will not exceed 1/7 for device drain to source voltages from 0.1 to 1.0.
6. VIN=0 to VDD, All other pins are not tested under VIN =0V.
7. DQs are disabled, VOUT=0 to VDDQ

IDD SPECIFICATION AND CONDITIONS (TA=0 to 70 °C, Voltage referenced to VSS = 0V)

Test Conditions

Test Condition	Symbol
Operating Current: One bank; Active - Precharge; tRC=tRC(min); tCK=tCK(min); DQ,DM and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	IDD0
Operating Current: One bank; Active - Read - Precharge; Burst Length=2; tRC=tRC(min); tCK=tCK(min); address and control inputs changing once per clock cycle	IDD1
Precharge Power Down Standby Current: All banks idle; Power down mode; CKE=Low, tCK=tCK(min)	IDD2P
Idle Standby Current: /CS=High, All banks idle; tCK=tCK(min); CKE=High; address and control inputs changing once per clock cycle. VIN=VREF for DQ, DQS and DM	IDD2F
Idle Quiet Standby Current: /CS>=Vih(min); All banks idle; CKE>=Vih(min); Addresses and other control inputs stable, Vin=Vref for DQ, DQS and DM	IDD2Q
Active Power Down Standby Current: One bank active; Power down mode; CKE=Low, tCK=tCK(min)	IDD3P
Active Standby Current: /CS=HIGH; CKE=HIGH; One bank; Active-Precharge; tRC=tRAS(max); tCK=tCK(min); DQ, DM and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle	IDD3N
Operating Current: Burst=2; Reads; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; tCK=tCK(min); IOUT=0mA	IDD4R
Operating Current: Burst=2; Writes; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; tCK=tCK(min); DQ, DM and DQS inputs changing twice per clock cycle	IDD4W
Auto Refresh Current: tRC=tRFC(min) - 8*tCK for DDR200 at 100Mhz, 10*tCK for DDR266A & DDR266B at 133Mhz; distributed refresh tRC=tRFC(min) - 14*tCK for DDR400 at 200Mhz	IDD5
Self Refresh Current: CKE =< 0.2V; External clock on; tCK=tCK(min)	IDD6
Operating Current - Four Bank Operation: Four bank interleaving with BL=4, Refer to the following page for detailed test condition	IDD7

DC CHARACTERISTICS II (TA=0 to 70 °C, Voltage referenced to VSS = 0V)

8Mx16 (2M x4Bank x16I/O)

Parameter	Symbol	Test Condition	Speed		Unit	Note
			FA	FB		
			250		MHz	
Operating Current	IDD0	One bank; Active - Precharge ; tRC=tRC(min); tCK=tCK(min) ; DQ,DM and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	130		mA	
Operating Current	IDD1	One bank; Active - Read - Precharge; Burst Length=2; tRC=tRC(min); tCK=tCK(min); address and control inputs changing once per clock cycle	140		mA	
Precharge Power Down Standby Current	IDD2P	All banks idle; Power down mode; CKE=Low, tCK=tCK(min)	10		mA	
Idle Standby Current	IDD2F	/CS=High, All banks idle; tCK=tCK(min); CKE=High; address and control inputs changing once per clock cycle. VIN=VREF for DQ, DQS and DM	70		mA	
Idle Quiet Standby Current	IDD2Q	/CS>=VIH(min); All banks idle; CKE>=VIH(min); Addresses and other control inputs stable, VIN=Vref for DQ, DQS and DM	70		mA	
Active Power Down Standby Current	IDD3P	One bank active; Power down mode; CKE=Low, tCK=tCK(min)	20		mA	
Active Standby Current	IDD3N	/CS=HIGH; CKE=HIGH; One bank; Active-Precharge; tRC=tRAS(max); tCK=tCK(min); DQ, DM and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle	70		mA	

- Continue

Parameter	Symbol	Test Condition	Speed		Unit	Note
			FA	FB		
			250		MHz	
Operating Current	IDD4R	Burst=2; Reads; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; tCK=tCK(min); IOUT=0mA	210		mA	
Operating Current	IDD4W	Burst=2; Writes; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; tCK=tCK(min); DQ, DM and DQS inputs changing twice per clock cycle	210			
Auto Refresh Current	IDD5	tRC=tRFC(min) - 14*tCK for DDR400 at 200Mhz	210		mA	
Self Refresh Current	IDD6	CKE =< 0.2V; External clock on; tCK=tCK(min)	3		mA	
Operating Current - Four Bank Operation	IDD7	Four bank interleaving with BL=4, Refer to the following page for detailed test condition	300		mA	

DC CHARACTERISTICS II (TA=0 to 70 °C, Voltage referenced to VSS = 0V)

8Mx16 (2M x4Bank x16I/O)

Parameter	Symbol	Test Condition	Speed		Unit	Note
			E3	E4		
			200		MHz	
Operating Current	IDD0	One bank; Active - Precharge ; tRC=tRC(min); tCK=tCK(min) ; DQ,DM and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	120		mA	
Operating Current	IDD1	One bank; Active - Read - Precharge; Burst Length=2; tRC=tRC(min); tCK=tCK(min); address and control inputs changing once per clock cycle	120		mA	
Precharge Power Down Standby Current	IDD2P	All banks idle; Power down mode; CKE=Low, tCK=tCK(min)	10		mA	
Idle Standby Current	IDD2F	/CS=High, All banks idle; tCK=tCK(min); CKE=High; address and control inputs changing once per clock cycle. VIN=VREF for DQ, DQS and DM	60		mA	
Idle Quiet Standby Current	IDD2Q	/CS>=VIH(min); All banks idle; CKE>=VIH(min); Addresses and other control inputs stable, VIN=Vref for DQ, DQS and DM	60		mA	
Active Power Down Standby Current	IDD3P	One bank active; Power down mode; CKE=Low, tCK=tCK(min)	20		mA	
Active Standby Current	IDD3N	/CS=HIGH; CKE=HIGH; One bank; Active-Precharge; tRC=tRAS(max); tCK=tCK(min); DQ, DM and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle	70		mA	

- Continue

Parameter	Symbol	Test Condition	Speed		Unit	Note
			E3	E4		
			200		MHz	
Operating Current	IDD4R	Burst=2; Reads; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; tCK=tCK(min); IOUT=0mA	200		mA	
Operating Current	IDD4W	Burst=2; Writes; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; tCK=tCK(min); DQ, DM and DQS inputs changing twice per clock cycle	200			
Auto Refresh Current	IDD5	tRC=tRFC(min) - 14*tCK for DDR400 at 200Mhz	200		mA	
Self Refresh Current	IDD6	CKE =< 0.2V; External clock on; tCK=tCK(min)	3		mA	
Operating Current - Four Bank Operation	IDD7	Four bank interleaving with BL=4, Refer to the following page for detailed test condition	300		mA	

DC CHARACTERISTICS II (TA=0 to 70 °C, Voltage referenced to VSS = 0V)

8Mx16 (2M x4Bank x16I/O)

Parameter	Symbol	Test Condition	Speed			Unit	Note
			J3	K2	K3		
			166	133	133	MHz	
Operating Current	IDD0	One bank; Active - Precharge ; tRC=tRC(min); tCK=tCK(min) ; DQ,DM and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	110	100	100	mA	
Operating Current	IDD1	One bank; Active - Read - Precharge; Burst Length=2; tRC=tRC(min); tCK=tCK(min); address and control inputs changing once per clock cycle	110	100	100	mA	
Precharge Power Down Standby Current	IDD2P	All banks idle; Power down mode; CKE=Low, tCK=tCK(min)	10	10	10	mA	
Idle Standby Current	IDD2F	/CS=High, All banks idle; tCK=tCK(min); CKE=High; address and control inputs changing once per clock cycle. VIN=VREF for DQ, DQS and DM	50	45	45	mA	
Idle Quiet Standby Current	IDD2Q	/CS>=VIH(min); All banks idle; CKE>=VIH(min); Addresses and other control inputs stable, VIN=Vref for DQ, DQS and DM	60	60	60	mA	
Active Power Down Standby Current	IDD3P	One bank active; Power down mode; CKE=Low, tCK=tCK(min)	20	20	20	mA	
Active Standby Current	IDD3N	/CS=HIGH; CKE=HIGH; One bank; Active-Precharge; tRC=tRAS(max); tCK=tCK(min); DQ, DM and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle	60	50	50	mA	

- Continue

Parameter	Symbol	Test Condition	Speed			Unit	Note
			J3	K2	K3		
			166	133	133	MHz	
Operating Current	IDD4R	Burst=2; Reads; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; tCK=tCK(min); IOUT=0mA	160	150	150	mA	
Operating Current	IDD4W	Burst=2; Writes; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; tCK=tCK(min); DQ, DM and DQS inputs changing twice per clock cycle	160	150	150		
Auto Refresh Current	IDD5	tRC=tRFC(min) - 14*tCK for DDR400 at 200Mhz	180	170	170	mA	
Self Refresh Current	IDD6	CKE =< 0.2V; External clock on; tCK=tCK(min)	3	3	3	mA	
Operating Current - Four Bank Operation	IDD7	Four bank interleaving with BL=4, Refer to the following page for detailed test condition	250	230	230	mA	

DETAILED TEST CONDITIONS FOR DDR SDRAM IDD1 & IDD7

IDD1 : Operating current: One bank operation

1. Typical Case : VDD = 2.6V, T=25 ^{o}C
2. Worst Case : VDD = 2.7V, T= 0 ^{o}C
3. Only one bank is accessed with tRC(min), Burst Mode, Address and Control inputs on NOP edge are changing once per clock cycle. Iout = 0mA
4. Timing patterns

   - DDR400(200Mhz, CL=3) : tCK = 5ns, CL = 3, BL = 4, tRCD = 3*tCK, tRC = 11*tCK, tRAS = 8*tCK
   Read : A0 N N R0 N N N P0 N N A0 N - repeat the same timing with random add

   Legend : A=Activate, R=Read, W=Write, P=Precharge, N=NOP

IDD7 : Operating current: Four bank operation

1. Typical Case : VDD = 2.6V, T=25 ^{o}C
2. Worst Case : VDD= 2.7V, T= 0 ^{o}C
3. Four banks are being interleaved with tRC(min), Burst Mode, Address and Control inputs on NOP edge are not changing. Iout = 0mA
4. Timing patterns

   - DDR400(200Mhz, CL=3) : tCK = 5ns, CL = 3, BL = 4, tRRD = 2*tCK, tRCD = 3*tCK, Read with autoprecharge
   Read : A0 N A1 R0 A2 R1 A3 R2 N R3 A0 N A1 R0 - repeat the same timing with random address changing 50% of data changing at every burst

   Legend : A=Activate, R=Read, W=Write, P=Precharge, N=NOP

AC OPERATING CONDITIONS (TA=0 to 70 °C, Voltage referenced to VSS = 0V)

Parameter	Symbol	Min	Max	Unit
Input High (Logic 1) Voltage, DQ, DQS and DM signals	VIH(AC)	VREF + 0.31	-	V
Input Low (Logic 0) Voltage, DQ, DQS and DM signals	VIL(AC)	-	VREF - 0.31	V
Input Differential Voltage, CK and /CK inputs[1]	VID(AC)	0.7	VDDQ + 0.6	V
Input Crossing Point Voltage, CK and /CK inputs[2]	VIX(AC)	0.5*VDDQ-0.2	0.5*VDDQ+0.2	V

Note:
1. V*ID* is the magnitude of the difference between the input level on CK and the input on /CK.
2. The value of VIX is expected to equal 0.5*VDDQ of the transmitting device and must track variations in the DC level of the same.

*For more information about AC Overshoot/Undershoot Specifications, refer to "Device Operation" section in hynix website.

AC OPERATING TEST CONDITIONS (TA=0 to 70°C, Voltage referenced to VSS = 0V)

Parameter	Value	Unit
Reference Voltage	VDDQ x 0.5	V
Termination Voltage	VDDQ x 0.5	V
AC Input High Level Voltage (VIH, min)	VREF + 0.31	V
AC Input Low Level Voltage (VIL, max)	VREF - 0.31	V
Input Timing Measurement Reference Level Voltage	VREF	V
Output Timing Measurement Reference Level Voltage	VTT	V
Input Signal maximum peak swing	1.5	V
Input minimum Signal Slew Rate	1	V/ns
Termination Resistor (RT)	50	Ω
Series Resistor (RS)	25	W
Output Load Capacitance for Access Time Measurement (CL)	30	pF

- Continue

Parameter		Symbol	FA		FB		UNIT
			Min	Max	Min	Max	
Row Cycle Time		tRC	52	-	52	-	ns
Auto Refresh Row Cycle Time		tRFC	60	-	60	-	ns
Row Active Time		tRAS	40	70K	40	70K	ns
Active to Read with Auto Precharge Delay		tRAP	tRCD or tRAS(min)	-	tRCD or tRAS(min)	-	ns
Row Address to Column Address Delay		tRCD	16	-	12	-	ns
Row Active to Row Active Delay		tRRD	12	-	12	-	ns
Column Address to Column Address Delay		tCCD	1	-	1	-	tCK
Row Precharge Time		tRP	16	-	12	-	ns
Write Recovery Time		tWR	15	-	15	-	ns
Internal Write to Read Command Delay		tWTR	2	-	2	-	tCK
Auto Precharge Write Recovery + Precharge Time[22]		tDAL	(tWR/tCK) + (tRP/tCK)	-	(tWR/tCK) + (tRP/tCK)	-	tCK
System Clock Cycle Time[24]	CL = 4	tCK	4	10	4	10	ns
	CL = 3		-	-	-	-	
	CL = 2		-	-	-	-	
Clock High Level Width		tCH	0.45	0.55	0.45	0.55	tCK
Clock Low Level Width		tCL	0.45	0.55	0.45	0.55	tCK
Data-Out edge to Clock edge Skew		tAC	-0.6	0.6	-0.6	0.6	ns
DQS-Out edge to Clock edge Skew		tDQSCK	-0.6	0.6	-0.6	0.6	ns
DQS-Out edge to Data-Out edge Skew[21]		tDQSQ	-	0.4	-	0.4	ns
Data-Out hold time from DQS[20]		tQH	tHP -tQHS	-	tHP -tQHS	-	ns
Clock Half Period[19,20]		tHP	min (tCL,tCH)	-	min (tCL,tCH)	-	ns
Data Hold Skew Factor[20]		tQHS	-	0.5	-	0.5	ns
Valid Data Output Window		tDV	tQH - tDQSQ		tQH - tDQSQ		ns

- Continue

Parameter		Symbol	E3		E4		UNIT
			Min	Max	Min	Max	
Row Cycle Time		tRC	55	-	60	-	ns
Auto Refresh Row Cycle Time		tRFC	70	-	70	-	ns
Row Active Time		tRAS	40	70K	40	70K	ns
Active to Read with Auto Precharge Delay		tRAP	tRCD or tRAS(min)	-	tRCD or tRAS(min)	-	ns
Row Address to Column Address Delay		tRCD	15	-	18	-	ns
Row Active to Row Active Delay		tRRD	10	-	10	-	ns
Column Address to Column Address Delay		tCCD	1	-	1	-	tCK
Row Precharge Time		tRP	15	-	18	-	ns
Write Recovery Time		tWR	15	-	15	-	ns
Internal Write to Read Command Delay		tWTR	2	-	2	-	tCK
Auto Precharge Write Recovery + Precharge Time[22]		tDAL	(tWR/tCK) + (tRP/tCK)	-	(tWR/tCK) + (tRP/tCK)	-	tCK
System Clock Cycle Time[24]	CL = 4	tCK	-	-	-	-	ns
	CL = 3		5	10	5	10	
	CL = 2		7.5	12	7.5	12	
Clock High Level Width		tCH	0.45	0.55	0.45	0.55	tCK
Clock Low Level Width		tCL	0.45	0.55	0.45	0.55	tCK
Data-Out edge to Clock edge Skew		tAC	-0.7	0.7	-0.7	0.7	ns
DQS-Out edge to Clock edge Skew		tDQSCK	-0.55	0.55	-0.65	0.65	ns
DQS-Out edge to Data-Out edge Skew[21]		tDQSQ	-	0.4	-	0.4	ns
Data-Out hold time from DQS[20]		tQH	tHP -tQHS	-	tHP -tQHS	-	ns
Clock Half Period[19,20]		tHP	min (tCL,tCH)	-	min (tCL,tCH)	-	ns
Data Hold Skew Factor[20]		tQHS	-	0.5	-	0.5	ns
Valid Data Output Window		tDV	tQH - tDQSQ		tQH - tDQSQ		ns

- Continue

Parameter		Symbol	J3		K2		K3		UNIT
			Min	Max	Min	Max	Min	Max	
Row Cycle Time		tRC	60	-	65	-	65	-	ns
Auto Refresh Row Cycle Time		tRFC	72	-	75	-	75	-	ns
Row Active Time		tRAS	42	70K	45	120K	50	120K	ns
Active to Read with Auto Precharge Delay		tRAP	tRCD or tRAS(min)	-	tRCD or tRAS(min)	-	tRCD or tRAS(min)	-	ns
Row Address to Column Address Delay		tRCD	18	-	20	-	20	-	ns
Row Active to Row Active Delay		tRRD	12	-	15	-	15	-	ns
Column Address to Column Address Delay		tCCD	1	-	1	-	1	-	t*CK*
Row Precharge Time		tRP	18	-	20	-	20	-	ns
Write Recovery Time		tWR	15	-	15	-	15	-	ns
Internal Write to Read Command Delay		tWTR	1	-	1	-	1	-	t*CK*
Auto Precharge Write Recovery + Precharge Time[22]		tDAL	(tWR/tCK) + (tRP/tCK)	-	(tWR/tCK) + (tRP/tCK)	-	(tWR/tCK) + (tRP/tCK)	-	t*CK*
System Clock Cycle Time[24]	CL = 3	tCK	6	12	-	-	-	-	ns
	CL = 2.5		6	12	7.5	12	7.5	12	
	CL = 2		7.5	12	7.5	12	10	12	
Clock High Level Width		tCH	0.45	0.55	0.45	0.55	0.45	0.55	tCK
Clock Low Level Width		tCL	0.45	0.55	0.45	0.55	0.45	0.55	tCK
Data-Out edge to Clock edge Skew		tAC	-0.7	0.7	-0.75	0.75	-0.75	0.75	ns
DQS-Out edge to Clock edge Skew		tDQSCK	-0.6	0.6	-0.75	0.75	-0.75	0.75	ns
DQS-Out edge to Data-Out edge Skew[21]		tDQSQ	-	0.45	-	0.5	-	0.5	ns
Data-Out hold time from DQS[20]		tQH	t*HP* -t*QHS*	-	t*HP* -t*QHS*	-	t*HP* -t*QHS*	-	ns
Clock Half Period[19,20]		tHP	min (tCL,tCH)	-	min (tCL,tCH)	-	min (tCL,tCH)	-	ns
Data Hold Skew Factor[20]		tQHS	-	0.55	-	0.75	-	0.75	ns
Valid Data Output Window		tDV	tQH - tDQSQ		tQH - tDQSQ		tQH - tDQSQ		ns

- Continue

Parameter	Symbol	FA		FB		UNIT
		Min	Max	Min	Max	
Data-out high-impedance window from CK,/CK[10]	tHZ	-	tAC (Max)	-	tAC (Max)	ns
Data-out low-impedance window from CK, /CK[10]	tLZ	-0.7	0.7	-0.7	0.7	ns
Input Setup Time (fast slew rate)[14,16-18]	tIS	0.75	-	0.75	-	ns
Input Hold Time (fast slew rate)[14,16-18]	tIH	0.75	-	0.75	-	ns
Input Setup Time (slow slew rate)[15-18]	tIS	0.7	-	0.7	-	ns
Input Hold Time (slow slew rate)[15-18]	tIH	0.7	-	0.7	-	ns
Input Pulse Width[17]	tIPW	2.2	-	2.2	-	ns
Write DQS High Level Width	tDQSH	0.4	0.6	0.4	0.6	tCK
Write DQS Low Level Width	tDQSL	0.4	0.6	0.4	0.6	tCK
Clock to First Rising edge of DQS-In	tDQSS	0.85	1.15	0.85	1.15	tCK
DQS falling edge to CK setup time	tDSS	0.3	-	0.3	-	tCK
DQS falling edge hold time from CK	tDSH	0.3	-	0.3	-	tCK
DQ & DM input setup time[25]	tDS	0.4	-	0.4	-	ns
DQ & DM input hold time[25]	tDH	0.4	-	0.4	-	ns
DQ & DM Input Pulse Width[17]	tDIPW	1.75	-	1.75	-	ns
Read DQS Preamble Time	tRPRE	0.9	1.1	0.9	1.1	tCK
Read DQS Postamble Time	tRPST	0.4	0.6	0.4	0.6	tCK
Write DQS Preamble Setup Time[12]	tWPRES	0	-	0	-	ns
Write DQS Preamble Hold Time	tWPREH	0.35	-	0.35	-	tCK
Write DQS Postamble Time[11]	tWPST	0.4	0.6	0.4	0.6	tCK
Mode Register Set Delay	tMRD	2	-	2	-	tCK
Exit Self Refresh to non-Read command[23]	tXSNR	75	-	75	-	ns
Exit Self Refresh to Read command	tXSRD	200	-	200	-	tCK
Average Periodic Refresh Interval[13,25]	tREFI	-	15.6	-	15.6	us

- Continue

Parameter	Symbol	E3		E4		UNIT
		Min	Max	Min	Max	
Data-out high-impedance window from CK,/CK[10]	tHZ	-	tAC (Max)	-	tAC (Max)	ns
Data-out low-impedance window from CK, /CK[10]	tLZ	-0.7	0.7	-0.7	0.7	ns
Input Setup Time (fast slew rate)[14,16-18]	tIS	0.6	-	0.6	-	ns
Input Hold Time (fast slew rate)[14,16-18]	tIH	0.6	-	0.6	-	ns
Input Setup Time (slow slew rate)[15-18]	tIS	0.7	-	0.7	-	ns
Input Hold Time (slow slew rate)[15-18]	tIH	0.7	-	0.7	-	ns
Input Pulse Width[17]	tIPW	2.2	-	2.2	-	ns
Write DQS High Level Width	tDQSH	0.35	-	0.35	-	tCK
Write DQS Low Level Width	tDQSL	0.35	-	0.35	-	tCK
Clock to First Rising edge of DQS-In	tDQSS	0.72	1.25	0.72	1.25	tCK
DQS falling edge to CK setup time	tDSS	0.2	-	0.2	-	tCK
DQS falling edge hold time from CK	tDSH	0.2	-	0.2	-	tCK
DQ & DM input setup time[25]	tDS	0.4	-	0.4	-	ns
DQ & DM input hold time[25]	tDH	0.4	-	0.4	-	ns
DQ & DM Input Pulse Width[17]	tDIPW	1.75	-	1.75	-	ns
Read DQS Preamble Time	tRPRE	0.9	1.1	0.9	1.1	tCK
Read DQS Postamble Time	tRPST	0.4	0.6	0.4	0.6	tCK
Write DQS Preamble Setup Time[12]	tWPRES	0	-	0	-	ns
Write DQS Preamble Hold Time	tWPREH	0.25	-	0.25	-	tCK
Write DQS Postamble Time[11]	tWPST	0.4	0.6	0.4	0.6	tCK
Mode Register Set Delay	tMRD	2	-	2	-	tCK
Exit Self Refresh to non-Read command[23]	tXSNR	75	-	75	-	ns
Exit Self Refresh to Read command	tXSRD	200	-	200	-	tCK
Average Periodic Refresh Interval[13,25]	tREFI	-	15.6	-	15.6	us

- Continue

Parameter	Symbol	J3		K2		K3		UNIT
		Min	Max	Min	Max	Min	Max	
Data-out high-impedance window from CK,/ CK[10]	tHZ	-	t*AC* (Max)	-	t*AC* (Max)	-	t*AC* (Max)	ns
Data-out low-impedance window from CK, / CK[10]	tLZ	-0.7	0.7	-0.75	0.75	-0.75	0.75	ns
Input Setup Time (fast slew rate)[14,16-18]	tIS	0.75	-	0.9	-	0.9	-	ns
Input Hold Time (fast slew rate)[14,16-18]	tIH	0.75	-	0.9	-	0.9	-	ns
Input Setup Time (slow slew rate)[15-18]	tIS	0.8	-	1.0	-	1.0	-	ns
Input Hold Time (slow slew rate)[15-18]	tIH	0.8	-	1.0	-	1.0	-	ns
Input Pulse Width[17]	tIPW	2.2	-	2.2	-	2.2	-	ns
Write DQS High Level Width	tDQSH	0.35	-	0.35	-	0.35	-	tCK
Write DQS Low Level Width	tDQSL	0.35	-	0.35	-	0.35	-	tCK
Clock to First Rising edge of DQS-In	tDQSS	0.75	1.25	0.75	1.25	0.75	1.25	tCK
DQS falling edge to CK setup time	tDSS	0.2	-	0.2	-	0.2	-	tCK
DQS falling edge hold time from CK	tDSH	0.2	-	0.2	-	0.2	-	tCK
DQ & DM input setup time[25]	tDS	0.45	-	0.5	-	0.5	-	ns
DQ & DM input hold time[25]	tDH	0.45	-	0.5	-	0.5	-	ns
DQ & DM Input Pulse Width[17]	tDIPW	1.75	-	1.75	-	1.75	-	ns
Read DQS Preamble Time	tRPRE	0.9	1.1	0.9	1.1	0.9	1.1	tCK
Read DQS Postamble Time	tRPST	0.4	0.6	0.4	0.6	0.4	0.6	tCK
Write DQS Preamble Setup Time[12]	tWPRES	0	-	0	-	0	-	ns
Write DQS Preamble Hold Time	tWPREH	0.25	-	0.25	-	0.25	-	tCK
Write DQS Postamble Time[11]	tWPST	0.4	0.6	0.4	0.6	0.4	0.6	tCK
Mode Register Set Delay	tMRD	2	-	2	-	2	-	tCK
Exit Self Refresh to non-Read command[23]	tXSNR	75	-	75	-	75	-	ns
Exit Self Refresh to Read command	tXSRD	200	-	200	-	200	-	tCK
Average Periodic Refresh Interval[13,25]	tREFI	-	15.6	-	15.6	-	15.6	us

Note:

1. All voltages referenced to Vss.
2. Tests for ac timing, IDD, and electrical, ac and dc characteristics, may be conducted at nominal reference/supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range specified.
3. Below figure represents the timing reference load used in defining the relevant timing parameters of the part. It is not intended to be either a precise representation of the typical system environment nor a depiction of the actual load presented by a production tester. System designers will use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers will correlate to their production test conditions (generally a coaxial transmission line terminated at the tester electronics).

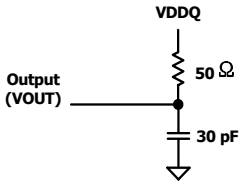


Figure: Timing Reference Load

4. AC timing and IDD tests may use a VIL to VIHswing of up to 1.5 V in the test environment, but input timing is still referenced to VREF (or to the crossing point for CK, /CK), and parameter specifications are guaranteed for the specified ac input levels under normal use conditions. The minimum slew rate for the input signals is 1 V/ns in the range between VIL(ac) and VIH(ac).
5. The ac and dc input level specifications are as defined in the SSTL_2 Standard (i.e., the receiver will effectively switch as a result of the signal crossing the ac input level and will remain in that state as long as the signal does not ring back above (below) the dc input LOW (HIGH) level.
6. Inputs are not recognized as valid until VREF stabilizes. Exception: during the period before VREF stabilizes, CKE $\leq$ 0.2VDDQ is recognized as LOW.
7. The CK, /CK input reference level (for timing referenced to CK, /CK) is the point at which CK and /CK cross; the input reference level for signals other than CK, /CK is VREF.
8. The output timing reference voltage level is VTT.
9. Operation or timing that is not specified is illegal and after such an event, in order to guarantee proper operation, the DRAM must be powered down and then restarted through the specified initialization sequence before normal operation can continue.
10. tHZ and tLZ transitions occur in the same access time windows as valid data transitions. These parameters are not referenced to a specific voltage level but specify when the device output is no longer driving (HZ), or begins driving (LZ).
11. The maximum limit for this parameter is not a device limit. The device will operate with a greater value for this parameter, but system performance (bus turnaround) will degrade accordingly.
12. The specific requirement is that DQS be valid (HIGH, LOW, or at some point on a valid transition) on or before this CK edge. A valid transition is defined as monotonic and meeting the input slew rate specifications of the device. When no writes were previously in progress on the bus, DQS will be transitioning from High-Z to logic LOW. If a previous write was in progress, DQS could be HIGH, LOW, or transitioning from HIGH to LOW at this time, depending on tDQSS.
13. A maximum of eight AUTO REFRESH commands can be posted to any given DDR SDRAM device.
14. For command/address input slew rate $\geq$ 1.0 V/ns.
15. For command/address input slew rate $\geq$ 0.5 V/ns and $<$ 1.0 V/ns
16. For CK & /CK slew rate $\geq$ 1.0 V/ns (single-ended)
17. These parameters guarantee device timing, but they are not necessarily tested on each device.
    They may be guaranteed by device design or tester correlation.
18. Slew Rate is measured between VOH(ac) and VOL(ac).
19. Min (tCL, tCH) refers to the smaller of the actual clock low time and the actual clock high time as provided to the device (i.e. this value can be greater than the minimum specification limits for tCL and tCH).
    For example, tCL and tCH are = 50% of the period, less the half period jitter (tJIT(HP)) of the clock source, and less the half period jitter due to crosstalk (tJIT(crosstalk)) into the clock traces.

20.tQH = tHP - tQHS, where:

tHP = minimum half clock period for any given cycle and is defined by clock high or clock low (tCH, tCL). tQHS accounts for 1) The pulse duration distortion of on-chip clock circuits; and 2) The worst case push--out of DQS on one transition followed by the worst case pull--in of DQ on the next transition, both of which are, separately, due to data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers.

21. tDQSQ:

Consists of data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers for any given cycle.

22. tDAL = (tWR/tCK) + (tRP/tCK)

For each of the terms above, if not already an integer, round to the next highest integer.

Example: For DDR266B at CL=2.5 and tCK=7.5 ns

tDAL = ((15 ns / 7.5 ns) + (20 ns / 7.5 ns)) clocks

= ((2) + (3)) clocks

= 5 clocks

23. In all circumstances, tXSNR can be satisfied using

tXSNR = tRFCmin + 1*tCK

24. The only time that the clock frequency is allowed to change is during self-refresh mode.

25. If refresh timing or tDS/tDH is violated, data corruption may occur and the data must be re-written with valid data before a valid READ can be executed.

SYSTEM CHARACTERISTICS CONDITIONS for DDR SDRAMS

The following tables are described specification parameters that required in systems using DDR devices to ensure proper performannce. These characteristics are for system simulation purposes and are guaranteed by design.

Input Slew Rate for DQ/DM/DQS (Table a.)

AC CHARACTERISTICS		DDR400		DDR333		DDR266		UNIT	Note
PARAMETER	Symbol	min	max	min	max	min	max		
DQ/DM/DQS input slew rate measured between VIH(DC), VIL(DC) and VIL(DC), VIH(DC)	DCSLEW	0.5	4.0	0.5	4.0	0.5	4.0	V/ns	1,12

Address & Control Input Setup & Hold Time Derating (Table b.)

Input Slew Rate	Delta tIS	Delta tIH	UNIT	Note
0.5 V/ns	0	0	ps	9
0.4 V/ns	+50	0	ps	9
0.3 V/ns	+100	0	ps	9

DQ & DM Input Setup & Hold Time Derating (Table c.)

Input Slew Rate	Delta tDS	Delta tDH	UNIT	Note
0.5 V/ns	0	0	ps	11
0.4 V/ns	+75	0	ps	11
0.3 V/ns	+150	0	ps	11

DQ & DM Input Setup & Hold Time Derating for Rise/Fall Delta Slew Rate (Table d.)

Input Slew Rate	Delta tDS	Delta tDH	UNIT	Note
± 0.0 ns/V	0	0	ps	10
± 0.25 ns/V	+50	+50	ps	10
± 0.5 ns/V	+100	+100	ps	10

Output Slew Rate Characteristics (for x16 Device) (Table e.)

Slew Rate Characteristic	Typical Range (V/ns)	Minimum (V/ns)	Maximum (V/ns)	Note
Pullup Slew Rate	1.2 - 2.5	0.7	5.0	1,3,4,6,7,8
Pulldown Slew Rate	1.2 - 2.5	0.7	5.0	2,3,4,6,7,8

Output Slew Rate Matching Ratio Characteristics (Table f.)

Slew Rate Characteristic	DDR266A		DDR266B		Note
Parameter	min	max	min	max	
Output Slew Rate Matching Ratio (Pullup to Pulldown)	-	-	-	-	5,12

Note:

1. Pullup slew rate is characterized under the test conditions as shown in below Figure.

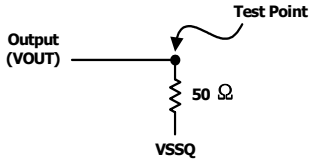


Figure: Pullup Slew rate

2. Pulldown slew rate is measured under the test conditions shown in below Figure.

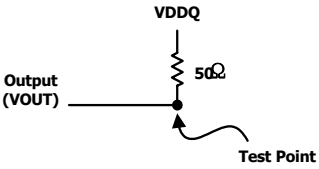


Figure: Pulldown Slew rate

3. Pullup slew rate is measured between (VDDQ/2 - 320 mV ± 250mV)
   Pulldown slew rate is measured between (VDDQ/2 + 320mV ± 250mV)
   Pullup and Pulldown slew rate conditions are to be met for any pattern of data, including all outputs switching and only one output switching.

Example: For typical slew, DQ0 is switching
   For minimum slew rate, all DQ bits are switching worst case pattern
   For maximum slew rate, only one DQ is switching from either high to low, or low to high.
   The remaining DQ bits remain the same as for previous state.

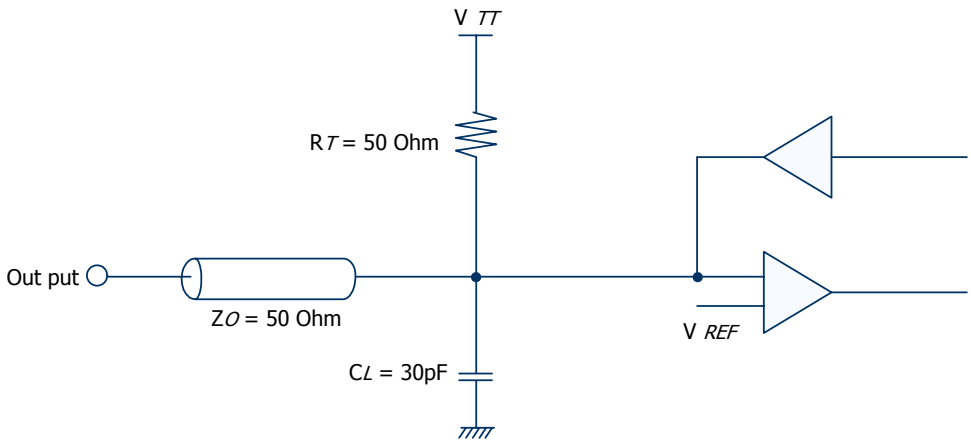
4. Evaluation conditions
   Typical: 25 ^{o}C (Ambient), VDDQ = nominal, typical process
   Minimum: 70 ^{o}C (Ambient), VDDQ = minimum, slow-slow process
   Maximum: 0 ^{o}C (Ambient), VDDQ = Maximum, fast-fast process
5. The ratio of pullup slew rate to pulldown slew rate is specified for the same temperature and voltage, over the entire temperature and voltage range. For a given output, it represents the maximum difference between pullup and pulldown drivers due to process variation.
6. Verified under typical conditions for qualification purposes.
7. TSOP-II package devices only.
8. Only intended for operation up to 256 Mbps per pin.
9. A derating factor will be used to increase tIS and tIH in the case where the input slew rate is below 0.5 V/ns as shown in Table b. The Input slew rate is based on the lesser of the slew rates determined by either VIH(AC) to VIL(AC) or VIH(DC) to VIL(DC), similarly for rising transitions.
10. A derating factor will be used to increase tDS and tDH in the case where DQ, DM, and DQS slew rates differ, as shown in Tables c & d. Input slew rate is based on the larger of AC-AC delta rise, fall rate and DC-DC delta rise, fall rate. Input slew rate is based on the lesser of the slew rates determined by either VIH(AC) to VIL(AC) or VIH(DC) to VIL(DC), similarly for rising transitions. The delta rise/fall rate is calculated as:
    {1/(Slew Rate1)} - {1/(slew Rate2)}
    For example:
    If Slew Rate 1 is 0.5 V/ns and Slew Rate 2 is 0.4 V/ns, then the delta rise, fall rate is -0.5 ns/V. Using the table given, this would result in the need for an increase in tDS and tDH of 100ps.
11. Table c is used to increase tDS and tDH in the case where the I/O slew rate is below 0.5 V/ns. The I/O slew rate is based on the lesser of the AC-AC slew rate and the DC-DC slew rate. The input slew rate is based on the lesser of the slew rates determined by either VIH(ac) to VIL(AC) or VIH(DC) to VIL(DC), and similarly for rising transitions.
12. DQS, DM, and DQ input slew rate is specified to prevent double clocking of data and preserve setup and hold times. Signal transitions through the DC region must be monotonic.

CAPACITANCE (TA=25°C, f=100MHz)

Parameter	Pin	Symbol	Min	Max	Unit
Input Clock Capacitance	CK, /CK	CI1	2.0	3.0	pF
Delta Input Clock Capacitance	CK, /CK	Delta CI1	-	0.25	pF
Input Capacitance	All other input-only pins	CI1	2.0	3.0	pF
Delta Input Capacitance	All other input-only pins	Delta CI2	-	0.5	pF
Input / Output Capacitance	DQ, DQS, DM	CIO	4.0	5.0	pF
Delta Input / Output Capacitance	DQ, DQS, DM	Delta CIO	-	0.5	pF

Note:
1. VDD = min. to max., VDDQ = 2.3V to 2.7V, VODC = VDDQ/2, VOpeak-to-peak = 0.2V
2. Pins not under test are tied to GND.
3. These values are guaranteed by design and are tested on a sample basis only.

OUTPUT LOAD CIRCUIT



PACKAGE INFORMATION

400mil 66pin Thin Small Outline Package

Unit : mm(Inch)