STiDP880

iDP to LVDS converter

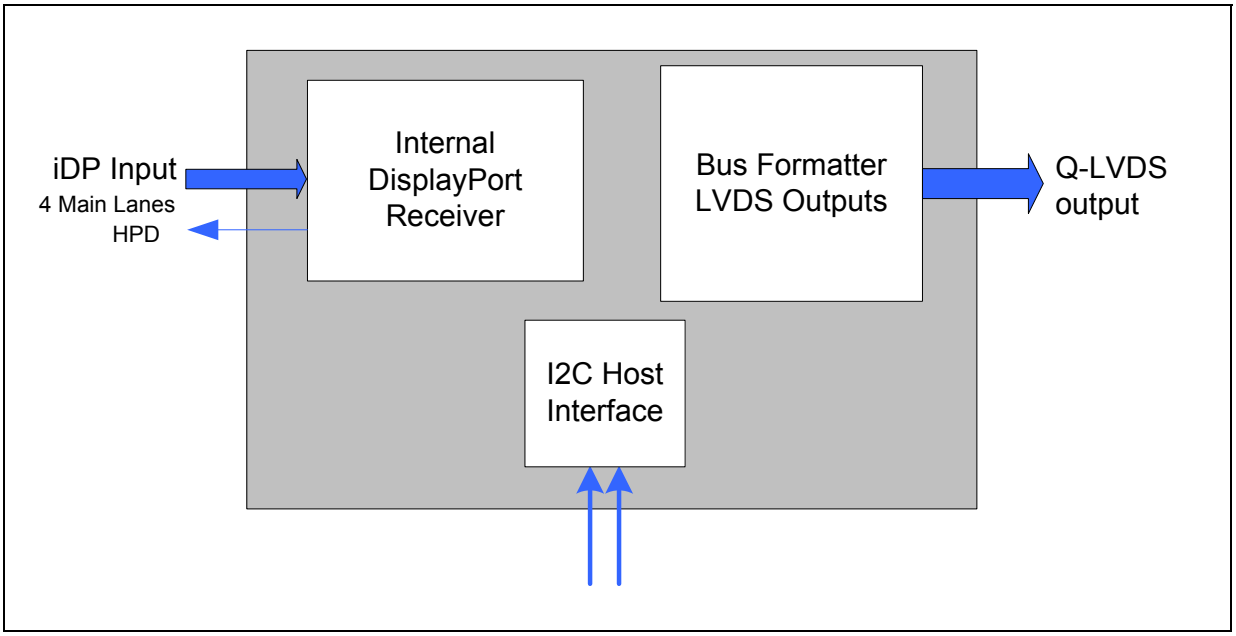
Data brief

Features

- Internal DisplayPort (iDP) receiver
  - Compliant with proposed iDP specification
  - 3.24 Gbps per lane
  - 1, 2, or 4 lanes
  - HPD pulse assertion as per proposed iDP standard
- Supports video timings up to 1920 x 1080 (FHD) 120 Hz/10-bit color
- Interface compatibility with wide range of panels
  - Quad LVDS interface up to 100 MHz per channel (400 MHz pixel rate)
  - High speed dual-link LVDS up to 150 MHz per channel (300 MHz pixel rate)
  - Supports JEIDA, non-JEIDA, VESA pixel data mappings
- Supports Asynchronous Scrambler Seed Reset (ASSR) for premium contents reception
- Configurable through I2C host interface
- Supports Spread Spectrum for EMI/RFI reduction
- Robust interoperability – supports FFC and UTP type cables
- Low power operation; 20 mW standby
- Package
  - 164 LFBGA (12 x 12 mm/0.8 mm pitch)
  - HF and RoHS compliant
- Power supply voltages
  - 3.3 V I/O; 1.2 V core
- ESD
  - 2 KV HBM, 200 V MM, 600V CDM

Applications

- High refresh rate TV/monitor panel interface



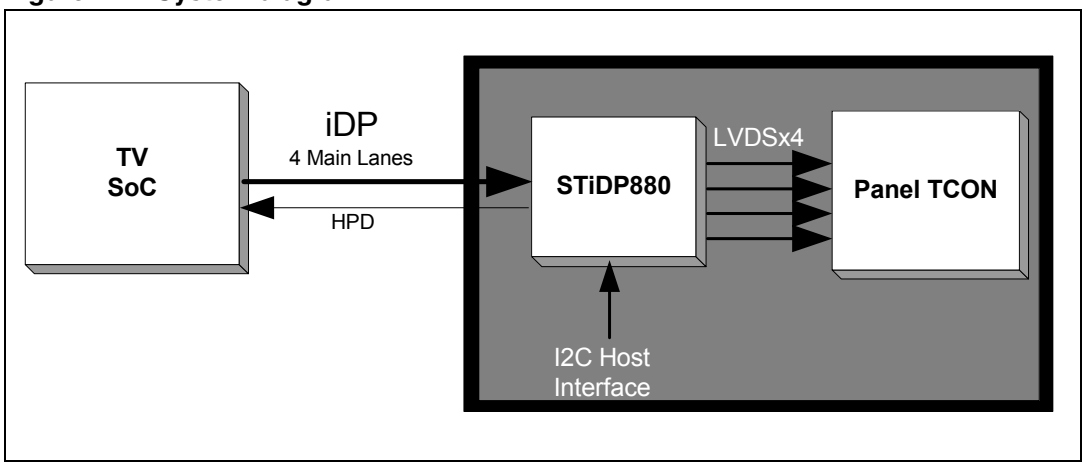
1 Description

The STiDP880 is an internal DisplayPort to high-speed Dual LVDS/Quad LVDS converter IC targeted for the interconnection between a TV controller SOC and panel TCON. STiDP880 is a proposed VESA iDP compliant device, implementing a single link internal DisplayPort input comprising four Main Link lanes and HPD, which operates without a sideband channel. This device supports the proposed standard iDP link rate of 3.24 Gbps per lane with a total link bandwidth of 12.96 Gbps, allowing interface connectivity for a wide range of panels up to FHD 120 Hz and 10 bits per color. The advanced equalizer built in this device offers robust performance over FFC and UTP type cables.

The STiDP880 supports RGB video color formats with color depth of 10 and 8 bits. This device offers LVDS output interface configurable to map a wide range of pixel data mapping, such as JEIDA, non-JEIDA, and VESA types. The Quad LVDS interface supports video signals up to 400 MHz pixel rate with flexible channel and lane swapping options. In Dual LVDS configuration, STiDP880 can support up to 300 MHz pixel rate.

The STiDP880 is designed to operate in standalone mode (without any programming from an external microcontroller) with default configuration of four lanes DP input and QLVDS output with non-JEIDA mapping. However, the device is configurable from an external microcontroller through I2C host interface for custom configuration.

Figure 1. System diagram



2 Benefits

- Industry's first iDP receiver based on ST's market proven DisplayPort technology
- Offers robust interoperability with ST and third party iDP transmitters
- Highly integrated single chip solution for FHD 120 Hz TV panel; two devices supports FHD240Hz panel over eight Main Link lanes
- Flexible interface to ease system design – DP 1, 2, 4 lane configuration, high speed LVDS 2, 4 channels
- Standalone operation with default LVDS mappings matches to majority non-JEIDA FHD 120 Hz TV panels
- I2C host interface for custom configurations – LVDS channel mappings, equalization settings, color depth selection, etc.
- Low EMI – supports down-spread DP input and spectrum-spreading of LVDS channels
- Low power – active power sub 800 mW max and 20 mW standby

3 Ordering information

Table 1. Order codes

Part number	Description
STiDP880	164 LFBGA (12 x 12 mm)

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*.
ECOPACK® is an ST trademark.

4 Revision history

Table 2. Document revision history

Date	Revision	Changes
10-Dec-2009	1	Initial release.

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