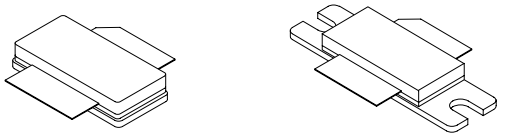
TriQuint SEMICONDUCTOR

AGR21090E
90 W, 2.110 GHz—2.170 GHz, N-Channel E-Mode, Lateral MOSFET

Introduction

The AGR21090E is a high-voltage, gold-metalized, laterally diffused, metal oxide semiconductor (LDMOS) RF power transistor suitable for wideband code-division multiple access (W-CDMA), and single and multicarrier class AB wireless base station power amplifier applications.



AGR21090EU (unflanged) **AGR21090EF (flanged)**

Figure 1. Available Packages

Features

Typical performance for 2 carrier 3GPP W-CDMA systems. F1 = 2135 MHz and F2 = 2145 MHz with 3.84 MHz channel BW, adjacent channel BW = 3.84 MHz at F1 – 5 MHz and F2 + 5 MHz. Third-order distortion is measured over 3.84 MHz BW at F1 – 10 MHz and F2 + 10 MHz. Typical P/A ratio of 8.5 dB at 0.01% (probability) CCDF:
- Output power: 19 W.
- Power gain: 14.5 dB.
- Efficiency: 26%.
- IM3: –33 dBc.
- ACPR: –36 dBc.
- Return loss: –12 dB.

High-reliability, gold-metalization process.

Low hot carrier injection (HCI) induced bias drift over 20 years.

Internally matched.

High gain, efficiency, and linearity.

Integrated ESD protection.

Device can withstand a 10:1 voltage standing wave ratio (VSWR) at 28 Vdc, 2140 MHz, 90 W continuous wave (CW) output power.

Large signal impedance parameters available.

Table 1. Thermal Characteristics

Parameter	Sym	Value	Unit
Thermal Resistance, Junction to Case:			
AGR21090EU	$R_{\theta JC}$	0.7	°C/W
AGR21090EF	$R_{\theta JC}$	0.7	°C/W

Table 2. Absolute Maximum Ratings*

Parameter	Sym	Value	Unit
Drain-source Voltage	V_{DSS}	65	Vdc
Gate-source Voltage	V_{GS}	–0.5, 15	Vdc
Total Dissipation at T_C = 25 °C:			
AGR21090EU	P_D	250	W
AGR21090EF	P_D	250	W
Derate Above 25 ˚C:			
AGR21090EU	—	1.4	W/°C
AGR21090EF	—	1.4	W/°C
CW RF Input Power (V_{DS} = 31 V)	—	30	W
Operating Junction Temperature	T_J	200	°C
Storage Temperature Range	T_{STG}	–65, 150	°C

* Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

Table 3. ESD Rating*

AGR21090E	Minimum (V)	Class
HBM	500	1B
MM	50	A
CDM	1500	4

* Although electrostatic discharge (ESD) protection circuitry has been designed into this device, proper precautions must be taken to avoid exposure to ESD and electrical overstress (EOS) during all handling, assembly, and test operations. PEAK Devices employs a human-body model (HBM), a machine model (MM), and a charged-device model (CDM) qualification requirement in order to determine ESD-susceptibility limits and protection design evaluation. ESD voltage thresholds are dependent on the circuit parameters used in each of the models, as defined by JEDEC's JESD22-A114B (HBM), JESD22-A115A (MM), and JESD22-C101A (CDM) standards.

Caution: MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

Electrical Characteristics

Recommended operating conditions apply unless otherwise specified: T_C = 30 °C.

Table 4. dc Characteristics

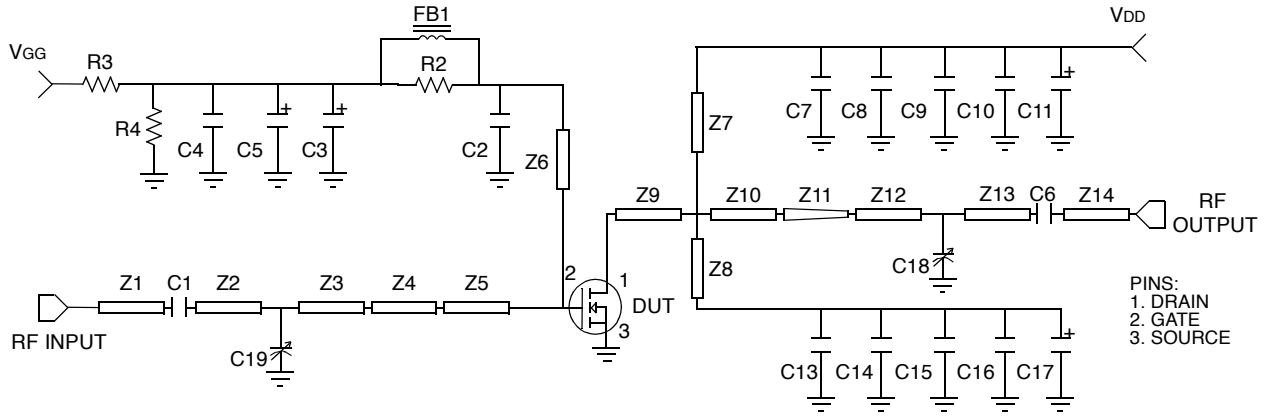
Parameter	Symbol	Min	Typ	Max	Unit
Off Characteristics					
Drain-source Breakdown Voltage (V_{GS} = 0, I_D = 300 μA)	$V_{(BR)DSS}$	65	—	—	Vdc
Gate-source Leakage Current (V_{GS} = 5 V, V_{DS} = 0 V)	I_{GSS}	—	—	3	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 28 V, V_{GS} = 0 V)	I_{DSS}	—	—	150	μAdc
On Characteristics					
Forward Transconductance (V_{DS} = 10 V, I_D = 1 A)	G_{FS}	—	6.4	—	S
Gate Threshold Voltage (V_{DS} = 10 V, I_D = 300 μA)	$V_{GS(TH)}$	2.8	3.4	4.8	Vdc
Gate Quiescent Voltage (V_{DS} = 28 V, I_D = 800 mA)	$V_{GS(Q)}$	3.0	3.7	4.6	Vdc
Drain-source On-voltage (V_{GS} = 10 V, I_D = 1 A)	$V_{DS(ON)}$	—	0.11	—	Vdc

Table 5. RF Characteristics

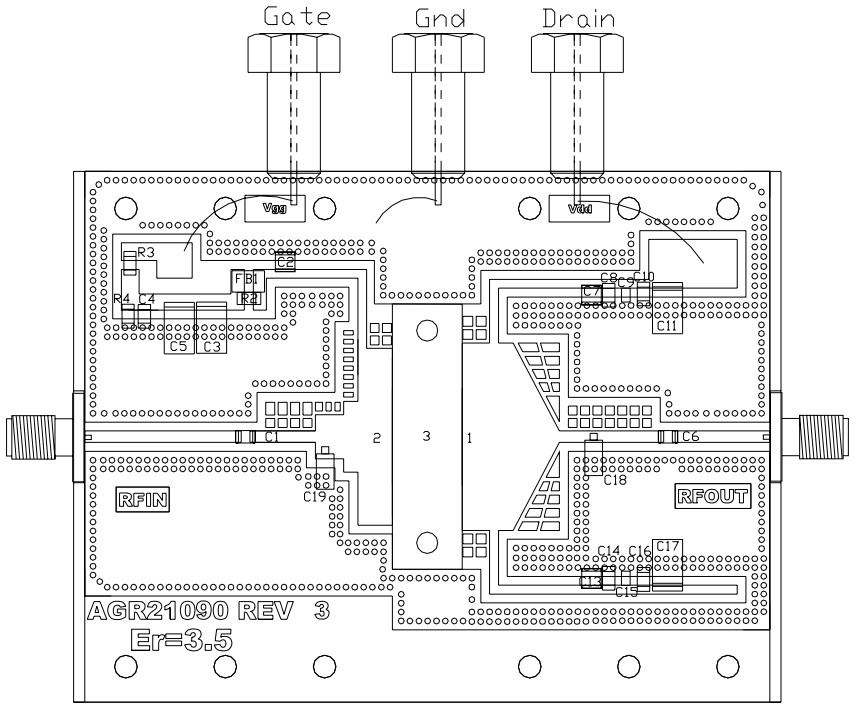
Parameter	Symbol	Min	Typ	Max	Unit
Dynamic Characteristics					
Reverse Transfer Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz) (This part is internally matched on both the input and output.)	C_{RSS}	—	2.1	—	pF
Functional Tests (in Supplied Test Fixture)					
Common-source Amplifier Power Gain*	G_{PS}	14.0	14.5	—	dB
Drain Efficiency*	η	24	26	—	%
Third-order Intermodulation Distortion* (IM3 distortion measured over 3.84 MHz BW @ f1 – 10 MHz and f2 + 10 MHz)	IM3	—	–33	–32	dBc
Adjacent Channel Power Ratio* (ACPR measured over BW of 3.84 MHz @ f1 – 5 MHz and f2 + 5 MHz)	ACPR	—	–36	–35	dBc
Input Return Loss*	IRL	—	–12	–9	dB
Power Output, 1 dB Compression Point (V_{DD} = 28 V, f_C = 2140.0 MHz)	P_{1dB}	85	93	—	W
Output Mismatch Stress (V_{DD} = 28 V, P_{OUT} = 90 W (CW), I_{DQ} = 800 mA, f_C = 2140.0 MHz VSWR = 10:1; [all phase angles])	ψ	No degradation in output power.			

* 3GPP W-CDMA, typical P/A ratio of 8.5 dB at 0.01% CCDF, f1 = 2135 MHz, and f2 = 2145 MHz.
V_{DD} = 28 Vdc, I_{DQ} = 800 mA, and P_{OUT} = 19 W average.
Nominal operating voltage 28 Vdc. Qualified for a maximum operating voltage of 32 Vdc ±0.5 V.

Test Circuit Illustrations for AGR21090E



A. Schematic



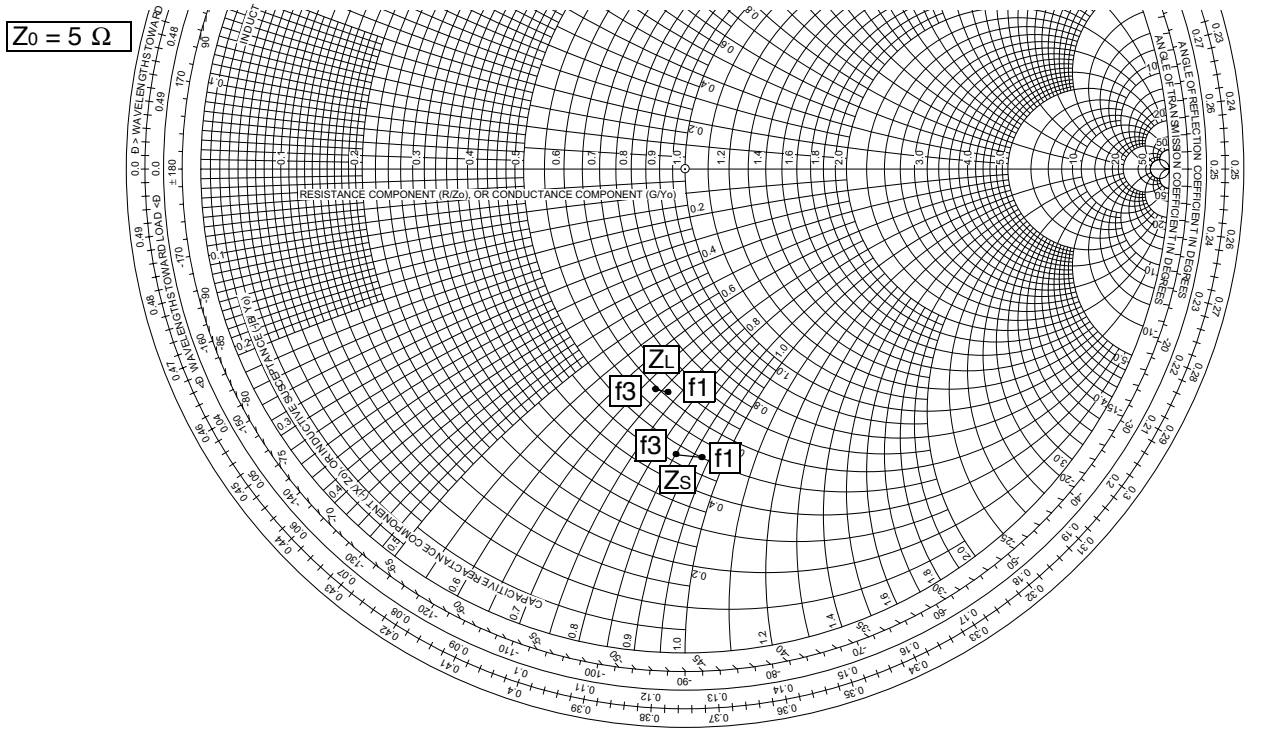
Parts List:

- Microstrip line: Z1 0.889 in. x 0.065 in.; Z2 0.370 in. x 0.065 in.; Z3 0.160 in. x 0.250 in.; Z4 0.080 in. x 0.400 in.; Z5 0.195 in. x 1.000 in.; Z6 0.050 in. x 0.860 in.; Z7 0.050 in. x 0.880 in.; Z8 0.050 in. x 0.880 in.; Z9 0.180 in. x 1.060 in.; Z10 0.110 in. x 1.060 in.; Z11 0.260 in. x 1.060 in. x 0.065 in. taper; Z12 0.195 x 0.065 in.; Z13 0.395 in. x 0.065 in.; Z14 0.555 in. x 0.065 in.
- *ATC*® chip capacitor: C1, C6: 8.2 pF 100B8R2JW500X; C2, C7, C13: 6.8 pF 100B6R8JW500X.
- *Sprague*® tantalum surface-mount chip capacitor: C3, C5, C11, C17: 22 μF, 35 V.
- *Kemet*® 1206 size chip capacitor: C10, C16: 0.1 μF C1206104K5RAC7800.
- *Murata*® 0805 size chip capacitor: C9, C15: 0.01 μF GRM40X7R103K100AL.
- *Johanson Giga-Trim*® variable capacitor: C18, C19: 0.4 pF to 2.5 pF 27281SL.
- 1206 size chip capacitor: C4, C8, C14: 22000 pF.
- 1206 size chip resistor: R2 4.7 Ω, R3 1.02 kΩ, R4 560 kΩ.
- *Fair-Rite*® ferrite bead: FB1 2743019447.
- *Taconic*® ORCER RF-35: board material, 1 oz. copper, 30 mil thickness, εr = 3.5.

B. Component Layout

Figure 2. AGR21090E Test Circuit

Typical Performance Characteristics



MHz (f)	ZS Ω (Complex Source Impedance)	ZL Ω (Complex Optimum Load Impedance)
2110 (f1)	2.52 – j4.60	3.10 – j3.11
2140 (f2)	2.46 – j4.42	3.01 – j3.05
2170 (f3)	2.37 – j4.25	2.94 – j2.99

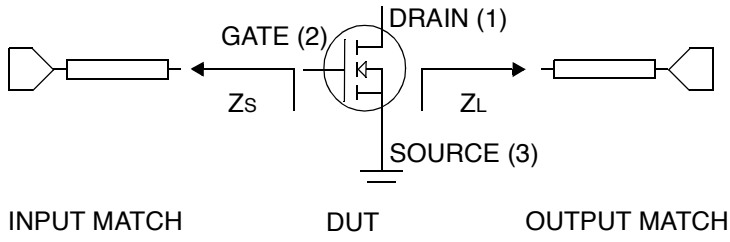
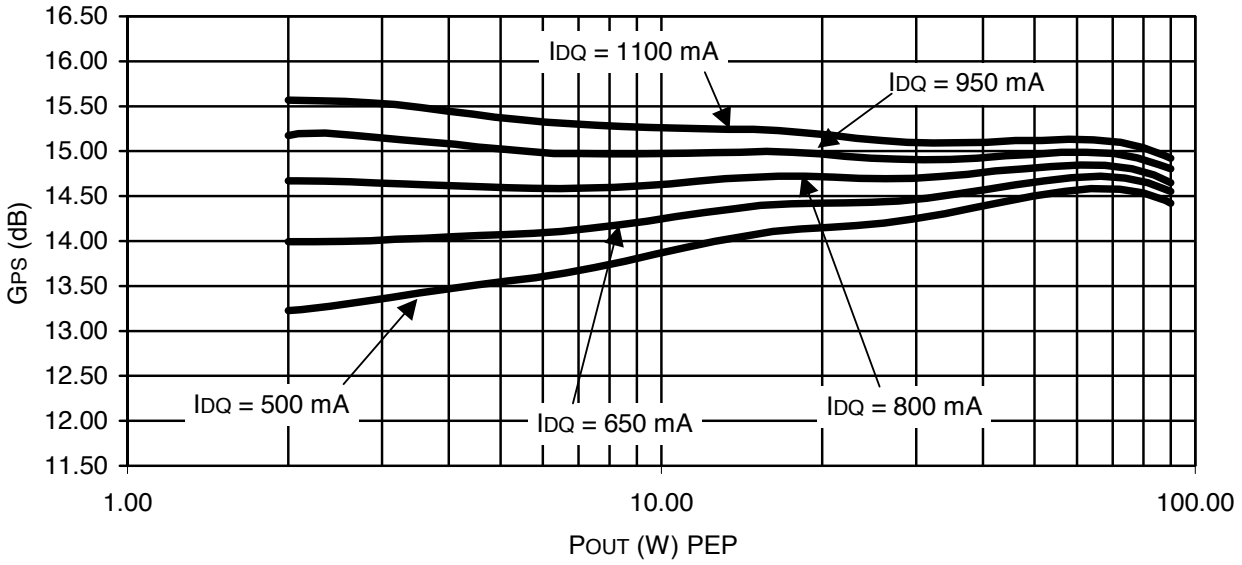


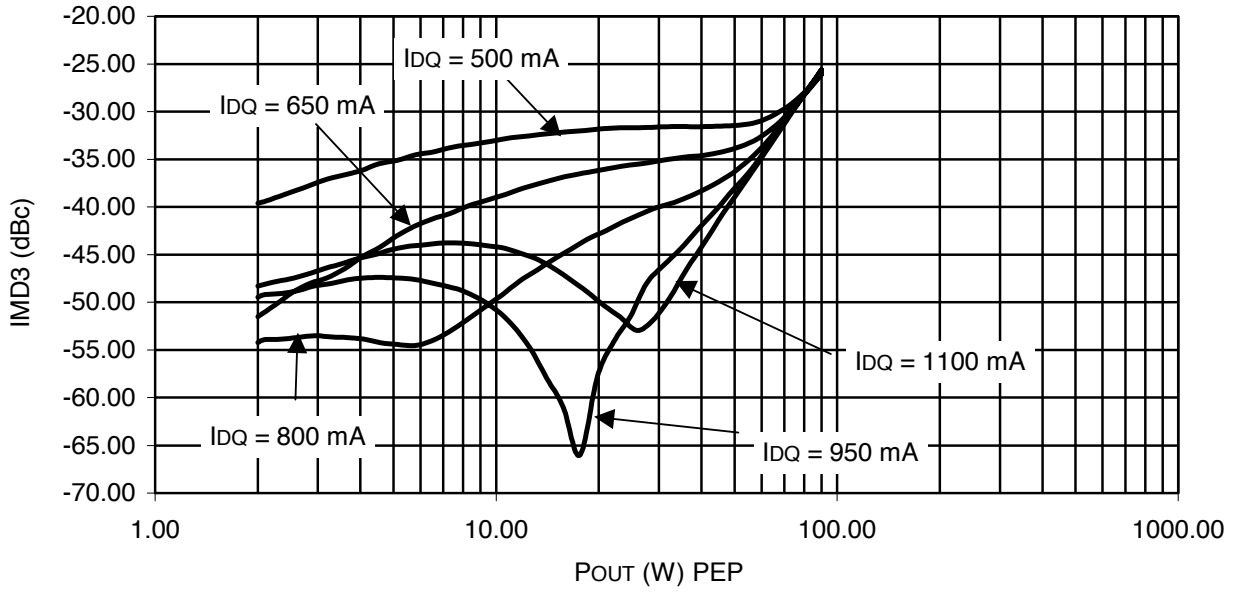
Figure 3. Series Equivalent Input and Output Impedances

Typical Performance Characteristics (continued)



Test Conditions:
V_{DD} 28 Vdc, f1 = 2135 MHz, f2 = 2145 MHz.
Two-tone measurement, 10 MHz tone spacing.

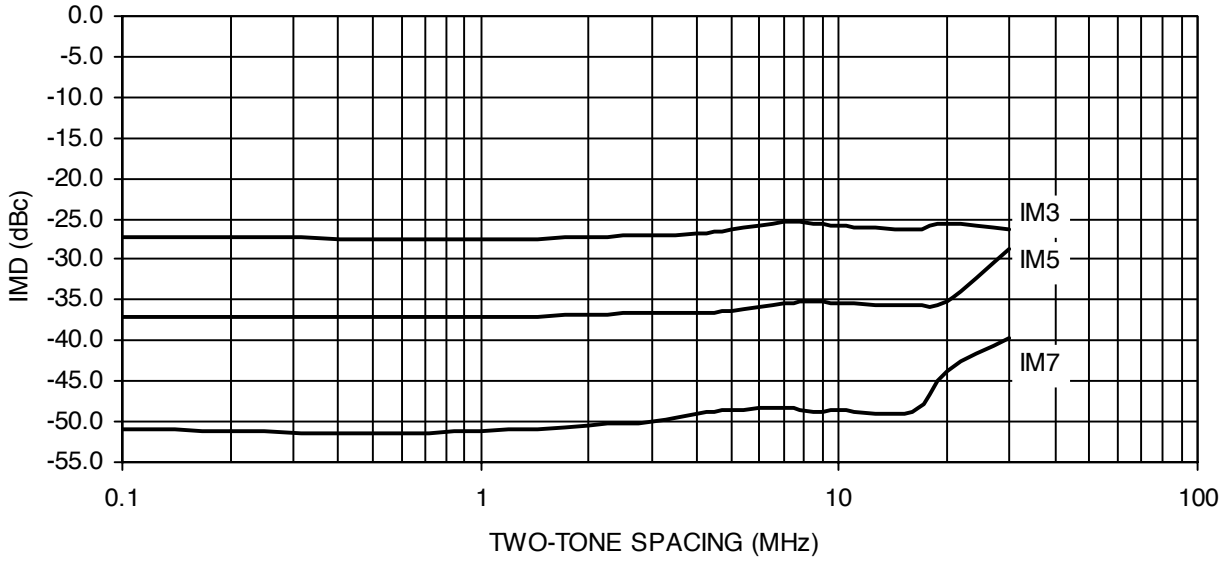
Figure 4. Two-Tone Power Gain vs. Output Power and I_{DQ}



Test Conditions:
V_{DD} 28 Vdc, f1 = 2135 MHz, f2 = 2145 MHz.
Two-tone measurement, 10 MHz tone spacing.

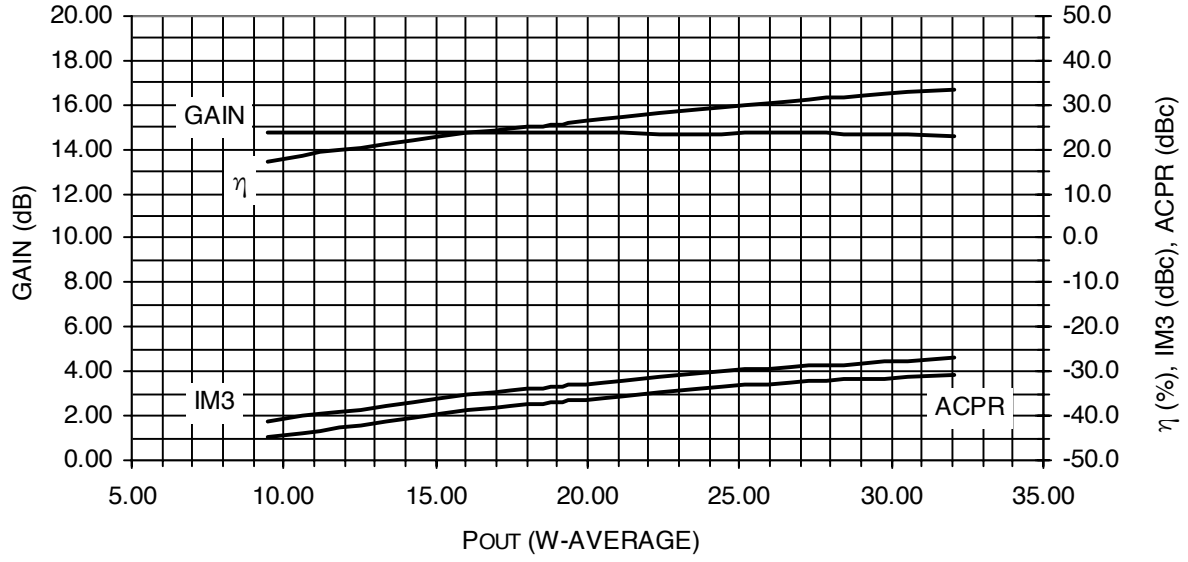
Figure 5. IMD3 vs. Output Power and I_{DQ}

Typical Performance Characteristics (continued)



Test Conditions:
V_{DD} 28 Vdc, f0 = 2140 MHz, P_{OUT} = 90 W PEP.
Two-tone measurement, 10 MHz tone spacing.

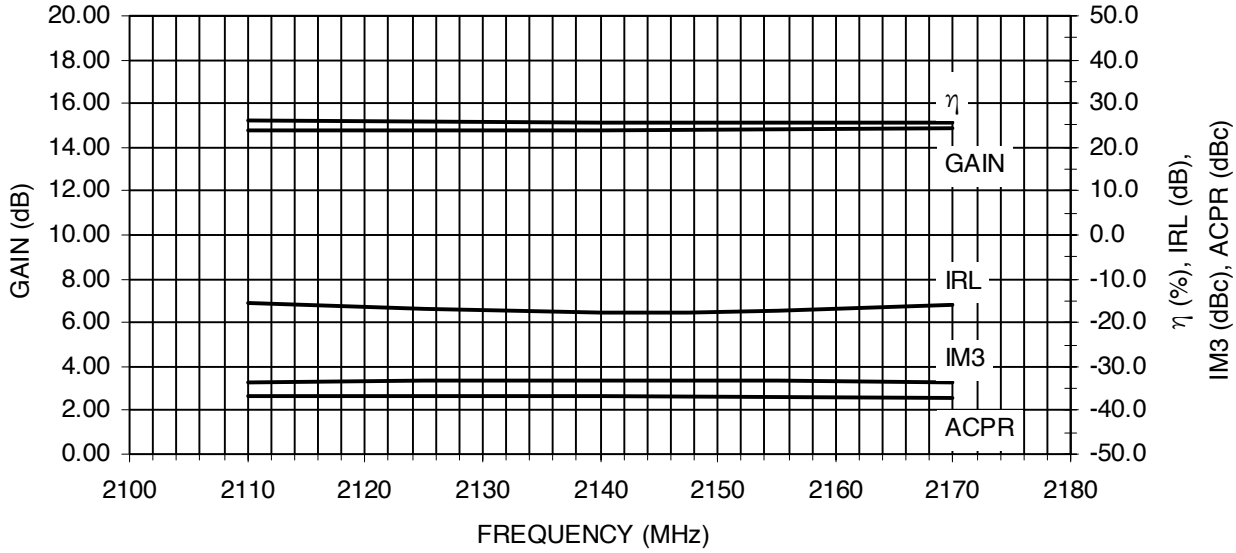
Figure 6. IMD vs. Tone Spacing



Test Conditions:
V_{DD} 28 Vdc, I_{DQ} = 800 mA.
2 carrier W-CDMA 3GPP peak-to-average = 8.5 dB @ 0.01% CCDF, 10 MHz spacing, 3.84 MHz CBW.

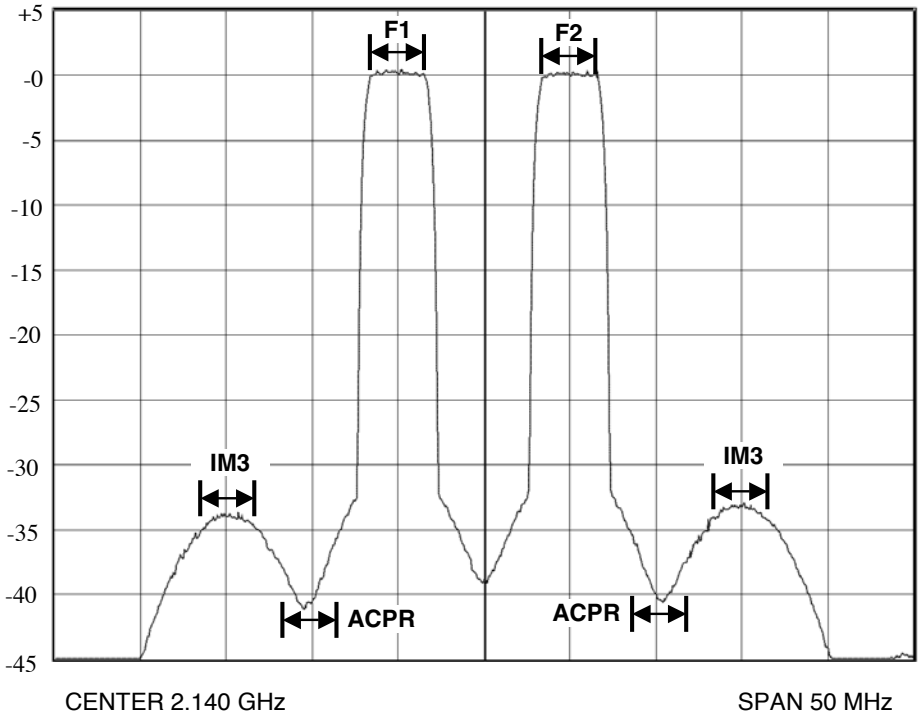
Figure 7. Gain, Efficiency, IM3, and ACPR vs. Output Power

Typical Performance Characteristics (continued)



Test Conditions:
V_{DD} 28 Vdc, P_{OUT} = 19 W, I_{DQ} = 800 mA.
2 carrier W-CDMA 3GPP peak-to-average = 8.5 dB @ 0.01% CCDF, 10 MHz spacing, 3.84 MHz CBW.

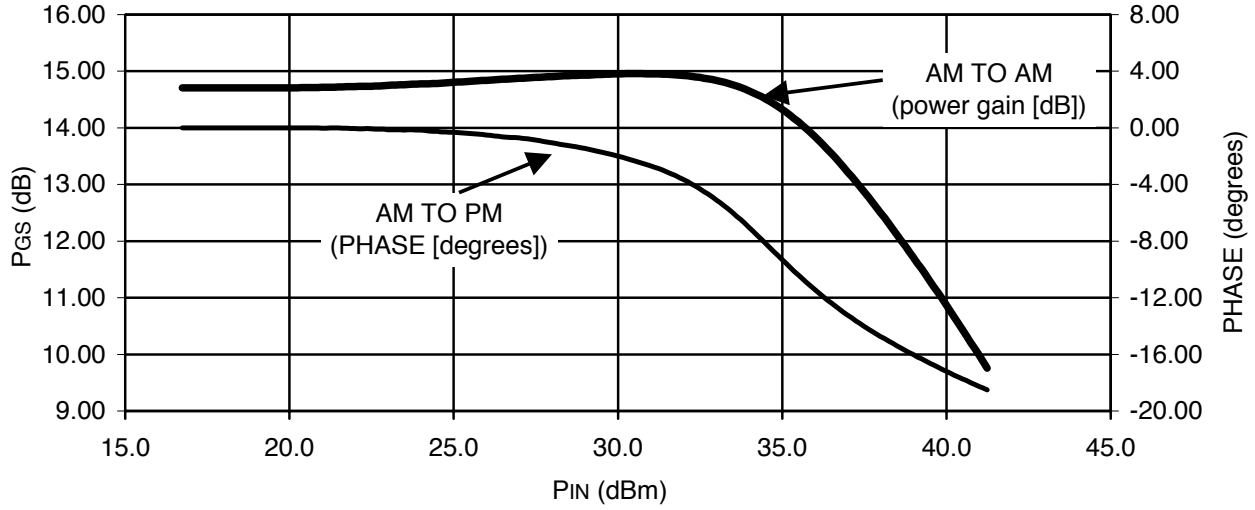
Figure 8. Broadband Performance



Test Conditions:
V_{DD} 28 Vdc, P_{OUT} = 19 W, I_{DQ} = 800 mA.
2 carrier W-CDMA 3GPP peak-to-average = 8.5 dB @ 0.01% CCDF, 10 MHz spacing, 3.84 MHz CBW.

Figure 9. Spectral Plot

Typical Performance Characteristics (continued)



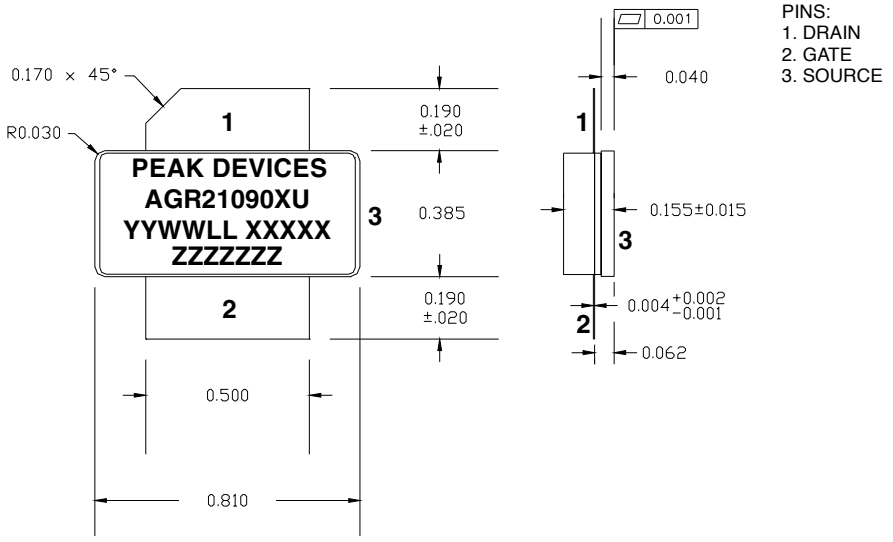
Test Conditions:
V_{DD} 28 Vdc, f0 = 2140 MHz, I_{DQ} = 800 mA.
CW input.

Figure 10. AM-AM and AM-PM Characteristics

Package Dimensions

All dimensions are in inches. Tolerances are ±0.005 in. unless specified.

AGR21090EU



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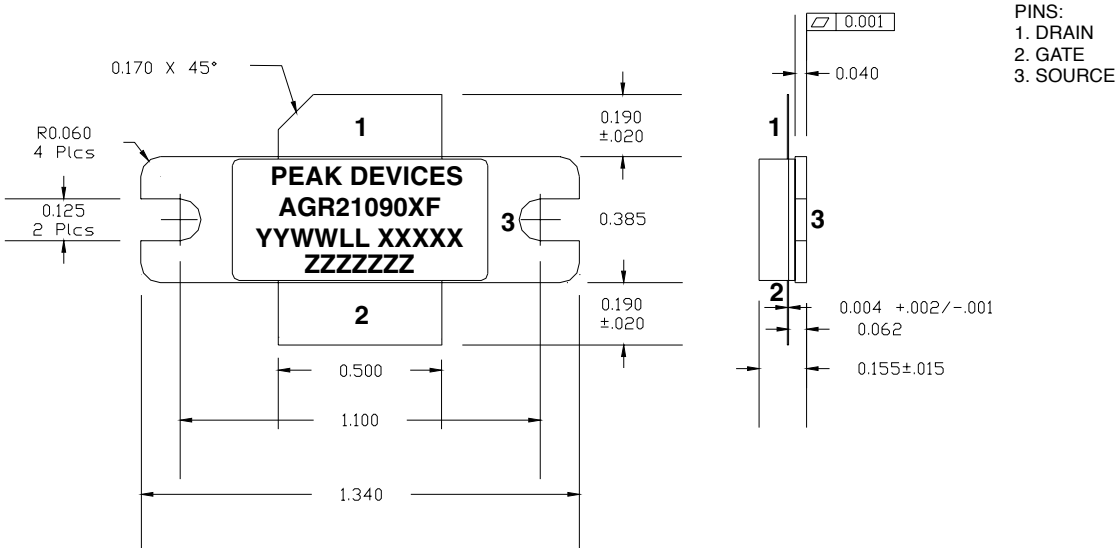

Label Notes:

- M before the part number denotes model program. X before the part number denotes engineering prototype.
- The last two letters of the part number denote wafer technology and package type.
- YYWWLL is the date code including place of manufacture: year year work week (YYWW), LL = location (AL = Allentown, PA; BK = Bangkok, Thailand). XXXXX = five-digit wafer lot number.
- ZZZZZZZ = seven-digit assembly lot number on production parts.
- ZZZZZZZZZZZZ = 12-digit (five-digit lot, two-digit wafer, and five-digit serial number) on models and engineering prototypes.