

Rail-to-rail input/output 29 μ A 420 kHz CMOS operational amplifiers

Features

- Low supply voltage: 1.5 V–5.5 V
- Rail-to-rail input and output
- Low input offset voltage: 800 μ V max (A version)
- Low power consumption: 29 μ A typ
- Gain bandwidth product: 420 kHz typ
- Unity gain stability
- Micropackages: SC70-5, SOT23-5
- Low input bias current: 1 pA typ
- Extended temperature range: -40 to +125° C
- 4 kV HBM

Applications

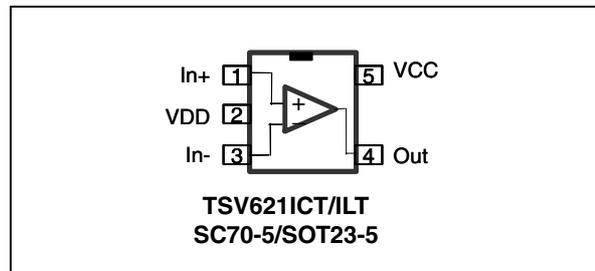
- Battery-powered applications
- Portable devices
- Signal conditioning
- Active filtering
- Medical instrumentation

Description

The TSV621 is a single operational amplifier offering low voltage, low power operation and rail-to-rail input and output.

With a very low input bias current and low offset voltage (800 μ V maximum for the A version), the TSV621 is ideal for applications that require precision. The device can operate at a power supply ranging from 1.5 to 5.5 V, and therefore suits battery-powered devices and extends battery life.

This product features an excellent speed/power consumption ratio, offering a 420 kHz gain bandwidth while consuming only 29 μ A at a 5-V supply voltage.



This operational amplifier is unity gain stable for capacitive loads up to 100 pF.

The device is internally adjusted to provide very narrow dispersion of AC and DC parameters, especially power consumption, product gain bandwidth and slew rate.

The TSV621 presents a high tolerance to ESD, sustaining 4 kV for the human body model.

Additionally, the TSV621 is offered in SC70-5 and SOT23-5 micropackages, with extended temperature ranges from -40° C to +125° C.

All these features make the TSV621 ideal for sensor interfaces, battery-supplied and portable applications, as well as active filtering.

1 Absolute maximum ratings and operating conditions

Table 1. Absolute maximum ratings (AMR)

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage ⁽¹⁾	6	V
V_{id}	Differential input voltage ⁽²⁾	$\pm V_{CC}$	V
V_{in}	Input voltage ⁽³⁾	$V_{DD}-0.2$ to $V_{CC}+0.2$	V
I_{in}	Input current ⁽⁴⁾	10	mA
T_{stg}	Storage temperature	-65 to +150	°C
R_{thja}	Thermal resistance junction to ambient ⁽⁵⁾⁽⁶⁾		°C/W
	SC70-5	205	
	SOT23-5	250	
T_j	Maximum junction temperature	150	°C
ESD	HBM: human body model ⁽⁷⁾	4	kV
	MM: machine model ⁽⁸⁾	300	V
	CDM: charged device model ⁽⁹⁾	1.5	kV
	Latch-up immunity	200	mA

1. All voltage values, except differential voltage are with respect to network ground terminal.
2. Differential voltages are the non-inverting input terminal with respect to the inverting input terminal.
3. $V_{CC}-V_{in}$ must not exceed 6 V.
4. Input current must be limited by a resistor in series with the inputs.
5. Short-circuits can cause excessive heating and destructive dissipation.
6. R_{th} are typical values.
7. Human body model: 100 pF discharged through a 1.5 kΩ resistor between two pins of the device, done for all couples of pin combinations with other pins floating.
8. Machine mode: a 200 pF capacitor is charged to the specified voltage, then discharged directly between two pins of the device with no external series resistor (internal resistor < 5 Ω), done for all couples of pin combinations with other pins floating.
9. Charged device model: all pins plus package are charged together to the specified voltage and then discharged directly to the ground.

Table 2. Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	1.5 to 5.5	V
V_{icm}	Common mode input voltage range	$V_{DD}-0.1$ to $V_{CC}+0.1$	V
T_{oper}	Operating free air temperature range	-40 to +125	°C

2 Electrical characteristics

Table 3. Electrical characteristics at $V_{CC} = +1.8\text{ V}$ with $V_{DD} = 0\text{ V}$, $V_{icm} = V_{CC}/2$, $T_{amb} = 25^\circ\text{ C}$, and R_L connected to $V_{CC}/2$ (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{io}	Offset voltage	TSV621 TSV621A			4 0.8	mV
		$T_{min} < T_{op} < T_{max}$ TSV621 TSV621A			6 2.8	
DV_{io}	Input offset voltage drift			2		$\mu\text{V}/^\circ\text{C}$
I_{io}	Input offset current ($V_{out} = V_{CC}/2$)			1	$10^{(1)}$	pA
		$T_{min} < T_{op} < T_{max}$		1	100	
I_{ib}	Input bias current ($V_{out} = V_{CC}/2$)			1	$10^{(1)}$	pA
		$T_{min} < T_{op} < T_{max}$		1	100	
CMR	Common mode rejection ratio $20 \log (\Delta V_{ic}/\Delta V_{io})$	0 V to 1.8 V, $V_{out} = 0.9\text{ V}$	53	74		dB
		$T_{min} < T_{op} < T_{max}$	51			
A_{vd}	Large signal voltage gain	$R_L = 10\text{ k}\Omega$, $V_{out} = 0.5\text{ V to }1.3\text{ V}$	78	95		dB
		$T_{min} < T_{op} < T_{max}$	73			
V_{OH}	High level output voltage	$R_L = 10\text{ k}\Omega$	35	5		mV
		$T_{min} < T_{op} < T_{max}$	50			
V_{OL}	Low level output voltage	$R_L = 10\text{ k}\Omega$		4	35	mV
		$T_{min} < T_{op} < T_{max}$			50	
I_{out}	Isink	$V_o = 1.8\text{ V}$	6	12		mA
		$T_{min} < T_{op} < T_{max}$	4			
	Isource	$V_o = 0\text{ V}$	6	10		mA
		$T_{min} < T_{op} < T_{max}$	4			
I_{CC}	Supply current (per operator)	No load, $V_{out} = V_{CC}/2$		25	31	μA
		$T_{min} < T_{op} < T_{max}$			33	
AC performance						
GBP	Gain bandwidth product	$R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$, $f = 100\text{ kHz}$	275	340		kHz
F_u	Unity gain frequency	$R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$		280		kHz
ϕ_m	Phase margin	$R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$		45		Degrees
G_m	Gain margin	$R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$		9		dB
SR	Slew rate	$R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$, $A_v = 1$	0.084	0.11	0.14	$\text{V}/\mu\text{s}$

1. Guaranteed by design.

Table 4. $V_{CC} = +3.3\text{ V}$, $V_{DD} = 0\text{ V}$, $V_{icm} = V_{CC}/2$, $T_{amb} = 25^\circ\text{ C}$, R_L connected to $V_{CC}/2$ (unless otherwise specified)

Symbol	Parameter		Min.	Typ.	Max.	Unit
DC performance						
V_{io}	Offset voltage	TSV621			4	mV
		TSV621A			0.8	
		$T_{min} < T_{op} < T_{max}$			6	
		TSV621			2.8	
		TSV621A				
DV_{io}	Input offset voltage drift			2		$\mu\text{V}/^\circ\text{C}$
I_{io}	Input offset current			1	$10^{(1)}$	pA
		$T_{min} < T_{op} < T_{max}$		1	100	pA
I_{ib}	Input bias current			1	$10^{(1)}$	pA
		$T_{min} < T_{op} < T_{max}$		1	100	pA
CMR	Common mode rejection ratio $20 \log (\Delta V_{ic}/\Delta V_{io})$	0 V to 3.3 V, $V_{out} = 1.75\text{ V}$	57	79		dB
		$T_{min} < T_{op} < T_{max}$	53			dB
A_{vd}	Large signal voltage gain	$R_L = 10\text{ k}\Omega$, $V_{out} = 0.5\text{ V to } 2.8\text{ V}$	81	98		dB
		$T_{min} < T_{op} < T_{max}$	76			dB
V_{OH}	High level output voltage	$R_L = 10\text{ k}\Omega$	35	5		mV
		$T_{min} < T_{op} < T_{max}$	50			
V_{OL}	Low level output voltage	$R_L = 10\text{ k}\Omega$		4	35	mV
		$T_{min} < T_{op} < T_{max}$			50	
I_{out}	Isink	$V_o = 5\text{ V}$	30	45		mA
		$T_{min} < T_{op} < T_{max}$	25			
	Isource	$V_o = 0\text{ V}$	30	38		mA
		$T_{min} < T_{op} < T_{max}$	25			
I_{CC}	Supply current (per operator)	No load, $V_{out} = 2.5\text{ V}$		26	33	μA
		$T_{min} < T_{op} < T_{max}$			35	μA
AC performance						
GBP	Gain bandwidth product	$R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$, $f = 100\text{ kHz}$	310	380		kHz
F_u	Unity gain frequency	$R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$		310		kHz
ϕ_m	Phase margin	$R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$		45		Degrees
G_m	Gain margin	$R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$		9		dB
SR	Slew rate	$R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$, $A_V = 1$	0.094	0.12		$\text{V}/\mu\text{s}$

1. Guaranteed by design.

Table 5. $V_{CC} = +5\text{ V}$, $V_{DD} = 0\text{ V}$, $V_{icm} = V_{CC}/2$, $T_{amb} = 25^\circ\text{ C}$, R_L connected to $V_{CC}/2$
(unless otherwise specified)

Symbol	Parameter		Min.	Typ.	Max.	Unit
DC performance						
V_{io}	Offset voltage	TSV621 TSV621A			4 0.8	mV
		$T_{min} < T_{op} < T_{max}$ TSV621 TSV621A			6 2.8	
DV_{io}	Input offset voltage drift			2		$\mu\text{V}/^\circ\text{C}$
I_{io}	Input offset current			1	$10^{(1)}$	pA
		$T_{min} < T_{op} < T_{max}$		1	100	pA
I_{ib}	Input bias current			1	$10^{(1)}$	pA
		$T_{min} < T_{op} < T_{max}$		1	100	pA
CMR	Common mode rejection ratio $20 \log (\Delta V_{ic}/\Delta V_{io})$	0 V to 5 V, $V_{out} = 2.5\text{ V}$	60	80		dB
		$T_{min} < T_{op} < T_{max}$	55			
SVR	Supply voltage rejection ratio $20 \log (\Delta V_{CC}/\Delta V_{io})$	$V_{CC} = 1.8\text{ to }5\text{ V}$	75	102		dB
		$T_{min} < T_{op} < T_{max}$	73			
A_{vd}	Large signal voltage gain	$R_L = 10\text{ k}\Omega$, $V_{out} = 0.5\text{ V to }4.5\text{ V}$	85	98		dB
		$T_{min} < T_{op} < T_{max}$	80			
V_{OH}	High level output voltage	$R_L = 10\text{ k}\Omega$	35	7		mV
		$T_{min} < T_{op} < T_{max}$	50			
V_{OL}	Low level output voltage	$R_L = 10\text{ k}\Omega$		6	35	mV
		$T_{min} < T_{op} < T_{max}$			50	
I_{out}	I_{sink}	$V_o = 5\text{ V}$	40	69		mA
		$T_{min} < T_{op} < T_{max}$	35	65		
	I_{source}	$V_o = 0\text{ V}$	40	74		mA
		$T_{min} < T_{op} < T_{max}$	35	68		
I_{CC}	Supply current (per operator)	No load, $V_{out} = 2.5\text{ V}$		29	36	μA
		$T_{min} < T_{op} < T_{max}$			38	μA
AC performance						
GBP	Gain bandwidth product	$R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$, $f = 100\text{ kHz}$	350	420		kHz
F_u	Unity gain frequency	$R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$		360		kHz
ϕ_m	Phase margin	$R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$		45		Degrees
G_m	Gain margin	$R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$		9		dB
SR	Slew rate	$R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$, $A_v = 1$	0.108	0.14		$\text{V}/\mu\text{s}$

Table 5. $V_{CC} = +5\text{ V}$, $V_{DD} = 0\text{ V}$, $V_{icm} = V_{CC}/2$, $T_{amb} = 25^\circ\text{ C}$, R_L connected to $V_{CC}/2$
(unless otherwise specified) (continued)

Symbol	Parameter		Min.	Typ.	Max.	Unit
e_n	Equivalent input noise voltage	$f = 1\text{ kHz}$		70		$\frac{\text{nV}}{\sqrt{\text{Hz}}}$
THD	Total harmonic distortion	$A_v = 1$, $f = 1\text{ kHz}$, $R_L = 100\text{ k}\Omega$, $V_{icm} = V_{CC}/2$, $V_{out} = 2\text{ V}_{pp}$		0.004		%

1. Guaranteed by design.

Figure 1. Input offset voltage vs input common mode at $V_{CC} = 1.5\text{ V}$

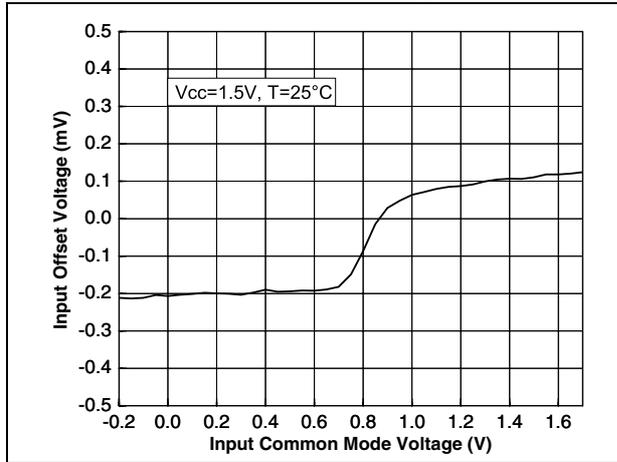


Figure 2. Input offset voltage vs input common mode at $V_{CC} = 5\text{ V}$

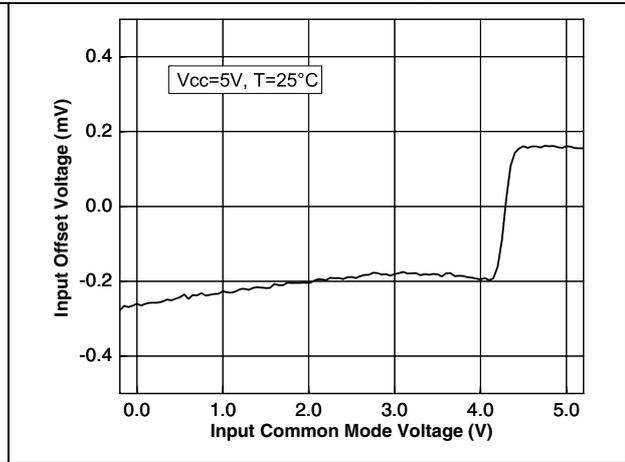


Figure 3. Supply current vs. supply voltage at $V_{icm} = V_{CC}/2$

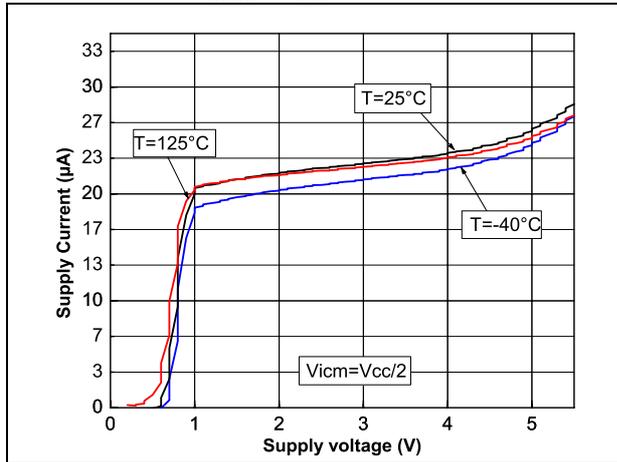


Figure 4. Output current vs. output voltage at $V_{CC} = 1.5\text{ V}$

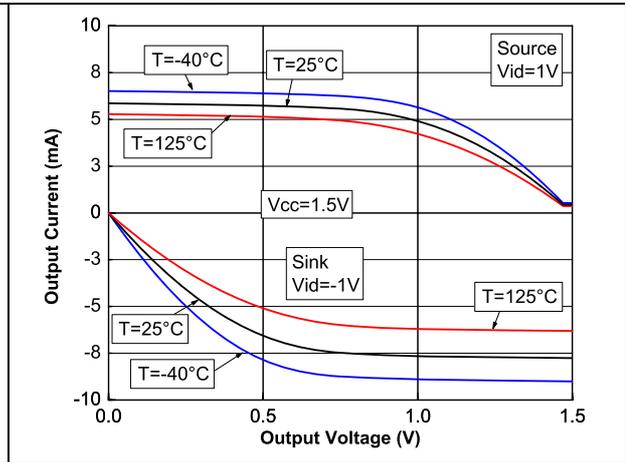


Figure 5. Output current vs. output voltage at $V_{CC} = 5\text{ V}$

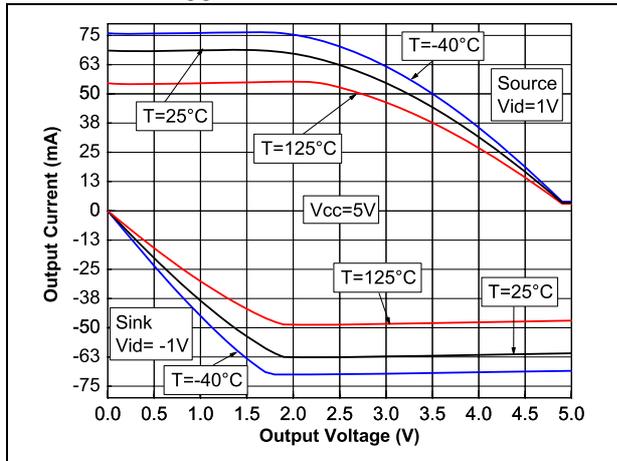


Figure 6. Voltage gain and phase vs. frequency at $V_{CC} = 1.5\text{ V}$

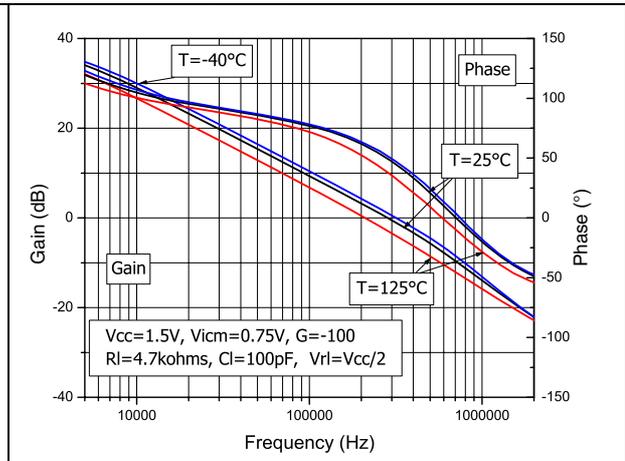


Figure 7. Voltage gain and phase vs. frequency at $V_{CC} = 5\text{ V}$

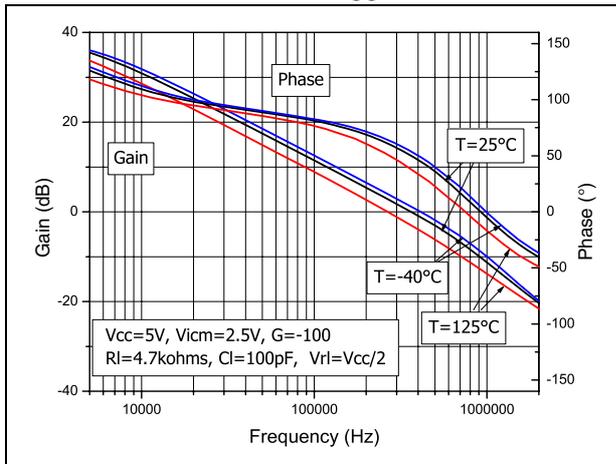


Figure 8. Phase margin vs. output current at $V_{CC} = 1.5\text{ V}$ and $V_{CC} = 5\text{ V}$

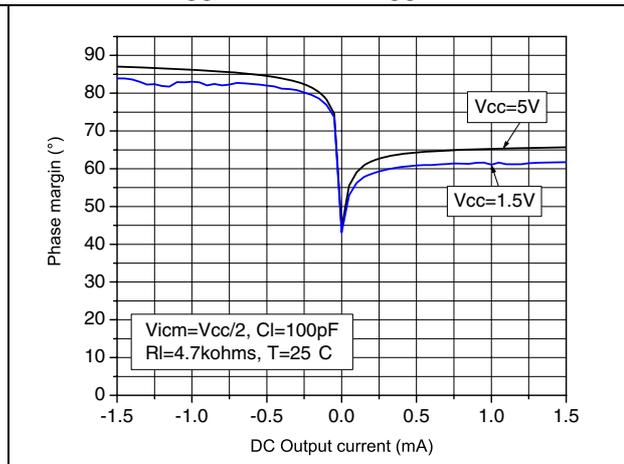


Figure 9. Slew rate vs. supply voltage

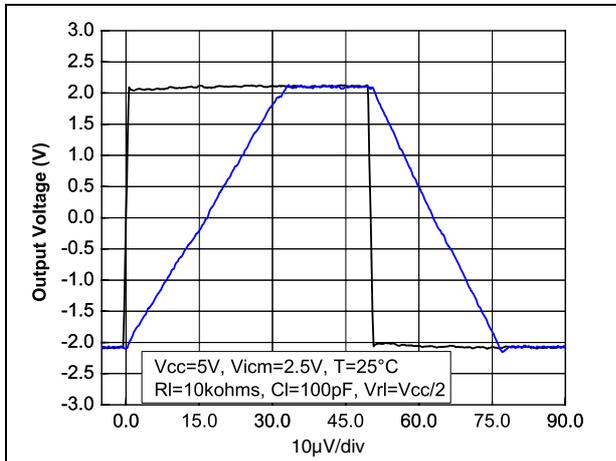


Figure 10. Slew rate vs. supply voltage

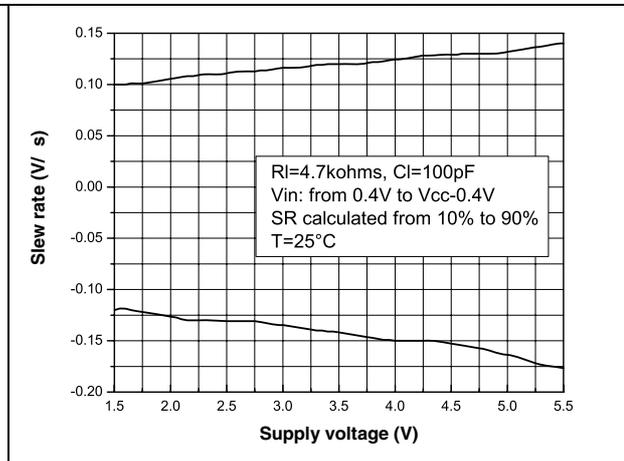


Figure 11. Distortion + noise vs. output voltage

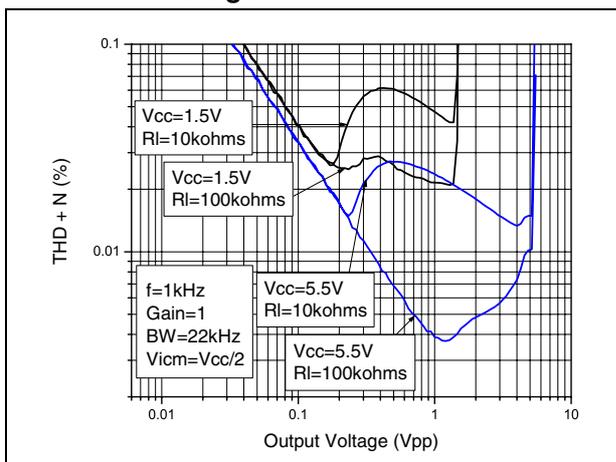


Figure 12. Distortion + noise vs. frequency

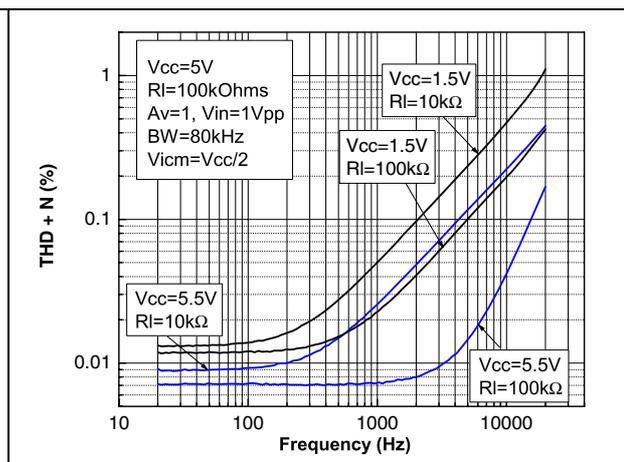
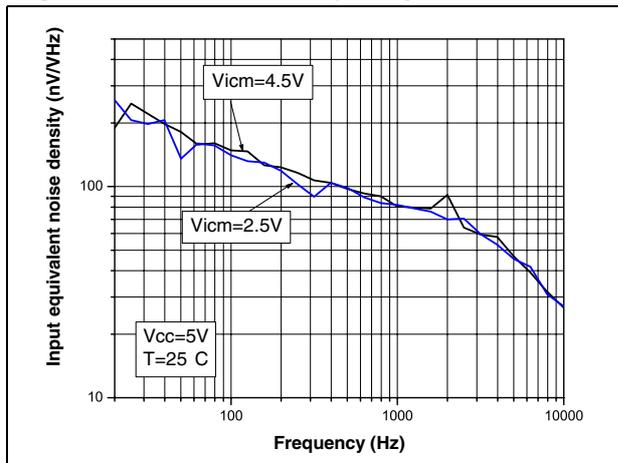


Figure 13. Noise vs. frequency



3 Application information

3.1 Operating voltages

The TSV621 can operate from 1.5 to 5.5 V. Its parameters are fully specified for 1.8-, 3.3- and 5-V power supplies. However, the parameters are very stable in the full V_{CC} range and several characterization curves show the TSV621 characteristics at 1.5 V. Additionally, the main specifications are guaranteed in extended temperature ranges from -40°C to $+125^{\circ}\text{C}$.

3.2 Rail-to-rail input

The TSV621 is built with two complementary PMOS and NMOS input differential pairs. The device has a rail-to-rail input, and the input common mode range is extended from $V_{DD} - 0.1\text{ V}$ to $V_{CC} + 0.1\text{ V}$. The transition between the two pairs appear at $V_{CC} - 0.7\text{ V}$. In the transition region, the performance of CMRR, PSRR, V_{iO} and THD is slightly degraded (as shown in [Figure 14](#) and [Figure 15](#) for V_{iO} vs. V_{iCM}).

Figure 14. Input offset voltage vs input common mode at $V_{CC} = 1.5\text{ V}$

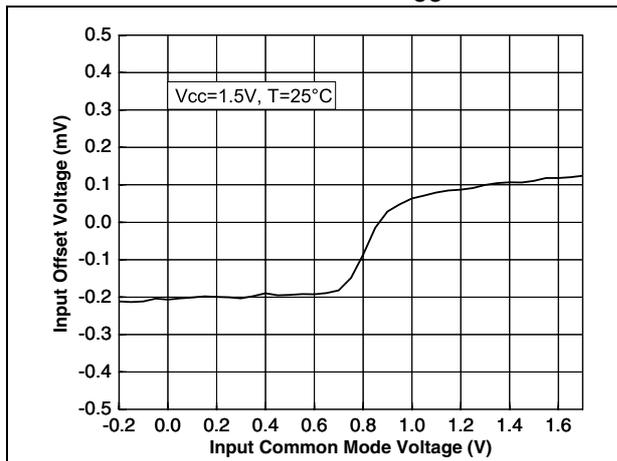
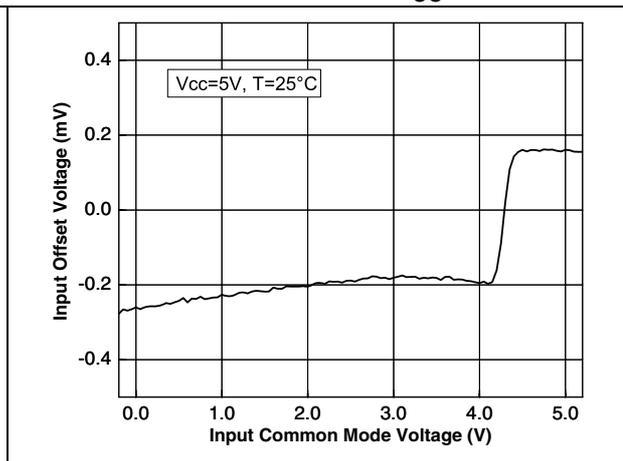


Figure 15. Input offset voltage vs input common mode at $V_{CC} = 5\text{ V}$



The device is guaranteed without phase reversal.

3.3 Rail-to-rail output

The operational amplifier’s output level can go close to the rails: 35 mV maximum above and below the rail when connected to a 10 kΩ resistive load to $V_{CC}/2$.

3.4 Optimization of DC and AC parameters

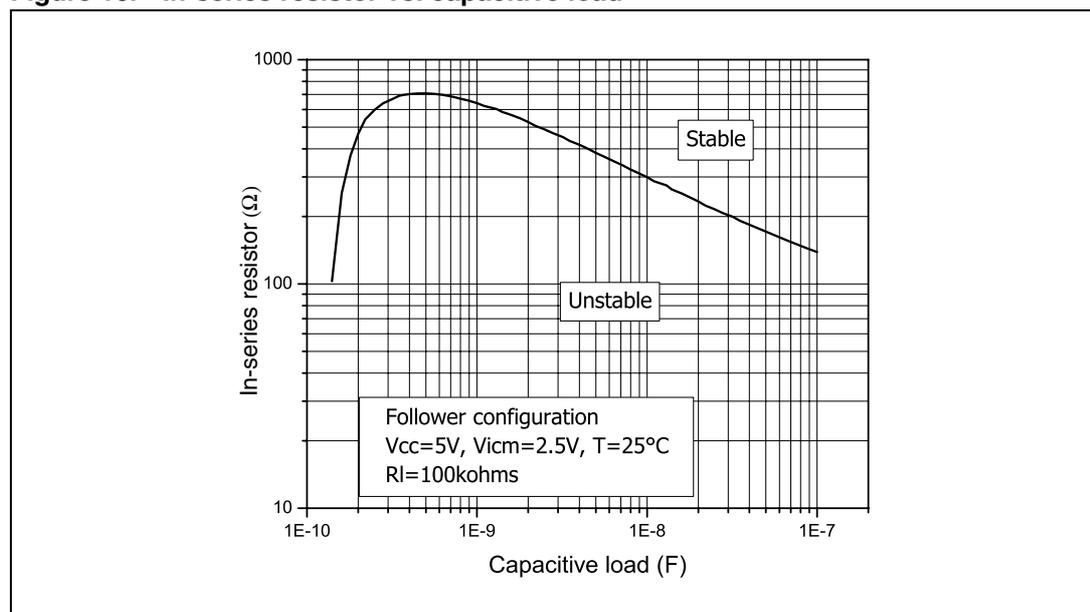
This device uses an innovative approach to reduce the spread of the main DC and AC parameters. An internal adjustment achieves a very narrow spread of current consumption (29 μA typical, min/max at $\pm 17\%$). Parameters linked to the current consumption value, such as GBP, SR and AVd benefit from this narrow dispersion. All parts present a similar speed and the same behavior in terms of stability. In addition, the minimum values of GBP and SR are guaranteed (GBP = 350 kHz min, SR = 0.15 V/ μs min).

3.5 Driving resistive and capacitive loads

These products are micro-power, low-voltage operational amplifiers optimized to drive rather large resistive loads, above 5 k Ω . For lower resistive loads, the THD level may significantly increase.

In a *follower* configuration, these operational amplifiers can drive capacitive loads up to 100 pF with no oscillations. When driving larger capacitive loads, adding a small in-series resistor at the output can improve the stability of the device (see [Figure 16](#) for recommended in-series resistor values). Once the in-series resistor value has been selected, the stability of the circuit should be tested on bench and simulated with the simulation model.

Figure 16. In-series resistor vs. capacitive load



3.6 PCB layouts

For correct operation, it is advised to add 10 nF decoupling capacitors as close as possible to the power supply pins.

3.7 Macromodel

An accurate macromodel of TSV621 is available on STMicroelectronics' web site at www.st.com. This model is a trade-off between accuracy and complexity (that is, time simulation) of the TSV62x operational amplifiers. It emulates the nominal performances of a typical device within the specified operating conditions mentioned in the datasheet. It helps to validate a design approach and to select the right operational amplifier, *but it does not replace on-board measurements*.

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

4.1 SOT23-5 package mechanical data

Figure 17. SOT23-5L package mechanical drawing

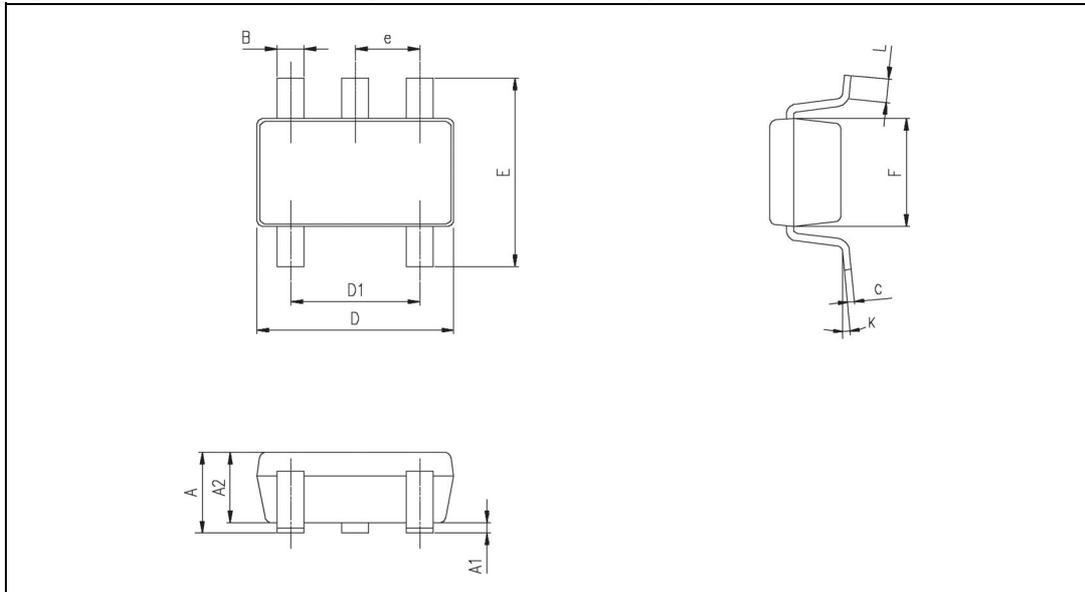


Table 6. SOT23-5L package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.90	1.20	1.45	0.035	0.047	0.057
A1			0.15			0.006
A2	0.90	1.05	1.30	0.035	0.041	0.051
B	0.35	0.40	0.50	0.013	0.015	0.019
C	0.09	0.15	0.20	0.003	0.006	0.008
D	2.80	2.90	3.00	0.110	0.114	0.118
D1		1.90			0.075	
e		0.95			0.037	
E	2.60	2.80	3.00	0.102	0.110	0.118
F	1.50	1.60	1.75	0.059	0.063	0.069
L	0.10	0.35	0.60	0.004	0.013	0.023
K	0°		10°			

4.2 SC70-5 (or SOT323-5) package mechanical data

Figure 18. SC70-5 (or SOT323-5) package mechanical drawing

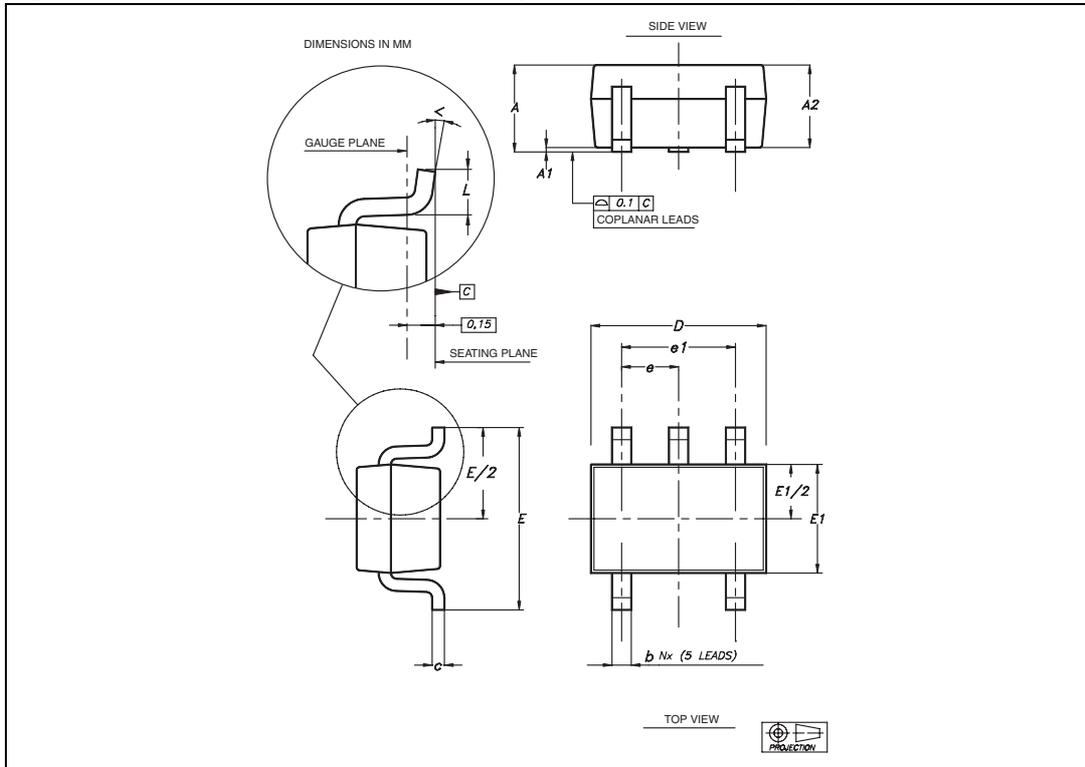


Table 7. SC70-5 (or SOT323-5) package mechanical data

Ref	Dimensions					
	Millimeters			Inches		
	Min	Typ	Max	Min	Typ	Max
A	0.80		1.10	0.315		0.043
A1			0.10			0.004
A2	0.80	0.90	1.00	0.315	0.035	0.039
b	0.15		0.30	0.006		0.012
c	0.10		0.22	0.004		0.009
D	1.80	2.00	2.20	0.071	0.079	0.087
E	1.80	2.10	2.40	0.071	0.083	0.094
E1	1.15	1.25	1.35	0.045	0.049	0.053
e		0.65			0.025	
e1		1.30			0.051	
L	0.26	0.36	0.46	0.010	0.014	0.018
<	0°		8°			

5 Ordering information

Table 8. Order codes

Part number	Temperature range	Package	Packing	Marking
TSV621ILT	-40°C to +125°C	SOT23-5	Tape & reel	K106
TSV621ICT	-40°C to +125°C	SC70-5	Tape & reel	K16

6 Revision history

Table 9. Document revision history

Date	Revision	Changes
12-Jan-2009	1	Initial release.

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