E7802

Low Cost, Dual-Channel, 15V Pin Electronics Driver/Window Comparator

Description

The E7802 is a dual-channel pin electronics driver and window comparator product fabricated in a wide voltage Bi-CMOS process. It is designed specifically for Test During Burn In (TDBI) applications and low cost testers, where cost, functional density, and power are all at a premium.

The E7802 incorporates two channels of programmable drivers and window comparators into a small 5 mm X 5 mm QFN package. Each channel has per pin driver levels, data, and high impedance control, along with per-pin high and low window comparator threshold levels.

The E7802 was specifically designed to offer a low cost, high density driver and window comparator solution with excellent small swing performance and stable timing characteristics.

A 15V driver output and receiver input range allow the E7802 to interface directly with TTL, ECL, CMOS (3V, 5V, and 7V), LVCMOS, and custom level circuitry, as well as high voltage levels required for many special test modes in Flash Devices and for stressing devices under test.

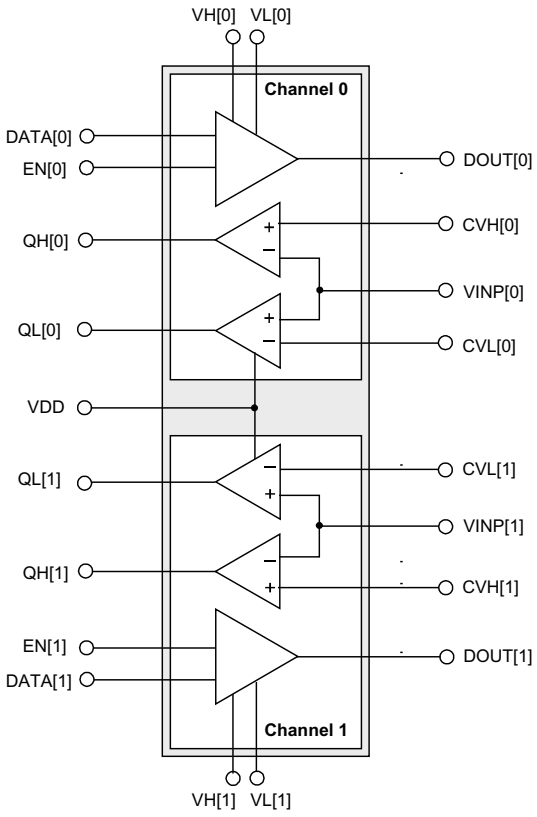
Applications

- Burn In ATE
- Low Cost ATE
- Instrumentation

Features

- 15V I/O Range
- 200 mA DC Current Capability
- Low Output Impedance
- 50 MHz Operation
- Driver Short Circuit Protection
- Per-Pin Flexibility
- Programmable Input Thresholds
- LVTTL Compatible I/O
- Small footprint (5 mm x 5 mm QFN with Exposed Heat Slug)
- Improved Small Signal Swing and Timing Performance
- Low Preshoot/Overshoot/Undershoot
- Pin Compatible with E7801 and E7803

Functional Block Diagram



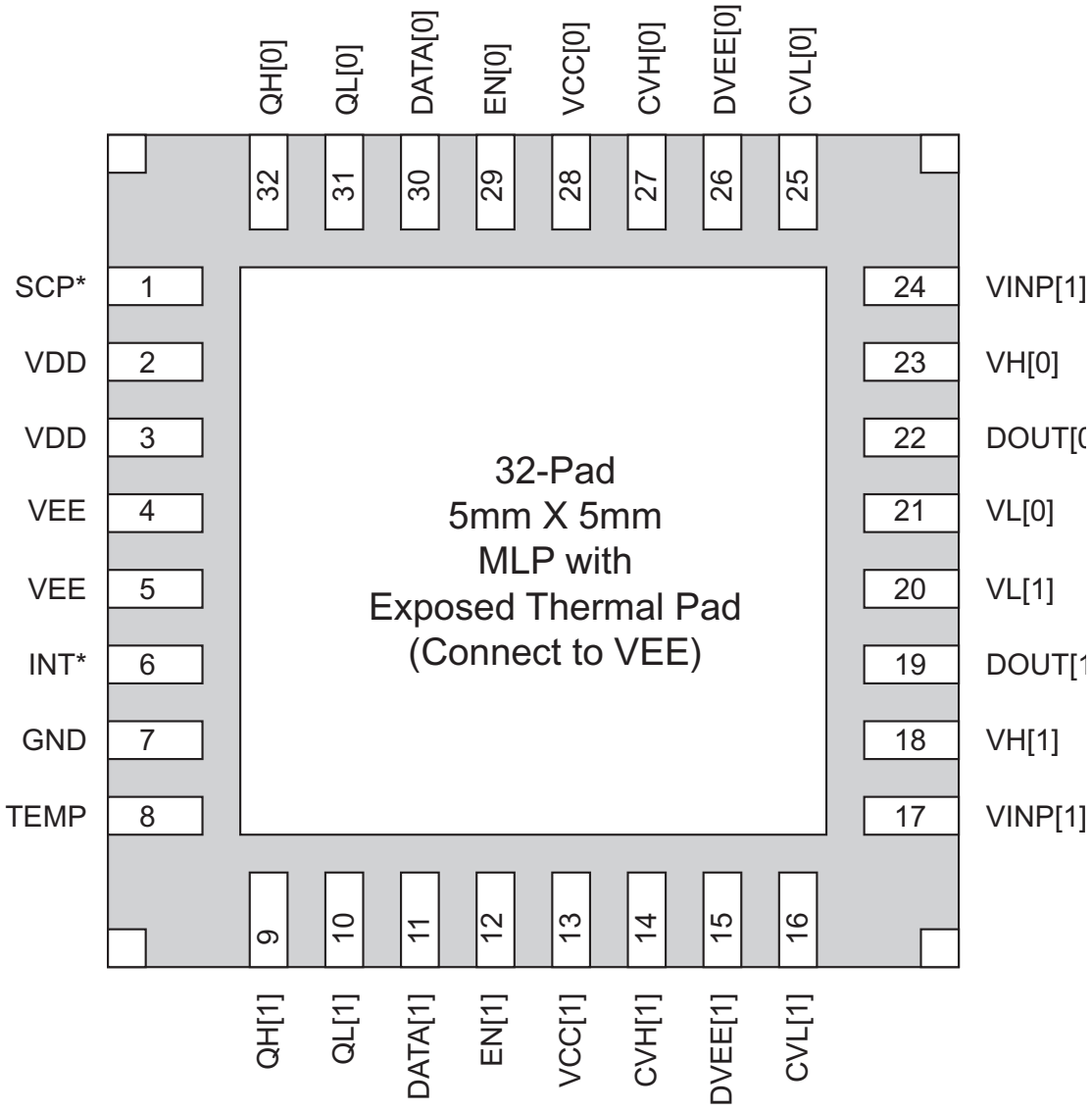
PIN Description

Customer Pin Descriptions

Pin Name	Pin Number	Description
DATA[0:1]	30, 11	Digital inputs which determine the high/low output state of the driver, when it is enabled.
EN[0:1]	29, 12	Digital input which enables/disables the driver.
QH[0:1] QL[0:1]	32, 9 31, 10	Comparator digital outputs.
DOUT[0:1]	22, 19	Driver Outputs.
VINP[0:1]	24, 17	Comparator Inputs.
VH[0:1]	23, 18	Unbuffered analog inputs that set the driver high voltage level.
VL[0:1])	21, 20	Unbuffered analog inputs that set the driver low voltage level.
CVH[0:1]	27, 14	Analog inputs that set the threshold for the high comparator.
CVL[0:1]	25, 16	Analog inputs that set the threshold for the low comparator.
VDD	2, 3	Digital supply.
GND	7	Ground pad. Connect to 0V.
VCC[0:1]	28, 13	Positive power supply.
VEE	4, 5, Center Pad	Negative power supply.
DVEE[0:1]	26, 15	Driver negative supply.
SCP*	1	Short circuit protection enable pin (has 5.3Kohms internal pull-down to GND). Connect to VDD if short circuit protection is not required in the application.
INT*	6	Open drain short circuit flag that pulls-down to indicate that a channel of the E7802 is in short circuit protection mode.
TEMP	8	Connected to anode of temperature sensing diodes.

PIN Description (continued)

Pinout



Circuit Description

Description

The E7802 supports independently programmable driver high and low levels as well as tristate per channel. There are no shared lines between the two drivers. The EN and DATA signals are inputs that are used to control the output of the driver as shown in Table 1. Each channel of the E7802 features a window comparator with separate high and low threshold levels (CVH, CVL), as well as independent digital outputs (QH, QL).

EN	DATA	DOUT
0	0	HiZ
0	1	HiZ
1	0	VL
1	1	VH

Table 1. Driver Functionality

NOTE: The voltage at DOUT needs to stay at DVEE ≤ DOUT ≤ VCC at all times (HiZ/Active).

Drive High and Low

VH and VL define the logical "1" and "0" levels of the driver, and can be adjusted to produce driver output swings from 200mV up to 15V.

The VH and VL inputs are unbuffered. They provide the driver output current (see Figure 1), so the source of VH and VL must have ample current drive capability. (See Applications Note PE-A1).

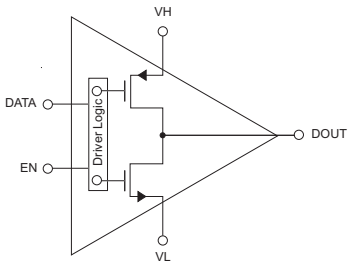
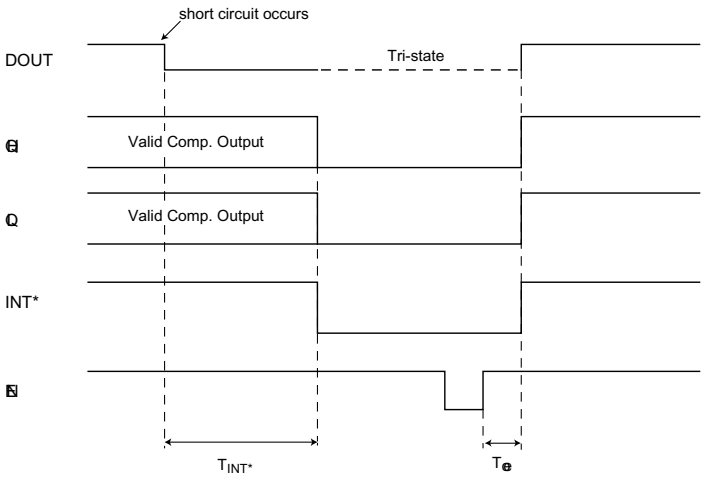


Figure 1.

Driver Output Protection

The E7802's drivers feature short circuit protection circuitry that prevents them from being damaged in the event of a short circuit at their outputs. In the event of a short circuit at the driver output and short circuit protection is enabled (SCP*=0), DOUT will place itself in a high impedance state and the comparator outputs, QH and QL, are designed to both assert a Logic "0" to indicate that a short circuit event has occurred. In addition to the comparator outputs pulling down, the INT* pin will become active (pull-down) when either channel detects a s hort-circuit condition. Multiple E7802 INT* pins may be wire-or'd together with a single VDD pull-up load to create a system-wide notification signal that a short circuit has occurred on one of the chanels in the system. After a short circuit event has occurred, the driver can be reset to the active state by toggling the EN pin from Logic "0" to Logic "1" .

Either after power-up or after short circuit protection is enabled, the EN pin needs to be toggled from Logic "0" to Logic "1" to allow the driver to power up in the active state and ensure the short circuit protection is reset for proper operation (see Timing Diagram below).



Because of the nature of the SCP circuit design, it is recommended that the user have SCP enabled only under the valid SCP operating zone. Refer to Figure 2 for the conditions.

Circuit Description (continued)

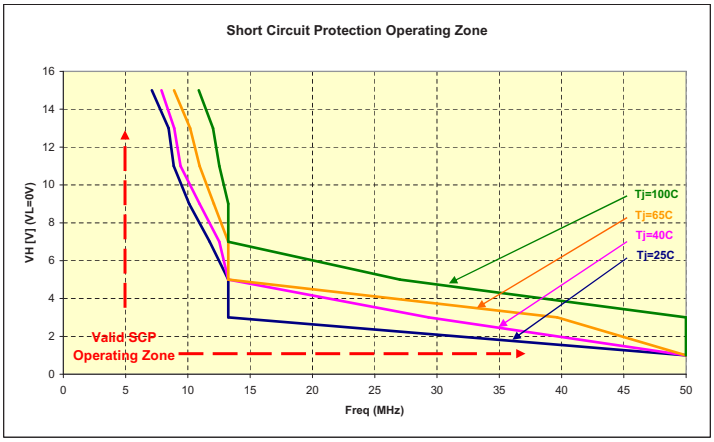


Figure 2.

For applications that require operation outside the valid SCP operating zone, the user can use the SCP to check for any short circuit occurrence down the line and protect the driver from over-current damage before running it at the desired operating conditions. Refer to the following procedure:

1. While the driver is in HiZ (EN=0), enable short-circuit protection (SCP*=0)

2. Set VH to the maximum programmable voltage in the system, switch DATA to Logic "1" and toggle the EN pin from Logic "0" to "Logic "1".

3. After the driver is enabled, wait approximately 2 µs and monitor all INT* pins in the system to determine if there is any short circuit occurrence.

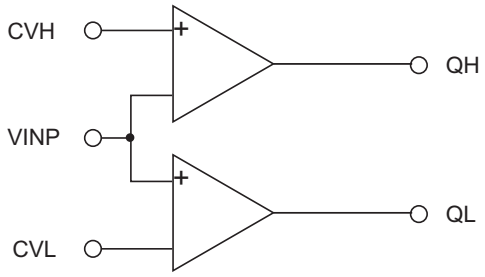
4. If the INT* signal remains high, no short circuit condition is detected. If the INT* signal becomes low (active), this indicates a short circuit condition has occurred in one or more channels in the system. Determine the shorted channel(s) by checking the comparator outputs (QH=0, QL=0). Remove the fault condition in each channel respectively and reset those driver(s)

5. Repeat Steps 3 through 4 with minimum programmable VL in the system and switch DATA to Logic "0".

6. Disable short circuit protection (SCP*=1) and start running the driver at the desired operating conditions.

NOTE: If short circuit protection is used outside of the valid SCP operating zone, false SCP triggers can occur which will disable the driver output, DOUT.

Window Comparator



Each channel of the E7802 features two comparators connected in a window comparator configuration. CVH and CVL are high impedance analog voltage inputs that establish the upper and lower thresholds for the window comparator. CVH should always be greater than or equal to CVL for normal comparator operation. QH and QL are digital outputs that indicate where a voltage measurement lies in relation to the CVH and CVL thresholds and are also used to indicate when short circuit protection is engaged as shown in Table 2.

Condition	QH	QL	INT*
Measurement is within the range established by CVH and CVL	1	1	1
Measurement is above the range established by CVH and CVL	0	1	1
Measurement is below the range established by CVH and CVL	1	0	1
Short circuit protection is engaged and Driver is disabled	0	0	0

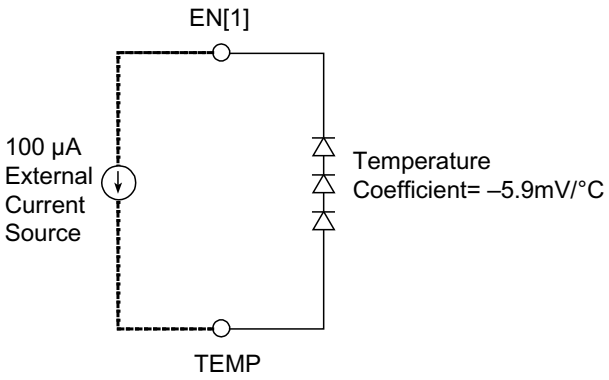
Table 2. Comparator Output Truth Table

The receiver thresholds can be used over a range of VEE +3V to VCC -3V. The VINP input of the receiver is designed to withstand voltages from VEE+2V to VCC such that the comparator input can be directly connected to the driver output without being damaged.

NOTE: DVEE MUST be set appropriately in order to accommodate VINP input voltages of VEE + 2V when DOUT and VINP are connected in an application.

Thermal Diode String

The E7802 features an internal diode string connected between EN[1] and TEMP that can be used to perform device junction temperature measurements as shown in the figure below. NOTE: EN[1] must be asserted "low" when making temperature measurements.



$$T_j[°C] = \frac{\left(0.7195 - \frac{TEMP - EN[1]}{3}\right)}{0.001967}$$

Application Information

Power Supply Decoupling

VCC, VEE, and DVEE should be decoupled to GND with a .1 µF chip capacitor in parallel with a .001 µF chip capacitor for best AC performance. A VCC, VEE, and DVEE plane, or at least a solid power bus, is recommended for optimal performance.

VH and VL Inputs

As the VH and VL inputs are unbuffered to the driver and need to supply the output current which can be quite large during edge transitions, bypass capacitors for these inputs are needed to supply the transient currents in proportion to the output current requirements (See Applications Note PE-A1).

For applications where VH and VL are shared over multiple channels, a solid power plane to distribute these levels with local bypassing is recommended for best AC performance .

Power Supply Sequencing/Latch-Up Protection

In order to avoid the possibility of latch-up when powering this device up (or down), be careful that the conditions listed in the Absolute Maximum Ratings are never violated. The power supplies should never be in reverse-polarity with respect to ground, and the input signals should never go beyond the power supply rails.

Furthermore, the lower-voltage supplies should never be greater than the higher-voltage supplies. This can easily be implemented by utilizing the diode circuit depicted in Figure 3 for each PCB utilizing the E7802. The following conditions must be met at all times during power-up and power-down:

1. VEE <= DVEE <= VDD <= VCC
2. VEE <= Analog Inputs <= VCC
3. GND <= Digital Inputs <= VDD

The following sequencing can be used as a guideline when powering up:

1. VEE(substrate)
2. VCC
3. VDD
4. Digital Iputs
5. Analog Inputs

The three diode configuration shown in Figure 3 should be used on a once-per-boad basis to help ensure that proper supply polarities are maintained.

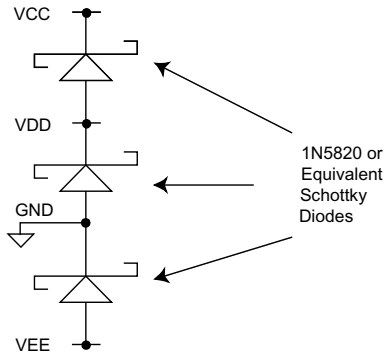
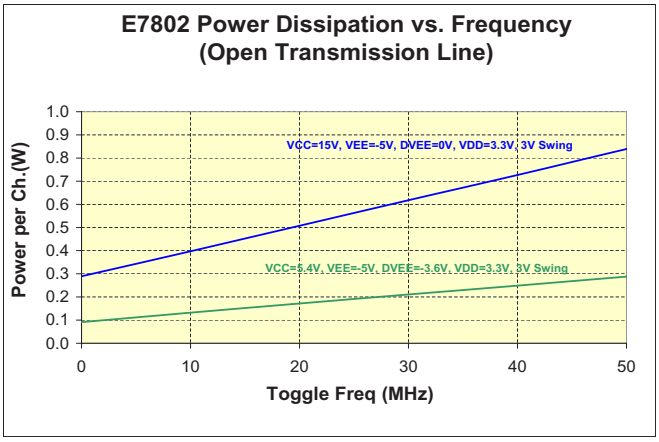


Figure 3. Power Supply Protection Scheme

Warning: It is extremely important that the voltage on any device pin does not exceed the range of VEE -0.5V or VCC +0.5V at any time, either during power up, normal operation, or during power down. Failure to adhere to this requirement could result in latch-up of the device which could be destructive if the system's power supplies are capable of supplying large amounts of current. Even if the device is not immediately destroyed, the cumulative damage caused by the stress of repeated latchup may affect device reliability.

Computing Maximum Power Comsumption

The power consumption of the E7802 increases with increasing frequency and output voltage swing. The diagram below shows the power consumption of the E7802 at a couple of different voltage swings across the frequency range with both channels toggling.



Cooling Considerations

Depending on the maximum operating frequencies and voltage swings the E7802 will need to drive, it may require the use of an external heatsink to keep the maximum die junction temperature within a safe range and below the specified maximum of 100°C.

The E7802 package has an external heat slug located on the bottom side of the package to efficiently conduct heat away from the die to the package surface. The thermal resistance of the package to the slug is the θjc (junction-to-case) and is specified at <1°C/W.

Additional cooling capability can be attained through the use of a heat sink on the top of the package. The plastic on the top of the E7802's package is extremely thin and has an effective thermal impedance of <4°C/W.

In order to calculate what type of heatsinking should be applied to the E7802, the designer needs to determine the worst case power dissipation of the device in the application. The graph above gives a good visual relationship of the power dissipation to the maximum operating frequency (all channels simultaneously) and driver output voltage swings. Another variable that needs to be determined is the maximum ambient air temperature that will be surrounding or blowing on the device and/or the heatsink system in the application (assuming an air cooled system).

A heatsinking solution should be chosen to be at or below a certain thermal impedance known as the Rθ in units of deg-C/Watt. The heatsinking system is a combination of factors including the actual heatsink chosen and the selection of the interface material between the E7802 package and the heatsink itself. This could be thermal grease or thermal epoxy, each of which has its own thermal impedance.

The heatsinking solution will also depend on the volume of air passing over the heatsink and at what angle the air is impacting the heatsink. There are many options available in selecting a heatsinking system. The formula below shows how to calculate the required maximum thermal impedance for the entire heatsink system. Once this is known, the designer can evaluate the options that best fit the system design and meet the required Rθ.

$$R\theta(\text{heatsink system}) = (Tjmax - Tambient - P*\theta jc)/P$$

where:

Rθ (heatsink_system) is the thermal resistance of the entire heatsink system

Tjmax is the maximum die temperature (100°C)

Tambient is the maximum ambient air temperature expected at the heatsink (°C)

P is the maximum expected power dissipation of the E7802 (Watts)

θjc is the thermal impedance of the E7802 junction to case (<1°C/W though bottom, <4°C/W through top)

The value of the thermal resistance of the E7802 package junction to air with 400 linear feet per minute (LFPM) of airflow is specified at 28°C/W. At operating points greater than or equal to this value, no additional heatsinking is needed to keep the die temperature below the maximum 100°C as long as the ambient temperature of the 400 LFPM air does not exceed 70°C.

More information on heatsink system selections can be read on heatsink vendors' web sites and in the Semtech Application Note "ATE-A2 *Cooling High Power, High Density Pin Electronics.*

Driving a Resistive Load

In addition to the VCC and VEE power supply levels, the "driver high" (VH) and "driver low" (VL) levels used in an application also have an effect on the total power dissipation of the device illustrated using Figure 4.

Application Information (continued)

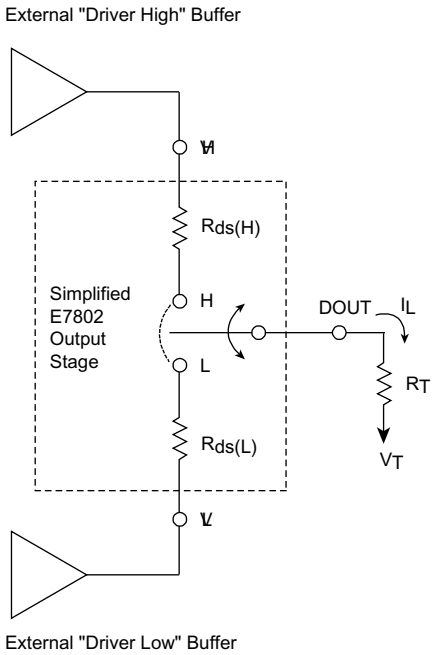


Figure 4. Simplified Functional Schematic of E7802 Output Stage and External Buffers

The CMOS switches of the E7802's output stage have on-resistance values (depicted by $R_{ds(H)}$ and $R_{ds(L)}$ in Figure 4) that vary as a function of VH and VL voltage levels. The amount of current required by the load impedance, R_T, is also a function of the VH and VL voltage levels as follows:

Switch in Figure 3 is in position "H":

$$I_{L(H)} = \frac{VH - V_T}{R_{ds(H)} + R_T}$$

Switch in Figure3 is in position "L":

$$I_{L(L)} = \frac{VL - V_T}{R_{ds(L)} + R_T}$$

Therefore, the per-channel power dissipation due to the E7802 driving resistive load is:

$$P = [I_L^2{}_{(H)} \times R_{ds(H)} \times D] + [I_L^2{}_{(L)}] \times R_{ds(L)} \times (1-D)]$$

where:

P is the total power dissipated by E7802 as a result of the resistive load, R_L [Ω]

$I_{L(H)}$ is the amount of current required by R_L during a logic "high" state [A]

$R_{ds(H)}$ is the output impedance of the E7802 driver when driving a logic "high" state [Ω]

D is the normalized amount of time that logic "high" is driven (Duty Cycle)

$I_{L(L)}$ is the amount of current required by R_L during a logic "low" state [A]

$R_{ds(L)}$ is the output impedance of the E7802 driver when driving a logic "low" state [Ω]

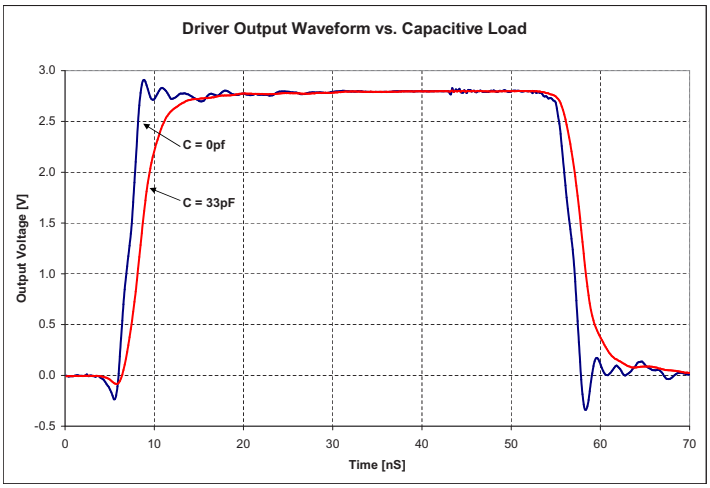
Driving Currents Larger than 200mA

The driver channels of the E7802 can be connected in parallel to drive currents larger than the rated 200mA per individual driver.

Optimizing Driver Waveforms

Overshoot/Undershoot/Preshoot

E7802 Driver overshoot, undershoot and preshoot are functions of the DOUT edge rate. Slower DOUT edge rates are associated with smaller overshoot, undershoot and preshoot amplitudes. The DOUT edge rate is influenced by the amount of capacitance that is present on the driver output with larger capacitance resulting in slower edge rates and less overshoot as shown below.



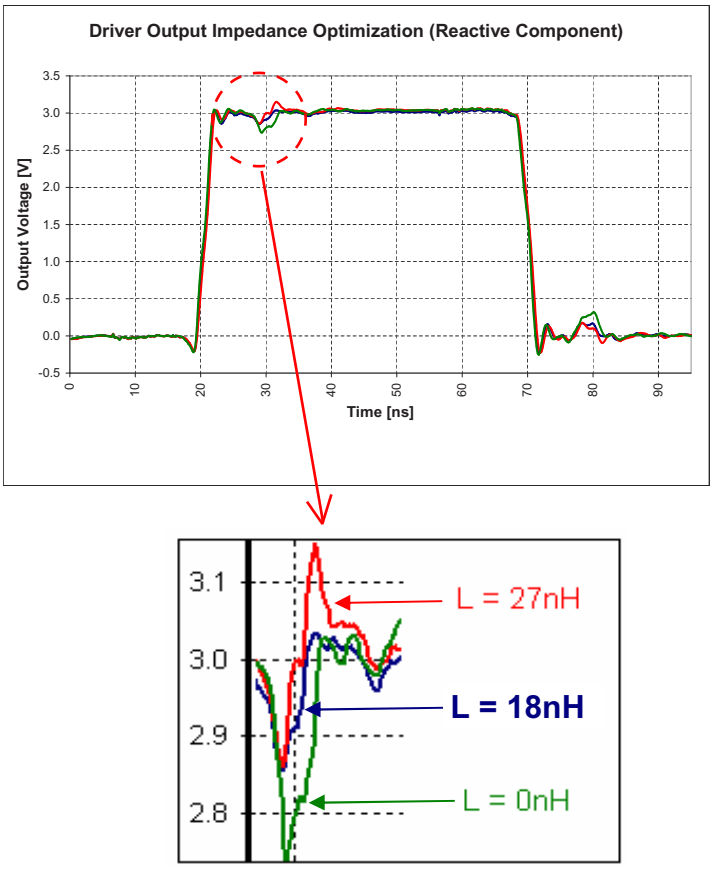
Overshoot, undershoot and preshoot are also influenced by power supply levels. In general, lower VCC levels are associated with less overshoot and better small-swing performance.

Output Impedance Matching

How well the driver output impedance matches a transmission line connected to it has a direct effect on waveform characteristics. Driver output impedance can be separated into two components:

1) *Real Component:* Accounts for the resistive (DC) portion of the driver output impedance and is matched to a transmission line by using an external "back-match" resistor. Using empirical methods in our lab, we have determined that a 45.3Ω back-match resistor offers the best real impedance matching for a 50Ω transmission line. See Applications Note PE-A2, "*Optimizing the Output Configuration of Semtech Bipolar Pin Drivers*" for more details on selecting the proper "back-match" resistor.

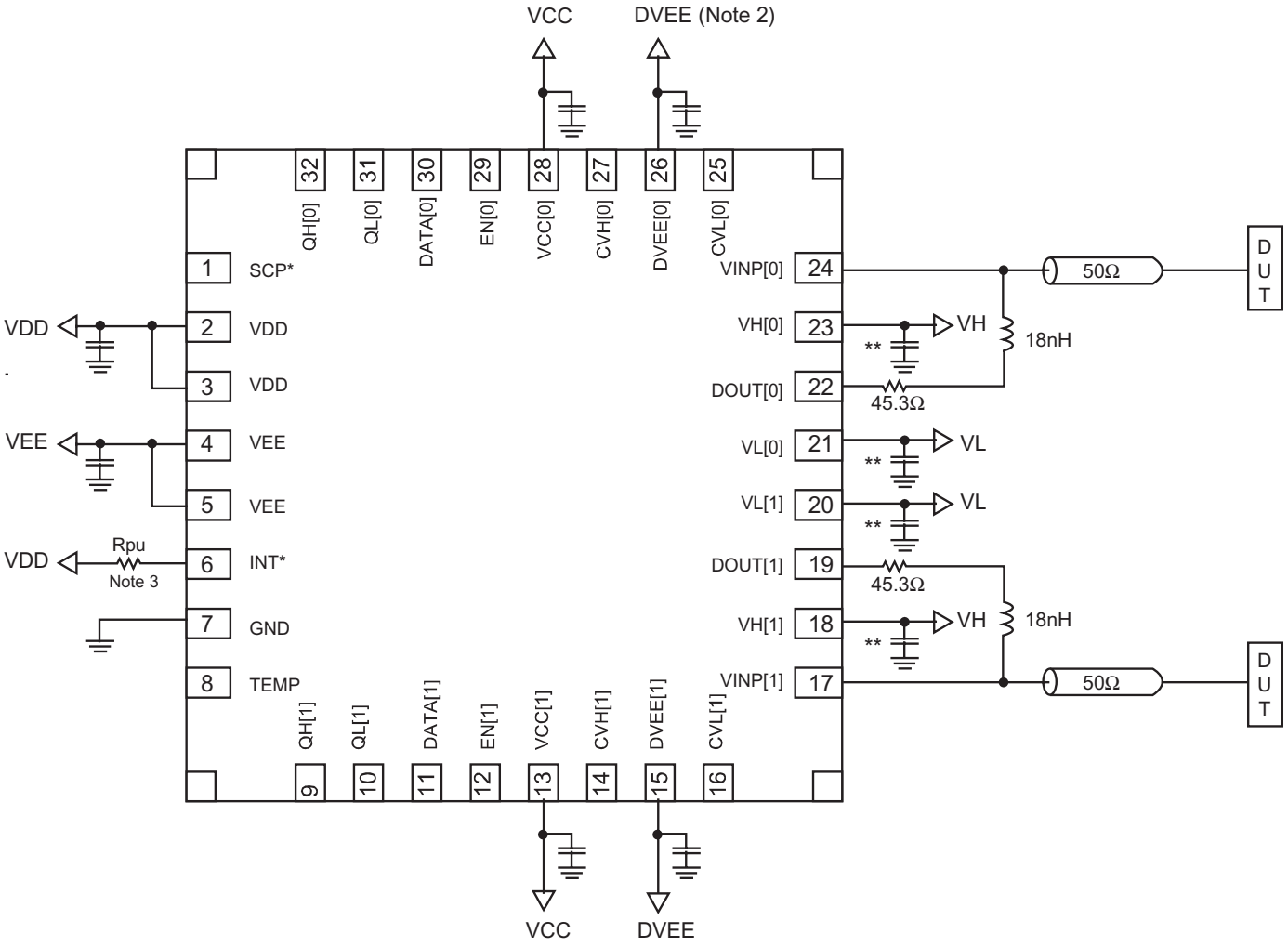
2) *Reactive Component:* Accounts for the reactive or "AC" component of the output impedance and is matched to a transmission line by using external inductors and/or capacitors. Using empirical methods in our lab, we have determined that an 18nH series inductor offers the best impedance matching for a 50Ω transmission line (see below).



External component connections are illustrated in the E7802 Hookup Diagram.

Application Information (continued)

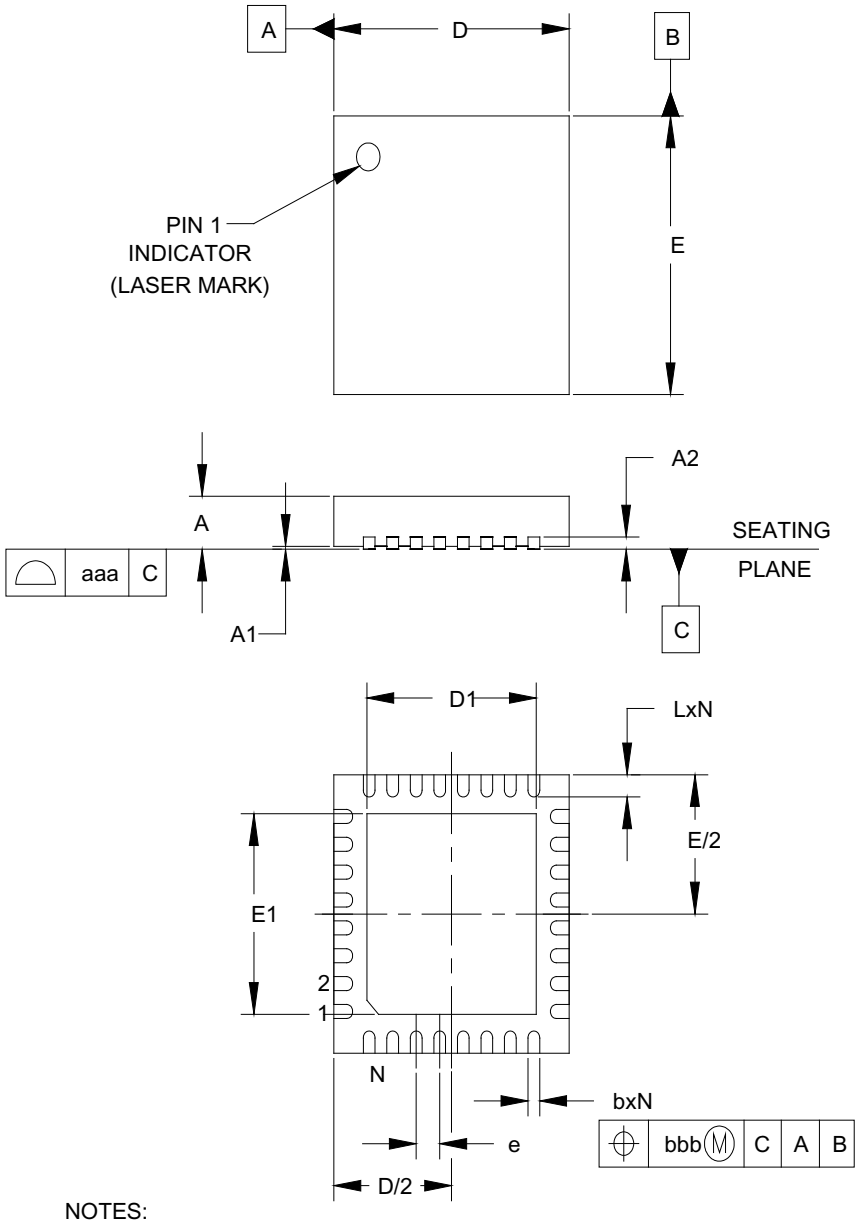
E7802 Hookup Diagram



Note 1: All capacitors are 0.1µF unless otherwise noted.
** See Applications Note PE-A1 for proper capacitor and VH/VL supply selection.
Note 2: DVEE supply can be connected to GND if DOUT does not need to swing below 0V.
Note 3: Choose Rpu such that the INT* current is less than 5mA.

Package Information

32-Pad
5mm x 5mm QFN
Package Outline



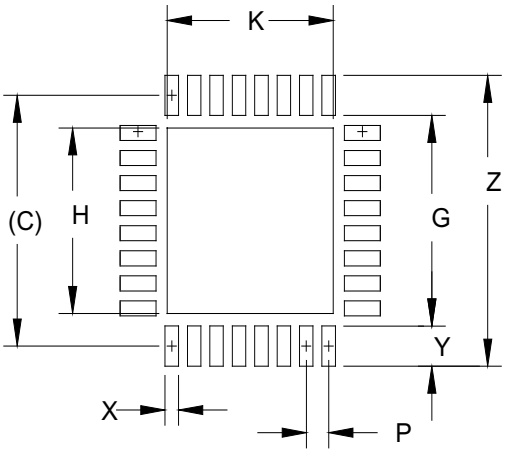
DIMENSIONS						
DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.031	-	.039	0.80	-	1.00
A1	.000	-	.002	0.00	-	0.05
A2	-	(.008)	-	-	(0.20)	-
b	.007	.010	.012	0.18	0.25	0.30
D	.193	.197	.201	4.90	5.00	5.10
D1	.130	.136	.140	3.30	3.45	3.55
E	.193	.197	.201	4.90	5.00	5.10
E1	.130	.136	.140	3.30	3.45	3.55
e	.020 BSC			0.50 BSC		
L	.012	.016	.020	0.30	0.40	0.50
N	32			32		
aaa	.003			0.08		
bbb	.004			0.10		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

Package Information (continued)

32-Pad
5mm x 5mm QFN
Land Pattern



DIMENSIONS		
DIM	INCHES	MILLIMETERS
C	(.197)	(5.00)
G	.165	4.20
H	.146	3.70
K	.146	3.70
P	.020	0.50
X	.012	0.30
Y	.031	0.80
Z	.228	5.80

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY.
   CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR
   COMPANY'S MANUFACTURING GUIDELINES ARE MET.
3. THERMAL VIAS IN THE LAND PATTERN OF THE EXPOSED PAD
   SHALL BE CONNECTED TO A SYSTEM GROUND PLANE.
   FAILURE TO DO SO MAY COMPROMISE THE THERMAL AND/OR
   FUNCTIONAL PERFORMANCE OF THE DEVICE.
4. SQUARE PACKAGE - DIMENSIONS APPLY IN BOTH " X " AND " Y " DIRECTIONS.

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units
Positive Analog Supply	VCC	-0.5	DVEE + 16	V
Negative Analog Supply	VEE	-6	+0.5	V
Negative Driver Supply	DVEE	VEE	+0.5	V
Digital Power Supply	VDD	-0.5	+6.0	V
Digital Input Voltages	EN[0:1], DATA[0:1], SCP*	-0.5	VDD + 0.5	V
Driver Pins	VH[0:1], VL[0:1], DOUT[0:1]	DVEE + 0.5	VCC + 0.5	V
Comparator Pins	CVH[0:1], CVL[0:1], VINP[0:1]	VEE - 0.5	VCC + 0.5	V
Storage Temperature	TS	-65	+150	°C
Junction Temperature	Tj		+150	°C
IR Reflow Conditions	Tpkg		+260	°C

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Positive Analog Supply	VCC	DVEE + 9	DVEE + 14.5	DVEE + 15	V
Negative Analog Supply	VEE	-5.25	-5	-4.75	V
Negative Driver Supply	DVEE	-3.6		0	V
Digital Power Supply	VDD	3.0		3.6	V
Thermal Resistance - Junction to Case	θjc				
Junction to Top-Center of Case			4		℃/W
Junction to Bottom-Center of Heat Slug			1		℃/W
Thermal Resistance - Junction to Ambient Still Air	θja		26		℃/W
Junction Temperature	TJ	25		100	℃

Stresses above those listed in "Absolute Maximum Ratings" section may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these, or any other conditions beyond those listed, is not implied. Exposure to absolute maximum conditions for extended periods may affect device reliability.

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Driver					
Driver "High Level" Range	VH	VL		VCC	V
Driver "Low Level" Range	VL				
10.4 V < VCC ≤ 15V		DVEE		VCC - 8.4	V
5.4V ≤ VCC ≤ 10.4V		DVEE		2	V
Driver Output Swing	DOUT	0.2		15	V
Driver Output Impedance	Rout				
VCC = 15V, Tj = 65℃ ± 3℃		4		8.5	Ω
Across Recommended Operating Conditions		2.5		11	Ω
Offset Voltage	|VH, VL - DOUT|		0.5	2.5	mV
Driver Digital Input Logic Levels (DATA, EN, SCP*)					
Logic Input "High" Level	VIH	2.0			V
Logic Input "Low" Level	VIL			0.8	V
Driver Digital Input Current					
DATA, EN	IIH, IIL	-200		+200	nA
SCP*	IIH, IIL	-1		0	mA
Hi-Z Leakage Current at DOUT (DVEE ≤ DOUT ≤ VCC)	ILEAK	-35		+75	nA
DC Output Current (Note 1)	IOUT(DC)	-200		+200	mA
AC Output Current (Note 2)	IOUT(AC)	±1.4		±3.6	A
Short Circuit Protection Threshold					
VL ≤ DOUT ≤ VH		205		300	mA
DVEE ≤ DOUT ≤ VCC		75		350	mA
INT* Output Low Voltage @ I_{INT}*=5mA	VOL			0.4	V
Comparator					
Analog Inputs					
CVH Input Voltage Range (Note 3)	VCVH	VCVL		VCC - 3	V
CVL Input Voltage Range (Note 3)	VCVL	VEE + 3		VCVH	V
CVH, CVL Input Current	IIN	-15		+15	µA
VINP Voltage Range	V_{VINP}	VEE + 2		VCC	V
VINP Input Current	I_{VINP}				
DVEE ≤ VINP ≤ VCC - 3V		-30		+30	µA
Across Full VINP Range		-200		+200	µA
Hysteresis	VHYS		30		mV
Offset Voltage	VOS	-50		+50	mV
Digital Outputs					
Output "High" Voltage @ +5 mA	VOH	2.4			V
Output "Low" Voltage @ -5 mA	VOL			0.4	V

Test conditions (unless otherwise specified): "Recommended Operating Conditions".

Note 1: DC output current is specified per individual driver, $V_{VL} \le V_{DOUT} \le V_{VH}$.

Note 2: Surge current capability with 1000pF lumped capacitive load on DOUT defined as the maximum output current during a 15V step.

Note 3: Comparator threshold inputs (CVH, CVL) can be overlapped (i.e. VCVH < VCVL), but comparator output logic will be inverted and functionality of the comparators is not guaranteed under this condition.

DC Characteristics (continued)

Parameter	Symbol	Min	Typ	Max	Units
Power Supply Current (Quiescent)					
Positive Supply Current	ICC	11	24	40	mA
Driver Negative Supply Current	IDEE	1.5	7	12	mA
Negative Supply Current	IEE	11	16	26	mA
Digital Supply Current	IDD	2	6	14	mA

AC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Driver (Note 1)					
Propagation Delay					
DATA to DOUT (Figure 5)	Tpd	13.6		15.6	ns
EN to DOUT (Active to HiZ) (Figure 7)	Tz	8		17	ns
EN to DOUT (HiZ to Active) (Figure 7)	Toe	8		14	ns
Propagation Delay Matching	|Tpd+ - Tpd-|			1	ns
Propagation Delay Tempco (ΔTj = 25°C to 100°C)	ΔTpd/ΔT			30	ps/°C
Driver Propagation Delay Dispersion vs. Amplitude (VL = 0, 0.2 < VH < 3.0)	ΔTpd(swing)			1	ns
Short Circuit Protection Activation Time					
Pulse Width for Trigger (VH=3V, VL=0V, DOUT Shorted to 0V)	Tprotect	125			ns
Short to Comparator Trigger	Tpd			600	ns
Short to INT* Trigger	T_{INT*}			600	ns
Rise/Fall Times (1000pF lumped capacitance at DOUT, Figure 5a)					
3V Programmed Swing (10% - 90%)	Tr/Tf		9.5	16	ns
5V Programmed Swing (10% - 90%)	Tr/Tf		10	16	ns
Rise/Fall Times (100pF Lumped Capacitance at DOUT, Figure 5a)					
0.4V Programmed Swing (20% - 80%) (Note 8)	Tr/Tf		2	4	ns
1V Programmed Swing (20% - 80%)	Tr/Tf		3	5	ns
3V Programmed Swing (10% - 90%)	Tr/Tf		3.5	5.5	ns
5V Programmed Swing (10% - 90%)	Tr/Tf		4	6.5	ns
Rise/Fall Times (50Ω termination, Figure 5b)					
0.4V Programmed Swing (20% - 80%) (Note 8)	Tr/Tf		2	4	ns
1V Programmed Swing (20% - 80%)	Tr/Tf		3	5	ns
3V Programmed Swing (10% - 90%)	Tr/Tf		3.5	5.5	ns
5V Programmed Swing (10% - 90%)	Tr/Tf		4	6.5	ns
Maximum Operating Frequency (50Ω termination, Figure 5b)	Fmax				
0.4V Programmed Swing (Note 8)		50			MHz
1V Programmed Swing		50			MHz
3V Programmed Swing		50			MHz
5V Programmed Swing		50			MHz
Maximum Operating Frequency (1KΩ termination, Figure 5c)	Fmax				
0.4V Programmed Swing (Note 8)		50			MHz
1V Programmed Swing		50			MHz
3V Programmed Swing		50			MHz
5V Programmed Swing		50			MHz
15V Programmed Swing		50			MHz
DOUT Capacitance	CDOUT		50		pF
Driver Overshoot/Preshoot/Undershoot (3V) (1KΩ termination, Figures 5c, 13, Note 6)	Vovershoot			100	mV
Minimum Pulse Width (Figures 5b, 9)	Mpw				
0.4V Programmed Swing (Note 8)				7	ns
1V Programmed Swing				7.5	ns
3V Programmed Swing				8	ns
5V Programmed Swing				9	ns

AC Characteristics (continued)

Parameter	Symbol	Min	Typ	Max	Units
Comparator (Note 2)					
Comparator Propagation Delay (Figure 10, Note 5)	Tpd +/-	3.5	5	6.5	ns
Propagation Delay Matching (Note 5)	|(Tpd+) - (Tpd-)|		0.5	1.5	ns
Propagation Delay Tempco (ΔTj = 25℃ to 100℃)	ΔTpd/ΔT		15	20	ps/℃
Propagation Delay Dispersion vs. Overdrive (Note 7) (Figure 11)	ΔTpd/Δ(VINP-VCH(L))				
100mV to 1V Overdrive			2.5	3.5	ns
1V to 2.5V Overdrive			0.25	0.5	ns
Propagation Delay Dispersion vs. Common Mode (Figure 12, Notes 3, 7)	ΔTpd(cm)			0.5	ns
Comparator Bandwidth (Note 4)	Fmax	100			MHz
Minimum Pulse Width				5	ns
VINP Capacitance	CVINP		3		pF

Note 1: Driver AC specifications are with Tj = 65°C ± 3°C, VCC = 15V, VDD = 3.3V, DVEE = 0V, VEE = -5V, VL = 0, VH = 3.0, into 20 inches of 50Ω transmission line unless otherwise noted.

Note 2: Tj = 65°C ± 3°C, CVH = 1.5, CVL = 1.5, VINP 0 - 3V @ 10MHz. VCC = 15V, VDD = 3.3V, DVEE = 0V, VEE = -5V unless otherwise noted.

Note 3: V_{VINP} = 5V pp, 0.5V ≤ $V_{CVH/L}$ ≤ 1.5V.

Note 4: Comparator bandwidth is the maximum frequency under which the comparator will switch with CVH/CVL = 1.5V, VINP = 0 to 3V.

Note 5: V_{VINP} = 5Vpp, VCVH,L = 2.5V.

Note 6: Measured with 33pF at end of transmission line. See "Optimizing Driver Waveforms" Section for characteristics with different capacitive loads.

Note 7: CVH, CVL are Calibrated Threshold Values (i.e., "Switching Point").

Note 8: VCC = 9V, DVEE = 0V, VEE = -5V.

Test Circuits:

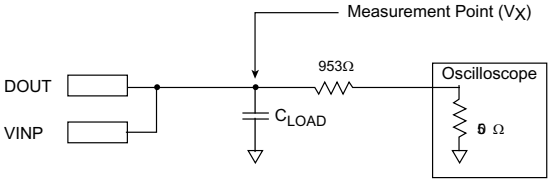


Figure 5a. Driver Output/Comparator Input, Lumped Load

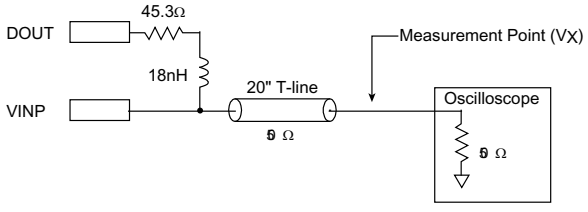


Figure 5b. Driver Output/Comparator Input, 50Ω Load

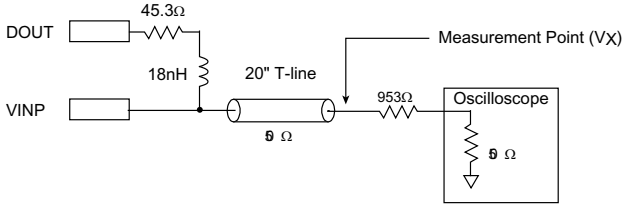


Figure 5c. Driver Output/Comparator Input, 1KΩ Load

AC Characteristics (continued)

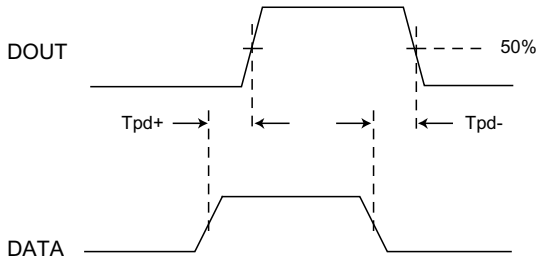
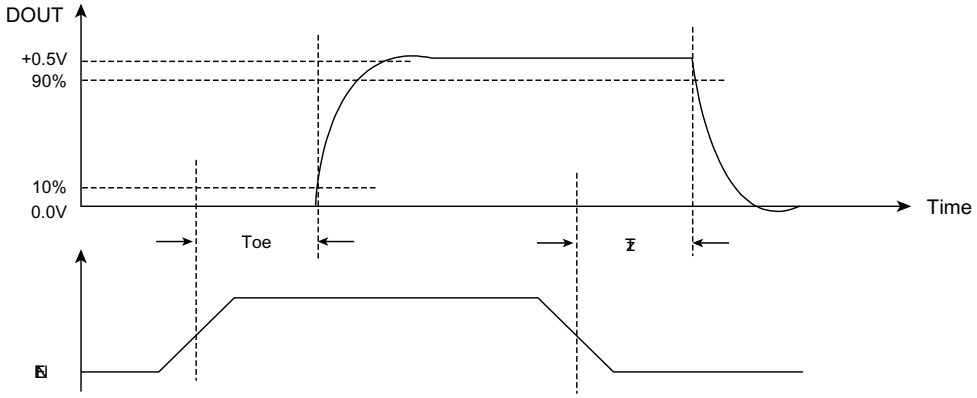


Figure 6. Driver Propagation Delay Measurements



Transmission line terminated 50Ω to ground.

Figure 7. Driver HiZ Enable/Disable Delay Measurement Definition

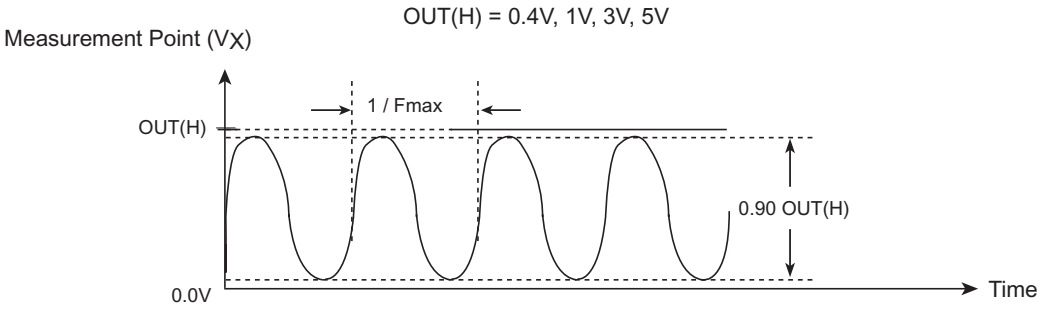


Figure 8. Driver Fmax Measurement Definition

AC Characteristics (continued)

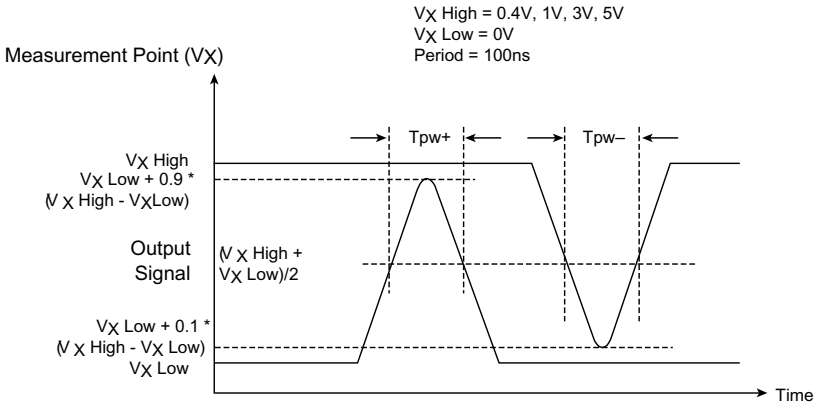


Figure 9. Driver Minimum Pulse Width Measurement Definition

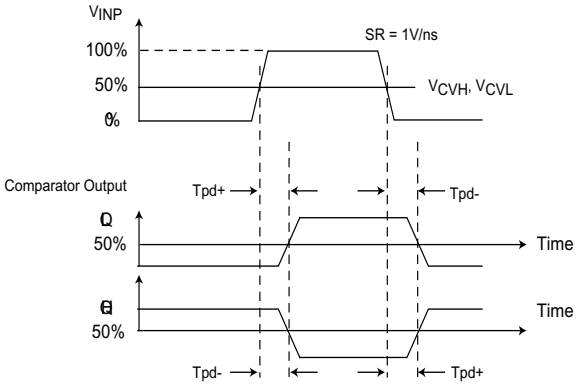


Figure 10. Comparator Propagation Delay Measurements

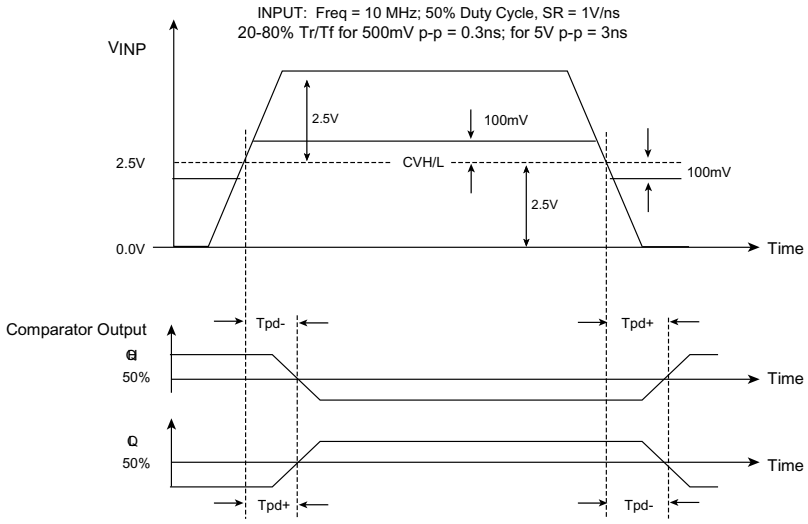


Figure 11. Comparator Dispersion: Overdrive Measurement Definition

AC Characteristics (continued)

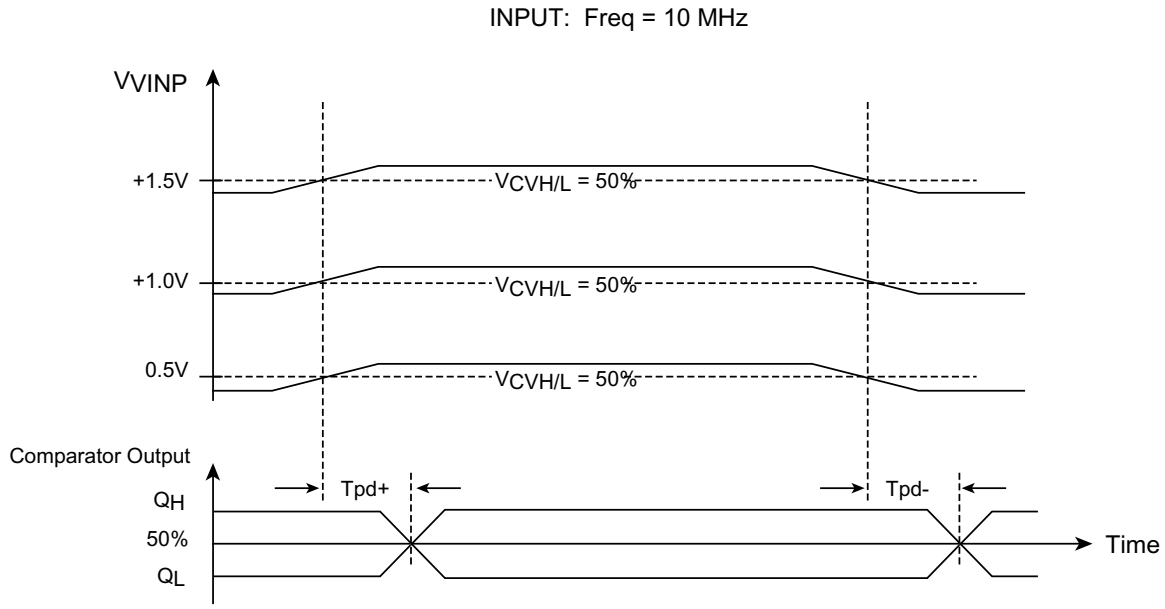


Figure 12. Comparator Dispersion: Common Mode Definition

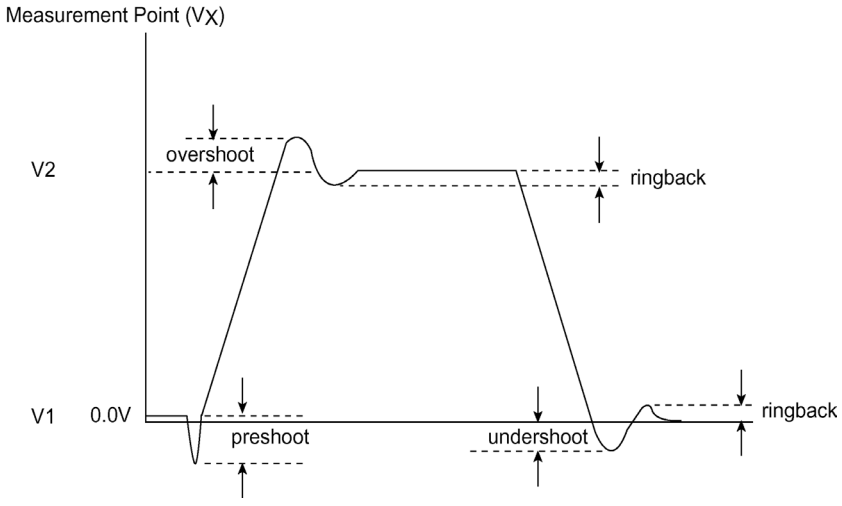


Figure 13. Driver Overshoot, Undershoot, and Ringback

Ordering Information

Model Number	Package
E7802ALPT	32-pad, 5mm x 5mm QFN
E7802ALPT-T	32-pad, 5mm x 5mm QFN (Tape & Reel)
EVM7802ALPT	E7802 Evaluation Board

Pb This product is lead-free.

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