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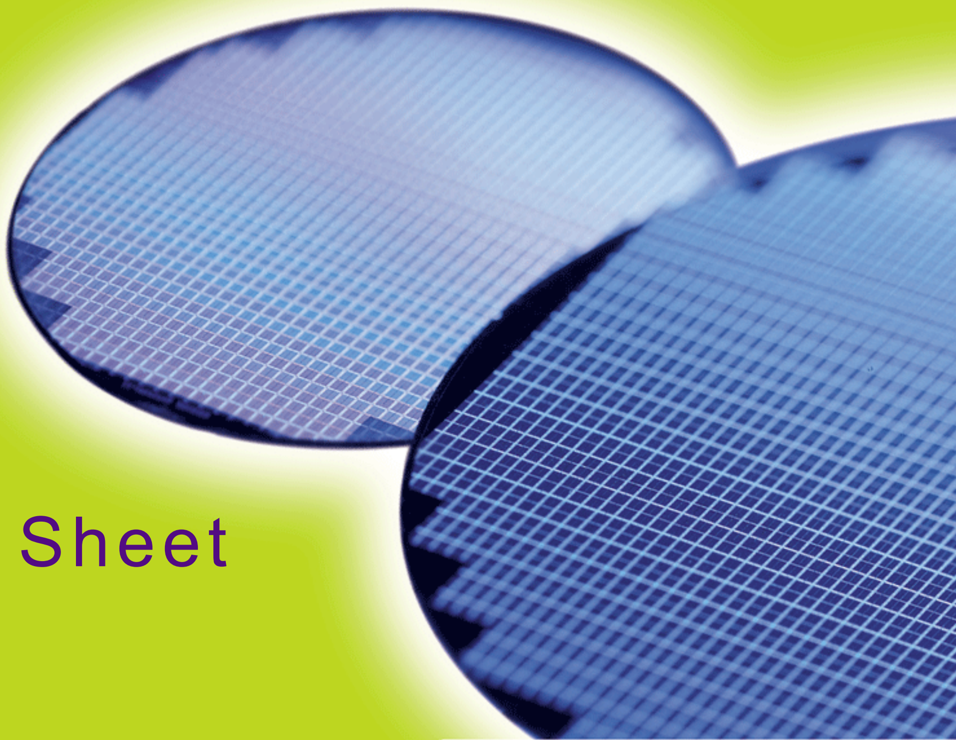
HYB25D512[40/80/16]0B[E/F](L)

512-Mbit Double-Data-Rate SDRAM
DDR SDRAM



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1 Overview

This chapter gives an overview of the 512-Mbit Double-Data-Rate SDRAM product family and describes its main characteristics

1.1 Features

- Double data rate architecture: two data transfers per clock cycle
- Bidirectional data strobe (DQS) is transmitted and received with data, to be used in capturing data at the receiver
- DQS is edge-aligned with data for reads and is center-aligned with data for writes
- Differential clock inputs (CK and $\overline{CK}$)
- Four internal banks for concurrent operation
- Data mask (DM) for write data
- DLL aligns DQ and DQS transitions with CK transitions
- Commands entered on each positive CK edge; data and data mask referenced to both edges of DQS
- Burst Lengths: 2, 4, or 8
- CAS Latency: (1.5), 2, 2.5, 3
- Auto Pre charge option for each burst access
- Auto Refresh and Self Refresh Modes
- RAS-lockout supported t_{RAP}=t_{RCD}
- 7.8 µs Maximum Average Periodic Refresh Interval
- 2.5 V (SSTL_2 compatible) I/O
- V_{DDQ} = 2.5 V ± 0.2 V and 2.6 V ± 0.1 V for DDR400
- V_{DD} = 2.5 V ± 0.2 V and 2.6 V ± 0.1 V for DDR400
- P-TFBGA-60 and P-TSOPII-66 package

TABLE 1
Performance

Part Number Speed Code			–5	–6	–7	Unit
Speed Grade	Component		DDR400B	DDR333B	DDR266A	—
	Module		PC3200–3033	PC2700–2533	PC2100–2033	—
max. Clock Frequency	@CL3	f_{CK3}	200	166	–	MHz
	@CL2.5	$f_{CK2.5}$	166	166	143	MHz
	@CL2	f_{CK2}	133	133	133	MHz

1.2 Description

The 512-Mbit Double-Data-Rate SDRAM is a high-speed CMOS, dynamic random-access memory containing 536,870,912 bits. It is internally configured as a quad-bank DRAM.

The 512-Mbit Double-Data-Rate SDRAM uses a double-data-rate architecture to achieve high-speed operation. The double data rate architecture is essentially a 2n pre fetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the 512-Mbit Double-Data-Rate SDRAM effectively consists of a single 2n-bit wide, one clock cycle data transfer at the internal DRAM core and two corresponding n-bit wide, one-half-clock-cycle data transfers at the I/O pins.

A bidirectional data strobe (DQS) is transmitted externally, along with data, for use in data capture at the receiver. DQS is a strobe transmitted by the DDR SDRAM during Reads and by the memory controller during Writes. DQS is edge-aligned with data for Reads and center-aligned with data for Writes.

The 512-Mbit Double-Data-Rate SDRAM operates from a differential clock (CK and $\overline{CK}$; the crossing of CK going HIGH and $\overline{CK}$ going LOW is referred to as the positive edge of CK). Commands (address and control signals) are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CK.

Read and write accesses to the DDR SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an Active command, which is then followed by a Read or Write command. The address bits registered coincident with the Active command are used to select the bank and row to be accessed. The address bits registered coincident with the Read or Write command are used to select the bank and the starting column location for the burst access.

The DDR SDRAM provides for programmable Read or Write burst lengths of 2, 4 or 8 locations. An Auto Precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst access.

As with standard SDRAMs, the pipelined, multibank architecture of DDR SDRAMs allows for concurrent operation, thereby providing high effective bandwidth by hiding row precharge and activation time.

An auto refresh mode is provided along with a power-saving power-down mode. All inputs are compatible with the JEDEC Standard for SSTL_2. All outputs are SSTL_2, Class II compatible.

Note: The functionality described and the timing specifications included in this data sheet are for the DLL Enabled mode of operation.

TABLE 2
Ordering Information

Part Number[1)]	Org.	CAS-RCD-RP Latencies	Clock (MHz)	CAS-RCD-RP Latencies	Clock (MHz)	Speed	Package
HYB25D512800BT–5	×8	3.0-3-3	200	2.5-3-3	166	DDR400B	P-TSOPII-66
HYB25D512160BT–5	×16						
HYB25D512400BT–6	×4	2.5-3-3	166	2-3-3	133	DDR333	
HYB25D512800BT–6	×8						
HYB25D512160BT–6	×16						
HYB25D512160BTL–6	×16						
HYB25D512400BT–7	×4		143			DDR266	
HYB25D512400BC–5	×4	3.0-3-3	200	2.5-3-3	166	DDR400B	P-TFBGA-60
HYB25D512800BC–5	×8						
HYB25D512160BC–5	×16						
HYB25D512400BC–6	×4	2.5-3-3	166	2-3-3	133	DDR333	
HYB25D512800BC–6	×8						
HYB25D512160BC–6	×16						

1) HYB: designator for memory components
25D: DDR SDRAMs at V_{DDQ} = 2.5 V
512: 512-Mbit density
400/800/160: Product variations x4, ×8 and ×16
B: Die revision B
C/F/E/T: Package type FBGA and TSOP
L: Low power (on request)

green Product

TABLE 3
Ordering Information for RoHS compliant products

Part Number	Org.	CAS-RCD-RP Latencies	Clock (MHz)	CAS-RCD-RP Latencies	Clock (MHz)	Speed	Package
HYB25D512400BF–5	×4	3.0-3-3	200	2.5-3-3	166	DDR400B	P-TFBGA-60
HYB25D512800BF–5	×8						
HYB25D512160BF–5	×16						
HYB25D512400BF–6	×4	2.5-3-3	166	2-3-3	133	DDR333	
HYB25D512800BF–6	×8						
HYB25D512160BF–6	×16						
HYB25D512400BE–5	×4	3.0-3-3	200	2.5-3-3	166	DDR400B	P-TSOPII-66
HYB25D512800BE–5	×8						
HYB25D512160BE–5	×16						
HYB25D512400BE–6	×4	2.5-3-3	166	2-3-3	133	DDR333	
HYB25D512800BE–6	×8						
HYB25D512800BEL–6	×8						
HYB25D512160BE–6	×16						
HYB25D512160BEL–6	×16						
HYB25D512400BE–7	×4		143			DDR266A	

2 Pin Configuration

The pin configuration of a DDR SDRAM is listed by function in **Table 4** (60 pins). The abbreviations used in the Pin#/Buffer# column are explained in **Table 5** and **Table 6** respectively. The pin numbering for FBGA is depicted in **Figure 1** and that of the TSOP package in **Figure 2**

TABLE 4
Pin Configuration of DDR SDRAM

Ball#/Pin#	Name	Pin Type	Buffer Type	Function
Clock Signals				
G2, 45	CK	I	SSTL	**Clock Signal**
G3, 46	$\overline{CK}$	I	SSTL	**Complementary Clock Signal**
H3, 44	CKE	I	SSTL	**Clock Enable**
Control Signals				
H7, 23	$\overline{RAS}$	I	SSTL	**Row Address Strobe**
G8, 22	$\overline{CAS}$	I	SSTL	**Column Address Strobe**
G7, 21	$\overline{WE}$	I	SSTL	**Write Enable**
H8, 24	$\overline{CS}$	I	SSTL	**Chip Select**
Address Signals				
J8, 26	BA0	I	SSTL	**Bank Address Bus 2:0**
J7, 27	BA1	I	SSTL	
K7, 29	A0	I	SSTL	**Address Bus 11:0**
L8, 30	A1	I	SSTL	
L7, 31	A2	I	SSTL	
M8, 32	A3	I	SSTL	
M2, 35	A4	I	SSTL	
L3, 36	A5	I	SSTL	
L2, 37	A6	I	SSTL	
K3, 38	A7	I	SSTL	
K2, 39	A8	I	SSTL	
J3, 40	A9	I	SSTL	
K8, 28	A10	I	SSTL	
	AP	I	SSTL	
J2, 41	A11	I	SSTL	
H2, 42	A12	I	SSTL	**Address Signal 12** *Note: 256 Mbit or larger dies*
	NC	NC	—	*Note: 128 Mbit or smaller dies*
F9, 17	A13	I	SSTL	**Address Signal 13** *Note: 1 Gbit based dies*
	NC	NC	—	*Note: 512 Mbit or smaller dies*

Ball#/Pin#	Name	Pin Type	Buffer Type	Function
Data Signals ×4 organization				
B7, 5	DQ0	I/O	SSTL	**Data Signal 3:0**
D7, 11	DQ1	I/O	SSTL	
D3, 56	DQ2	I/O	SSTL	
B3, 62	DQ3	I/O	SSTL	
Data Strobe ×4 organisation				
E3, 51	DQS	I/O	SSTL	**Data Strobe**
Data Mask ×4 organization				
F3, 47	DM	I	SSTL	**Data Mask**
Data Signals ×8 organization				
A8, 2	DQ0	I/O	SSTL	Data Signal 7:0
B7, 5	DQ1	I/O	SSTL	
C7, 8	DQ2	I/O	SSTL	
D7, 11	DQ3	I/O	SSTL	
D3, 56	DQ4	I/O	SSTL	
C3, 59	DQ5	I/O	SSTL	Data Signal
B3, 62	DQ6	I/O	SSTL	
A2, 65	DQ7	I/O	SSTL	
Data Strobe ×8 organisation				
E3, 51	DQS	I/O	SSTL	**Data Strobe**
Data Mask ×8 organization				
F3, 47	DM	I	SSTL	**Data Mask**
Data Signals ×16 organization				
A8, 2	DQ0	I/O	SSTL	Data Signal 15:0
B9, 4	DQ1	I/O	SSTL	
B7, 5	DQ2	I/O	SSTL	
C9, 7	DQ3	I/O	SSTL	
C7, 8	DQ4	I/O	SSTL	
D9, 10	DQ5	I/O	SSTL	
D7, 11	DQ6	I/O	SSTL	
E9, 13	DQ7	I/O	SSTL	
E1, 54	DQ8	I/O	SSTL	
D3, 56	DQ9	I/O	SSTL	
D1, 57	DQ10	I/O	SSTL	
C3, 59	DQ11	I/O	SSTL	
C1, 60	DQ12	I/O	SSTL	
B3, 62	DQ13	I/O	SSTL	
B1, 63	DQ14	I/O	SSTL	
A2, 65	DQ15	I/O	SSTL	

Ball#/Pin#	Name	Pin Type	Buffer Type	Function
Data Strobe ×16 organization				
E3, 51	UDQS	I/O	SSTL	**Data Strobe Upper Byte**
E7, 16	LDQS	I/O	SSTL	**Data Strobe Lower Byte**
Data Mask ×16 organization				
F3, 47	UDM	I	SSTL	**Data Mask Upper Byte**
F7, 20	LDM	I	SSTL	**Data Mask Lower Byte**
Power Supplies				
F1, 49	V_{REF}	AI	—	**I/O Reference Voltage**
A9, B2, C8, D2, E8, 3, 9, 15, 55, 61	V_{DDQ}	PWR	—	**I/O Driver Power Supply**
A7, F8, M7, 1, 18, 33	V_{DD}	PWR	—	**Power Supply**
A1, B8, C2, D8, E2, 6, 12, 52, 58, 64	V_{SSQ}	PWR	—	**Power Supply**
A3,F2, M3, 34, 48, 66,	V_{SS}	PWR	—	**Power Supply**
Not Connected				
A2, 65	NC	NC	—	Not Connected *Note: ×4 organization*
A8, 2	NC	NC	—	Not Connected *Note: ×4 organization*
B1, 63	NC	NC	—	Not Connected *Note: ×8 and ×4 organisation*
B9, 4	NC	NC	—	Not Connected *Note: ×8 and ×4 organization*
C1, 60	NC	NC	—	Not Connected *Note: ×8 and ×4 organization*
C3, 59	NC	NC	—	Not Connected *Note: ×4 organization*
C7, 8	NC	NC	—	Not Connected *Note: ×4 organization*
C9, 7	NC	NC	—	Not Connected *Note: ×8 and ×4 organization*
D1, 57	NC	NC	—	Not Connected *Note: ×8 and ×4 organization*
D9, 10	NC	NC	—	Not Connected *Note: ×8 and ×4 organization*
E1, 54	NC	NC	—	Not Connected *Note: ×8 and ×4 organization*

Ball#/Pin#	Name	Pin Type	Buffer Type	Function
E7, 16	NC	NC	—	Not Connected *Note: ×8 and ×4 organization*
E9, 13	NC	NC	—	Not Connected *Note: ×8 and ×4 organization*
F7, 20	NC	NC	—	Not Connected *Note: ×8 and ×4 organization*
F9, 14, 17, 19, 25,43, 50, 53	NC	NC	—	Not Connected *Note: ×16, ×8 and ×4 organization*

TABLE 5
Abbreviations for Pin Type

Abbreviation	Description
I	Standard input-only pin. Digital levels.
O	Output. Digital levels.
I/O	I/O is a bidirectional input/output signal.
AI	Input. Analog levels.
PWR	Power
GND	Ground
NC	Not Connected

TABLE 6
Abbreviations for Buffer Type

Abbreviation	Description
SSTL	Serial Stub Terminated Logic (SSTL2)
LV-CMOS	Low Voltage CMOS
CMOS	CMOS Levels
OD	Open Drain. The corresponding pin has 2 operational states, active low and tristate, and allows multiple devices to share as a wire-OR.

FIGURE 1

Pin Configuration P-TFBGA-60 Top View, see the balls throught the package

(x4)

	1	2	3	4	5	6	7	8	9
A	V_{SSQ}	N.C.	V_{SS}				V_{DD}	N.C.	V_{DDQ}
B	N.C.	V_{DDQ}	DQ3				DQ0	V_{SSQ}	N.C.
C	N.C.	V_{SSQ}	N.C.				N.C.	V_{DDQ}	N.C.
D	N.C.	V_{DDQ}	DQ2				DQ1	V_{SSQ}	N.C.
E	N.C.	V_{SSQ}	DQS				N.C.	V_{DDQ}	N.C.
F	V_{REF}	V_{SS}	DM				N.C.	V_{DD}	NC,A13
G		CK	$\overline{CK}$				$\overline{WE}$	$\overline{CAS}$	
H		NC,A12	CKE				$\overline{RAS}$	$\overline{CS}$	
J		A11	A9				BA1	BA0	
K		A8	A7				A0	A10/AP	
L		A6	A5				A2	A1	
M		A4	V_{SS}				V_{DD}	A3	

(x8)

	1	2	3	4	5	6	7	8	9
A	V_{SSQ}	DQ7	V_{SS}				V_{DD}	DQ0	V_{DDQ}
B	N.C.	V_{DDQ}	DQ6				DQ1	V_{SSQ}	N.C.
C	N.C.	V_{SSQ}	DQ5				DQ2	V_{DDQ}	N.C.
D	N.C.	V_{DDQ}	DQ4				DQ3	V_{SSQ}	N.C.
E	N.C.	V_{SSQ}	DQS				N.C.	V_{DDQ}	N.C.
F	V_{REF}	V_{SS}	DM				N.C.	V_{DD}	NC,A13
G		CK	$\overline{CK}$				$\overline{WE}$	$\overline{CAS}$	
H		NC,A12	CKE				$\overline{RAS}$	$\overline{CS}$	
J		A11	A9				BA1	BA0	
K		A8	A7				A0	A10/AP	
L		A6	A5				A2	A1	
M		A4	V_{SS}				V_{DD}	A3	

(x16)

	1	2	3	4	5	6	7	8	9
A	V_{SSQ}	DQ15	V_{SS}				V_{DD}	DQ0	V_{DDQ}
B	DQ14	V_{DDQ}	DQ13				DQ2	V_{SSQ}	DQ1
C	DQ12	V_{SSQ}	DQ11				DQ4	V_{DDQ}	DQ3
D	DQ10	V_{DDQ}	DQ9				DQ6	V_{SSQ}	DQ5
E	DQ8	V_{SSQ}	UDQS				LDQS	V_{DDQ}	DQ7
F	V_{REF}	V_{SS}	UDM				LDM	V_{DD}	NC,A13
G		CK	$\overline{CK}$				$\overline{WE}$	$\overline{CAS}$	
H		NC,A12	CKE				$\overline{RAS}$	$\overline{CS}$	
J		A11	A9				BA1	BA0	
K		A8	A7				A0	A10/AP	
L		A6	A5				A2	A1	
M		A4	V_{SS}				V_{DD}	A3	

MPPD0060

FIGURE 2
Pin Configuration P-TSOPII-66-1

x4	x8	x16	Pin	Pin	x16	x8	x4
V_{DD}	V_{DD}	V_{DD}	1	66	V_{SS}	V_{SS}	V_{SS}
N.C.	DQ0	DQ0	2	65	DQ15	DQ7	N.C.
V_{DDQ}	V_{DDQ}	V_{DDQ}	3	64	V_{SSQ}	V_{SSQ}	V_{SSQ}
N.C.	N.C.	DQ1	4	63	DQ14	N.C.	N.C.
DQ0	DQ1	DQ2	5	62	DQ13	DQ6	DQ3
V_{SSQ}	V_{SSQ}	V_{SSQ}	6	61	V_{DDQ}	V_{DDQ}	V_{DDQ}
N.C.	N.C.	DQ3	7	60	DQ12	N.C.	N.C.
N.C.	DQ2	DQ4	8	59	DQ11	DQ5	N.C.
V_{DDQ}	V_{DDQ}	V_{DDQ}	9	58	V_{SSQ}	V_{SSQ}	V_{SSQ}
N.C.	N.C.	DQ5	10	57	DQ10	N.C.	N.C.
DQ1	DQ3	DQ6	11	56	DQ9	DQ4	DQ2
V_{SSQ}	V_{SSQ}	V_{SSQ}	12	55	V_{DDQ}	V_{DDQ}	V_{DDQ}
N.C.	N.C.	DQ7	13	54	DQ8	N.C.	N.C.
N.C.	N.C.	N.C.	14	53	N.C.	N.C.	N.C.
V_{DDQ}	V_{DDQ}	V_{DDQ}	15	52	V_{SSQ}	V_{SSQ}	V_{SSQ}
N.C.	N.C.	LDQS	16	51	UDQS	DQS	DQS
N.C.,A13	N.C.,A13	N.C.,A13	17	50	N.C.	N.C.	N.C.
V_{DD}	V_{DD}	V_{DD}	18	49	V_{REF}	V_{REF}	V_{REF}
N.C.	N.C.	N.C.	19	48	V_{SS}	V_{SS}	V_{SS}
N.C.	N.C.	LDM	20	47	UDM	DM	DM
$\overline{WE}$	$\overline{WE}$	$\overline{WE}$	21	46	$\overline{CK}$	$\overline{CK}$	$\overline{CK}$
$\overline{CAS}$	$\overline{CAS}$	$\overline{CAS}$	22	45	CK	CK	CK
$\overline{RAS}$	$\overline{RAS}$	$\overline{RAS}$	23	44	CKE	CKE	CKE
$\overline{CS0}$	$\overline{CS0}$	$\overline{CS0}$	24	43	N.C.	N.C.	N.C.
N.C.,$\overline{CS1}$	N.C.,$\overline{CS1}$	N.C.,$\overline{CS1}$	25	42	N.C.,A12	N.C.,A12	N.C.,A12
BA0	BA0	BA0	26	41	A11	A11	A11
BA1	BA1	BA1	27	40	A9	A9	A9
A10/AP	A10/AP	A10/AP	28	39	A8	A8	A8
A0	A0	A0	29	38	A7	A7	A7
A1	A1	A1	30	37	A6	A6	A6
A2	A2	A2	31	36	A5	A5	A5
A3	A3	A3	32	35	A4	A4	A4
V_{DD}	V_{DD}	V_{DD}	33	34	V_{SS}	V_{SS}	V_{SS}

MPPD0072

3 Functional Description

The 512-Mbit Double-Data-Rate SDRAM is a high-speed CMOS, dynamic random-access memory containing 536,870,912 bits. The 512-Mbit Double-Data-Rate SDRAM is internally configured as a quad-bank DRAM.

The 512-Mbit Double-Data-Rate SDRAM uses a double-data-rate architecture to achieve high-speed operation. The double-data-rate architecture is essentially a 2n pre fetch architecture, with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the 512-Mbit Double-Data-Rate SDRAM consists of a single 2n-bit wide, one clock cycle data transfer at the internal DRAM core and two corresponding n-bit wide, one-half clock cycle data transfers at the I/O pins.

Read and write accesses to the DDR SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an Active command, which is then followed by a Read or Write command. The address bits registered coincident with the Active command are used to select the bank and row to be accessed (BA0, BA1 select the bank; A0-A12 select the row). The address bits registered coincident with the Read or Write command are used to select the starting column location for the burst access.

Prior to normal operation, the DDR SDRAM must be initialized. The following sections provide detailed information covering device initialization, register definition, command descriptions and device operation.

BA1	BA0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	0	Operating MODE						CL			BT	BL		
reg. addr		w						w			w	w		

TABLE 7
Mode Register Definition

Field	Bits	Type	Description
BL	[2:0]	w	**Burst Length** Number of sequential bits per DQ related to one read/write command. *Note: All other bit combinations are RESERVED.* 001_B **2** 010_B **4** 011_B **8**
BT	3	w	**Burst Type** See **Table 8** for internal address sequence of low order address bits. 0_B **Sequential** 1_B **Interleaved**
CL	[6:4]	w	**CAS Latency** Number of full clocks from read command to first data valid window. *Note: All other bit combinations are RESERVED.* 010_B **2** 011_B **3** 101_B **(1.5 Optional, not covered by this data sheet)** 110_B **2.5**
MODE	[12:7]	w	**Operating Mode** *Note: All other bit combinations are RESERVED.* 000000_B **Normal Operation without DLL Reset** 000010_B **DLL Reset**

TABLE 8
Burst Definition

Burst Length	Starting Column Address			Order of Accesses Within a Burst	
	A2	A1	A0	Type = Sequential	Type = Interleaved
2			0	0-1	0-1
			1	1-0	1-0
4		0	0	0-1-2-3	0-1-2-3
		0	1	1-2-3-0	1-0-3-2
		1	0	2-3-0-1	2-3-0-1
		1	1	3-0-1-2	3-2-1-0
8	0	0	0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0	0	1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0	1	0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	0	1	1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1	0	0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1	0	1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1	1	0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	1	1	1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0

Notes

1. *For a burst length of two, A1-Ai selects the two-data-element block; A0 selects the first access within the block.*
2. *For a burst length of four, A2-Ai selects the four-data-element block; A0-A1 selects the first access within the block.*
3. *For a burst length of eight, A3-Ai selects the eight-data- element block; A0-A2 selects the first access within the block.*
4. *Whenever a boundary of the block is reached within a given sequence above, the following access wraps within the block.*

BA1	BA0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	1	MODE											DS	DLL

TABLE 9
Extended Mode Register Definition

Field	Bits	Type	Description
DLL	0	w	**DLL Status** 0_B **Enabled** 1_B **Disabled**
DS	1	w	**Drive Strength** 0_B **Normal** 1_B **Weak**
MODE	[12:2]	w	**Operating Mode** *Note: All other bit combinations are RESERVED.* 0_B **Normal Operation**

TABLE 10
Truth Table 1a: Commands

Name (Function)	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	MNE	Note
Deselect (NOP)	H	X	X	X	X	NOP	1)2)
No Operation (NOP)	L	H	H	H	X	NOP	1)2)
Active (Select Bank And Activate Row)	L	L	H	H	Bank/Row	ACT	1)3)
Read (Select Bank And Column, And Start Read Burst)	L	H	L	H	Bank/Col	Read	1)4)
Write (Select Bank And Column, And Start Write Burst)	L	H	L	L	Bank/Col	Write	1)4)
Burst Terminate	L	H	H	L	X	BST	1)5)
Precharge (Deactivate Row In Bank Or Banks)	L	L	H	L	Code	PRE	1)6)
Auto Refresh Or Self Refresh (Enter Self Refresh Mode)	L	L	L	H	X	AR/SR	1)7)8)
Mode Register Set	L	L	L	L	Op-Code	MRS	1)9)

1) CKE is HIGH for all commands shown except Self Refresh.
   V_{REF} must be maintained during Self Refresh operation
2) Deselect and NOP are functionally interchangeable.
3) BA0-BA1 provide bank address and A0-A12 provide row address.
4) BA0, BA1 provide bank address; A0-Ai provide column address (where i = 8 for ×16, i = 9 for ×8 and 9, 11 for ×4);
   A10 HIGH enables the Auto Precharge feature (non persistent), A10 LOW disables the Auto Precharge feature.
5) Applies only to read bursts with Auto Precharge disabled; this command is undefined (and should not be used) for read bursts with Auto Precharge enabled or for write bursts.
6) A10 LOW: BA0, BA1 determine which bank is precharged.
   A10 HIGH: all banks are precharged and BA0, BA1 are “Don’t Care”.
7) This command is AUTO REFRESH if CKE is HIGH; Self Refresh if CKE is LOW.
8) Internal refresh counter controls row and bank addressing; all inputs and I/Os are “Don’t Care” except for CKE.
9) BA0, BA1 select either the Base or the Extended Mode Register (BA0 = 0, BA1 = 0 selects Mode Register; BA0 = 1, BA1 = 0 selects Extended Mode Register; other combinations of BA0-BA1 are reserved; A0-A12 provide the op-code to be written to the selected Mode Register).

TABLE 11
Truth Table 1b: DM Operation

Name (Function)	DM	DQs	Note
Write Enable	L	Valid	1)
Write Inhibit	H	X	1)

1) Used to mask write data; provided coincident with the corresponding data.

TABLE 12
Truth Table 2: Clock Enable (CKE)

Current State	CKE n-1	CKEn	Command n	Action n	Note
	Previous Cycle	Current Cycle			
Self Refresh	L	L	X	Maintain Self-Refresh	1)
Self Refresh	L	H	Deselect or NOP	Exit Self-Refresh	2)
Power Down	L	L	X	Maintain Power-Down	–
Power Down	L	H	Deselect or NOP	Exit Power-Down	–
All Banks Idle	H	L	Deselect or NOP	Precharge Power-Down Entry	–
All Banks Idle	H	L	AUTO REFRESH	Self Refresh Entry	–
Bank(s) Active	H	L	Deselect or NOP	Active Power-Down Entry	–
	H	H	See **Table 13**	–	–

1) V_{REF} must be maintained during Self Refresh operation
2) Deselect or NOP commands should be issued on any clock edges occurring during the Self Refresh Exit (t_{XSNR}) period. A minimum of 200 clock cycles are needed before applying a read command to allow the DLL to lock to the input clock.

Notes

1. *CKEn is the logic state of CKE at clock edge n: CKE n-1 was the state of CKE at the previous clock edge.*
2. *Current state is the state of the DDR SDRAM immediately prior to clock edge n.*
3. *COMMAND n is the command registered at clock edge n, and ACTION n is a result of COMMAND n.*
4. *All states and sequences not shown are illegal or reserved.*

TABLE 13
Truth Table 3: Current State Bank n - Command to Bank n (same bank)

Current State	$\overline{\text{CS}}$	$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{WE}}$	Command	Action	Note
Any	H	X	X	X	Deselect	NOP. Continue previous operation.	1)2)3)4)5)6)
	L	H	H	H	No Operation	NOP. Continue previous operation.	1) to 6)
Idle	L	L	H	H	Active	Select and activate row	1) to 6)
	L	L	L	H	AUTO REFRESH	–	1) to 7)
	L	L	L	L	MODE REGISTER SET	–	1) to 7)
Row Active	L	H	L	H	Read	Select column and start Read burst	1) to 6), 8)
	L	H	L	L	Write	Select column and start Write burst	1) to 6), 8)
	L	L	H	L	Precharge	Deactivate row in bank(s)	1) to 6), 9)
Read (Auto Precharge Disabled)	L	H	L	H	Read	Select column and start new Read burst	1) to 6), 8)
	L	L	H	L	Precharge	Truncate Read burst, start Precharge	1) to 6), 9)
	L	H	H	L	BURST TERMINATE	BURST TERMINATE	1) to 6), 10)
Write (Auto Precharge Disabled)	L	H	L	H	Read	Select column and start Read burst	1) to 6), 8), 11)
	L	H	L	L	Write	Select column and start Write burst	1) to 6), 8)
	L	L	H	L	Precharge	Truncate Write burst, start Precharge	1) to 6), 9), 11)

1) This table applies when CKE n-1 was HIGH and CKE n is HIGH (see **Table 12** and after t_{XSNR}/t_{XSRD} has been met (if the previous state was self refresh).
2) This table is bank-specific, except where noted, i.e., the current state is for a specific bank and the commands shown are those allowed to be issued to that bank when in that state. Exceptions are covered in the notes below.
3) Current state definitions:
Idle: The bank has been precharged, and t_{RP} has been met.
Row Active: A row in the bank has been activated, and t_{RCD} has been met. No data bursts/accesses and no register accesses are in progress.
Read: A Read burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.
Write: A Write burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.
4) The following states must not be interrupted by a command issued to the same bank.
Pre charging: Starts with registration of a Precharge command and ends when t_{RP} is met. Once t_{RP} is met, the bank is in the idle state.
Row Activating: Starts with registration of an Active command and ends when t_{RCD} is met. Once t_{RCD} is met, the bank is in the “row active” state.
Read w/Auto Precharge Enabled: Starts with registration of a Read command with Auto Precharge enabled and ends when t_{RP} has been met. Once t_{RP} is met, the bank is in the idle state.
Write w/Auto Precharge Enabled: Starts with registration of a Write command with Auto Precharge enabled and ends when t_{RP} has been met. Once t_{RP} is met, the bank is in the idle state.
Deselect or NOP commands, or allowable commands to the other bank should be issued on any clock edge occurring during these states. Allowable commands to the other bank are determined by its current state and according to **Table 14**.
5) The following states must not be interrupted by any executable command; Deselect or NOP commands must be applied on each positive clock edge during these states.
Refreshing: Starts with registration of an Auto Refresh command and ends when t_{RFC} is met. Once t_{RFC} is met, the DDR SDRAM is in the “all banks idle” state.
Accessing Mode Register: Starts with registration of a Mode Register Set command and ends when t_{MRD} has been met. Once t_{MRD} is met, the DDR SDRAM is in the “all banks idle” state.
Pre charging All: Starts with registration of a Precharge All command and ends when t_{RP} is met. Once t_{RP} is met, all banks is in the idle state.
6) All states and sequences not shown are illegal or reserved.
7) Not bank-specific; requires that all banks are idle.
8) Reads or Writes listed in the Command/Action column include Reads or Writes with Auto Precharge enabled and Reads or Writes with Auto Precharge disabled.
9) May or may not be bank-specific; if all/any banks are to be precharged, all/any must be in a valid state for pre charging.

10) Not bank-specific; BURST TERMINATE affects the most recent Read burst, regardless of bank.
11) Requires appropriate DM masking.

TABLE 14
Truth Table 4: Current State Bank n - Command to Bank m (different bank)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Command	Action	Note
Any	H	X	X	X	Deselect	NOP. Continue previous operation.	1)2)3)4)5)6)
	L	H	H	H	No Operation	NOP. Continue previous operation.	1) to 6)
Idle	X	X	X	X	Any Command Otherwise Allowed to Bank m	–	1) to 6)
Row Activating, Active, or Pre charging	L	L	H	H	Active	Select and activate row	1) to 6)
	L	H	L	H	Read	Select column and start Read burst	1) to 7)
	L	H	L	L	Write	Select column and start Write burst	1) to 7)
	L	L	H	L	Precharge	–	1) to 6)
Read (Auto Precharge Disabled)	L	L	H	H	Active	Select and activate row	1) to 6)
	L	H	L	H	Read	Select column and start new Read burst	1) to 7)
	L	L	H	L	Precharge	–	1) to 6)
Write (Auto Precharge Disabled)	L	L	H	H	Active	Select and activate row	1) to 6)
	L	H	L	H	Read	Select column and start Read burst	1) to 8)
	L	H	L	L	Write	Select column and start new Write burst	1) to 7)
	L	L	H	L	Precharge	–	1) to 6)
Read (With Auto Precharge)	L	L	H	H	Active	Select and activate row	1) to 6)
	L	H	L	H	Read	Select column and start new Read burst	1) to 7), 9)
	L	H	L	L	Write	Select column and start Write burst	1) to 7), 9), 10)
	L	L	H	L	Precharge	–	1) to 6)
Write (With Auto Precharge)	L	L	H	H	Active	Select and activate row	1) to 6)
	L	H	L	H	Read	Select column and start Read burst	1) to 7), 9)
	L	H	L	L	Write	Select column and start new Write burst	1) to 7), 9)
	L	L	H	L	Precharge	–	1) to 6)

1) This table applies when CKE n-1 was HIGH and CKE n is HIGH (see **Table 12**: Clock Enable (CKE) and after t_{XSNR}/t_{XSRD} has been met (if the previous state was self refresh).
2) This table describes alternate bank operation, except where noted, i.e., the current state is for bank n and the commands shown are those allowed to be issued to bank m (assuming that bank m is in such a state that the given command is allowable). Exceptions are covered in the notes below.
3) Current state definitions:
Idle: The bank has been precharged, and t_{RP} has been met.
Row Active: A row in the bank has been activated, and t_{RCD} has been met. No data bursts/accesses and no register accesses are in progress.
Read: A Read burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.
Write: A Write burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.
Read with Auto Precharge Enabled: See [10].
Write with Auto Precharge Enabled: See [10].
4) AUTO REFRESH and Mode Register Set commands may only be issued when all banks are idle.
5) A BURST TERMINATE command cannot be issued to another bank; it applies to the bank represented by the current state only.
6) All states and sequences not shown are illegal or reserved.
7) Reads or Writes listed in the Command/Action column include Reads or Writes with Auto Precharge enabled and Reads or Writes with Auto Precharge disabled.
8) Requires appropriate DM masking.

9) Concurrent Auto Precharge:
This device supports "Concurrent Auto Precharge". When a read with auto precharge or a write with auto precharge is enabled any command may follow to the other banks as long as that command does not interrupt the read or write data transfer and all other limitations apply (e.g. contention between READ data and WRITE data must be avoided). The minimum delay from a read or write command with auto precharge enable, to a command to a different banks is summarized in **Table 15**.

10) A Write command may be applied after the completion of data output.

TABLE 15
Truth Table 5: Concurrent Auto Precharge

From Command	To Command (different bank)	Minimum Delay with Concurrent Auto Precharge Support	Unit
WRITE w/AP	Read or Read w/AP	1 + (BL/2) + RU(t_{WTR}/t_{CK})[1]	t_{CK}
	Write to Write w/AP	BL/2	t_{CK}
	Precharge or Activate	1	t_{CK}
Read w/AP	Read or Read w/AP	BL/2	t_{CK}
	Write or Write w/AP	RU(CL)[1] + BL/2	t_{CK}
	Precharge or Activate	1	t_{CK}

1) RU means rounded to the next integer

4 Electrical Characteristics

4.1 Operating Conditions

TABLE 16
Absolute Maximum Ratings

Parameter	Symbol	Values			Unit	Note/ Test Condition
		min.	typ.	max.		
Voltage on I/O pins relative to V_{SS}	V_{IN}, V_{OUT}	–0.5	–	V_{DDQ} + 0.5	V	–
Voltage on inputs relative to V_{SS}	V_{IN}	–1	–	+3.6	V	–
Voltage on V_{DD} supply relative to V_{SS}	V_{DD}	–1	–	+3.6	V	–
Voltage on V_{DDQ} supply relative to V_{SS}	V_{DDQ}	–1	–	+3.6	V	–
Operating temperature (ambient)	T_A	0	–	+70	°C	–
Storage temperature (plastic)	T_{STG}	-55	–	+150	°C	–
Power dissipation (per SDRAM component)	P_D	–	1	–	W	–
Short circuit output current	I_{OUT}	–	50	–	mA	–

***Attention:** Permanent damage to the device may occur if "Absolute Maximum Ratings" are exceeded. This is a stress rating only, and functional operation should be restricted to recommended operation conditions. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability and exceeding only one of the values may cause irreversible damage to the integrated circuit.*

TABLE 17
Input and Output Capacitances

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Input Capacitance: CK, $\overline{CK}$	C_{I1}	1.5	—	2.5	pF	TSOPII [1]
		2.0	—	3.0	pF	TFBGA [1]
Delta Input Capacitance	C_{dI1}	—	—	0.25	pF	[1]
Input Capacitance: All other input-only pins	C_{I2}	1.5	—	2.5	pF	TFBGA [1]
		2.0	—	3.0	pF	TSOPII [1]
Delta Input Capacitance: All other input-only pins	C_{dIO}	—	—	0.5	pF	[1]
Input/Output Capacitance: DQ, DQS, DM	C_{IO}	3.5	—	4.5	pF	TFBGA [1][2]
		4.0	—	5.0	pF	TSOPII [1][2]
Delta Input/Output Capacitance: DQ, DQS, DM	C_{dIO}	—	—	0.5	pF	[1]

1) These values are guaranteed by design and are tested on a sample base only. $V_{DDQ} = V_{DD} = 2.5\ \text{V} \pm 0.2\ \text{V}$, f= 100 MHz, T_A = 25 °C, $V_{OUT(DC)} = V_{DDQ}/2$, V_{OUT} (Peak to Peak) 0.2 V. Unused pins are tied to ground.
2) DM inputs are grouped with I/O pins reflecting the fact that they are matched in loading to DQ and DQS to facilitate trace matching at the board level.

TABLE 18
Electrical Characteristics and DC Operating Conditions

Parameter	Symbol	Values			Unit	Note[1]/Test Condition
		Min.	Typ.	Max.		
Device Supply Voltage	V_{DD}	2.3	2.5	2.7	V	$f_{CK} \leq$ 166 MHz
Device Supply Voltage	V_{DD}	2.5	2.6	2.7	V	$f_{CK} >$ 166 MHz [2]
Output Supply Voltage	V_{DDQ}	2.3	2.5	2.7	V	$f_{CK} \leq$ 166 MHz [3]
Output Supply Voltage	V_{DDQ}	2.5	2.6	2.7	V	$f_{CK} >$ 166 MHz [2][3]
EEPROM supply voltage	V_{DDSPD}	2.3	2.5	3.6	V	—
Supply Voltage, I/O Supply Voltage	V_{SS}, V_{SSQ}	0	—	0	V	—
Input Reference Voltage	V_{REF}	$0.49 \times V_{DDQ}$	$0.5 \times V_{DDQ}$	$0.51 \times V_{DDQ}$	V	[4]
I/O Termination Voltage (System)	V_{TT}	$V_{REF} - 0.04$	—	$V_{REF} + 0.04$	V	[5]
Input High (Logic1) Voltage	$V_{IH(DC)}$	$V_{REF} + 0.15$	—	$V_{DDQ} + 0.3$	V	[6]
Input Low (Logic0) Voltage	$V_{IL(DC)}$	–0.3	—	$V_{REF} - 0.15$	V	[6]
Input Voltage Level, CK and $\overline{CK}$ Inputs	$V_{IN(DC)}$	–0.3	—	$V_{DDQ} + 0.3$	V	[6]
Input Differential Voltage, CK and $\overline{CK}$ Inputs	$V_{ID(DC)}$	0.36	—	$V_{DDQ} + 0.6$	V	[6][7]
VI-Matching Pull-up Current to Pull-down Current	VI_{Ratio}	0.71	—	1.4	—	[8]
Input Leakage Current	I_I	–2	—	2	µA	Any input 0 V $\leq V_{IN} \leq V_{DD}$; All other pins not under test = 0 V [9]
Output Leakage Current	I_{OZ}	–5	—	5	µA	DQs are disabled; 0 V $\leq V_{OUT} \leq V_{DDQ}$ [9]
Output High Current, Normal Strength Driver	I_{OH}	—	—	–16.2	mA	V_{OUT} = 1.95 V
Output Low Current, Normal Strength Driver	I_{OL}	16.2	—	—	mA	V_{OUT} = 0.35 V

1) 0 °C $\leq T_A \leq$ 70 °C; V_{DDQ} = 2.5 V ± 0.2 V, V_{DD} = +2.5 V ± 0.2 V; V_{DDQ} = 2.6 V ± 0.1 V, V_{DD} = +2.6 V ± 0.1 V (DDR400);
2) DDR400 conditions apply for all clock frequencies above 166 MHz
3) Under all conditions, V_{DDQ} must be less than or equal to V_{DD}.
4) Peak to peak AC noise on V_{REF} may not exceed ± 2% V_{REF} (DC). V_{REF} is also expected to track noise variations in V_{DDQ}.
5) V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF}, and must track variations in the DC level of V_{REF}.
6) Inputs are not recognized as valid until V_{REF} stabilizes.
7) V_{ID} is the magnitude of the difference between the input level on CK and the input level on $\overline{CK}$.
8) The ratio of the pull-up current to the pull-down current is specified for the same temperature and voltage, over the entire temperature and voltage range, for device drain to source voltage from 0.25 to 1.0 V. For a given output, it represents the maximum difference between pull-up and pull-down drivers due to process variation.
9) Values are shown per pin.

4.2 AC Characteristics

(Notes 1-5 apply to the following Tables; Electrical Characteristics and DC Operating Conditions, AC Operating Conditions, I_{DD} Specifications and Conditions, and Electrical Characteristics and AC Timing.)Note

Note

1. All voltages referenced to V_{SS}
2. Tests for AC timing, I_{DD}, and electrical, AC and DC characteristics, may be conducted at nominal reference/supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range specified.
3. **Figure 3** represents the timing reference load used in defining the relevant timing parameters of the part. It is not intended to be either a precise representation of the typical system environment nor a depiction of the actual load presented by a production tester. System designers will use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers will correlate to their production test conditions (generally a coaxial transmission line terminated at the tester electronics).
4. AC timing and I_{DD} tests may use a V_{IL} to V_{IH} swing of up to 1.5 V in the test environment, but input timing is still referenced to V_{REF} (or to the crossing point for CK, $\overline{\text{CK}}$), and parameter specifications are guaranteed for the specified AC input levels under normal use conditions. The minimum slew rate for the input signals is 1 V/ns in the range between $V_{IL(AC)}$ and $V_{IH(AC)}$.
5. The AC and DC input level specifications are as defined in the SSTL_2 Standard (i.e. the receiver effectively switches as a result of the signal crossing the AC input level, and remains in that state as long as the signal does not ring back above (below) the DC input LOW (HIGH) level).
6. For System Characteristics like Setup & Holdtime Derating for Slew Rate, I/O Delta Rise/Fall Derating, DDR SDRAM Slew Rate Standards, Overshoot & Undershoot specification and Clamp V-I characteristics see the latest JEDEC specification for DDR components.

FIGURE 3
AC Output Load Circuit Diagram / Timing Reference Load

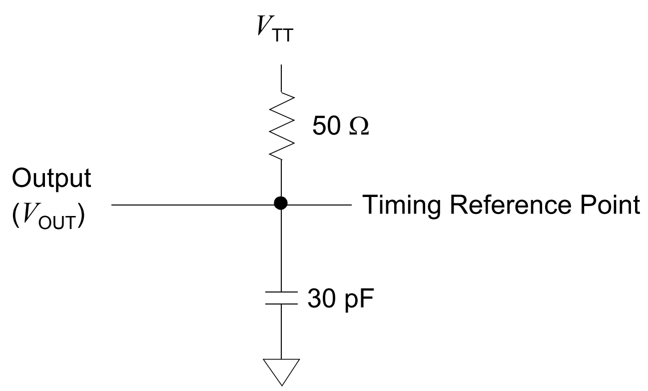


TABLE 19
AC Timing - Absolute Specifications for PC3200 and PC2700

Parameter	Symbol	–5		–6		Unit	Note[1]/Test Condition
		DDR400B		DDR333			
		Min.	Max.	Min.	Max.		
DQ output access time from CK/$\overline{CK}$	t_{AC}	–0.5	+0.5	–0.7	+0.7	ns	[2)3)4)5)]
CK high-level width	t_{CH}	0.45	0.55	0.45	0.55	t_{CK}	[2)3)4)5)]
Clock cycle time	t_{CK}	5	8	6	12	ns	CL = 3.0 [2)3)4)5)]
		6	12	6	12	ns	CL = 2.5 [2)3)4)5)]
		7.5	12	7.5	12	ns	CL = 2.0 [2)3)4)5)]
CK low-level width	t_{CL}	0.45	0.55	0.45	0.55	t_{CK}	[2)3)4)5)]
Auto precharge write recovery + precharge time	t_{DAL}	$(t_{WR}/t_{CK})+(t_{RP}/t_{CK})$				t_{CK}	[2)3)4)5)6)]
DQ and DM input hold time	t_{DH}	0.4	—	0.45	—	ns	[2)3)4)5)]
DQ and DM input pulse width (each input)	t_{DIPW}	1.75	—	1.75	—	ns	[2)3)4)5)6)]
DQS output access time from CK/$\overline{CK}$	t_{DQSCK}	–0.6	+0.6	–0.6	+0.6	ns	[2)3)4)5)]
DQS input low (high) pulse width (write cycle)	$t_{DQSL,H}$	0.35	—	0.35	—	t_{CK}	[2)3)4)5)]
DQS-DQ skew (DQS and associated DQ signals)	t_{DQSQ}	—	+0.40	—	+0.40	ns	TFBGA [2)3)4)5)]
		—	+0.40	—	+0.45	ns	TSOPII [2)3)4)5)]
Write command to 1st DQS latching transition	t_{DQSS}	0.72	1.25	0.75	1.25	t_{CK}	[2)3)4)5)]
DQ and DM input setup time	t_{DS}	0.4	—	0.45	—	ns	[2)3)4)5)]
DQS falling edge hold time from CK (write cycle)	t_{DSH}	0.2	—	0.2	—	t_{CK}	[2)3)4)5)]
DQS falling edge to CK setup time (write cycle)	t_{DSS}	0.2	—	0.2	—	t_{CK}	[2)3)4)5)]
Clock Half Period	t_{HP}	min. (t_{CL}, t_{CH})	—	min. (t_{CL}, t_{CH})	—	ns	[2)3)4)5)]
Data-out high-impedance time from CK/$\overline{CK}$	t_{HZ}	—	+0.7	–0.7	+0.7	ns	[2)3)4)5)7)]
Address and control input hold time	t_{IH}	0.6	—	0.75	—	ns	fast slew rate [3)4)5)6)8)]
		0.7	—	0.8	—	ns	slow slew rate[3)4)5)6)8)]
Control and Addr. input pulse width (each input)	t_{IPW}	2.2	—	2.2	—	ns	[2)3)4)5)9)]

Parameter	Symbol	–5		–6		Unit	Note[1]/Test Condition
		DDR400B		DDR333			
		Min.	Max.	Min.	Max.		
Address and control input setup time	t_{IS}	0.6	—	0.75	—	ns	fast slew rate [3)4)5)6)8)]
		0.7	—	0.8	—	ns	slow slew rate [3)4)5)6)8)]
Data-out low-impedance time from CK/$\overline{CK}$	t_{LZ}	–0.7	+0.70	–0.70	+0.70	ns	[2)3)4)5)7)]
Mode register set command cycle time	t_{MRD}	2	—	2	—	t_{CK}	[2)3)4)5)]
DQ/DQS output hold time	t_{QH}	$t_{HP} - t_{QHS}$	—	$t_{HP} - t_{QHS}$	—	ns	[2)3)4)5)]
Data hold skew factor	t_{QHS}	—	+0.50	—	+0.50	ns	TFBGA [2)3)4)5)]
		—	+0.50	—	+0.55	ns	TSOPII [2)3)4)5)]
Active to Autoprecharge delay	t_{RAP}	t_{RCD}	—	t_{RCD}	—	ns	[2)3)4)5)]
Active to Precharge command	t_{RAS}	40	70E+3	42	70E+3	ns	[2)3)4)5)]
Active to Active/Auto-refresh command period	t_{RC}	55	—	60	—	ns	[2)3)4)5)]
Active to Read or Write delay	t_{RCD}	15	—	18	—	ns	[2)3)4)5)]
Average Periodic Refresh Interval	t_{REFI}	—	7.8	—	7.8	µs	[2)3)4)5)8)]
Auto-refresh to Active/Auto-refresh command period	t_{RFC}	65	—	72	—	ns	[2)3)4)5)]
Precharge command period	t_{RP}	15	—	18	—	ns	[2)3)4)5)]
Read preamble	t_{RPRE}	0.9	1.1	0.9	1.1	t_{CK}	[2)3)4)5)]
Read postamble	t_{RPST}	0.40	0.60	0.40	0.60	t_{CK}	[2)3)4)5)]
Active bank A to Active bank B command	t_{RRD}	10	—	12	—	ns	[2)3)4)5)]
Write preamble	t_{WPRE}	0.25	—	0.25	—	t_{CK}	[2)3)4)5)]
Write preamble setup time	t_{WPRES}	0	—	0	—	ns	[2)3)4)5)10)]
Write postamble	t_{WPST}	0.40	0.60	0.40	0.60	t_{CK}	[2)3)4)5)11)]
Write recovery time	t_{WR}	15	—	15	—	ns	[2)3)4)5)]
Internal write to read command delay	t_{WTR}	2	—	1	—	t_{CK}	[2)3)4)5)]
Exit self-refresh to non-read command	t_{XSNR}	75	—	75	—	ns	[2)3)4)5)]
Exit self-refresh to read command	t_{XSRD}	200	—	200	—	t_{CK}	[2)3)4)5)]

1) 0 °C ≤ T_A ≤ 70 °C; V_{DDQ} = 2.5 V ± 0.2 V, V_{DD} = +2.5 V ± 0.2 V (DDR333); V_{DDQ} = 2.6 V ± 0.1 V, V_{DD} = +2.6 V ± 0.1 V (DDR400)
2) Input slew rate ≥ 1 V/ns for DDR400, DDR333
3) The CK/$\overline{CK}$ input reference level (for timing reference to CK/$\overline{CK}$) is the point at which CK and $\overline{CK}$ cross: the input reference level for signals other than CK/$\overline{CK}$, is V_{REF}. CK/$\overline{CK}$ slew rate are ≥ 1.0 V/ns.
4) Inputs are not recognized as valid until V_{REF} stabilizes.
5) The Output timing reference level, as measured at the timing reference point indicated in AC Characteristics (note 3) is V_{TT}.
6) For each of the terms, if not already an integer, round to the next highest integer. t_{CK} is equal to the actual system clock cycle time.

7) t_{HZ} and t_{LZ} transitions occur in the same access time windows as valid data transitions. These parameters are not referred to a specific voltage level, but specify when the device is no longer driving (HZ), or begins driving (LZ).
8) Fast slew rate ≥ 1.0 V/ns , slow slew rate ≥ 0.5 V/ns and < 1 V/ns for command/address and CK & $\overline{CK}$ slew rate > 1.0 V/ns, measured between $V_{IH(ac)}$ and $V_{IL(ac)}$.
9) These parameters guarantee device timing, but they are not necessarily tested on each device.
10) The specific requirement is that DQS be valid (HIGH,LOW, or some point on a valid transition) on or before this CK edge. A valid transition is defined as monotonic and meeting the input slew rate specificationsof the device. When no writes were previously in progress on the bus, DQS will be transitioning from Hi-Z to logic LOW. If a previous write was in progress, DQS could be HIGH, LOW at this time, depending on t_{DQSS}.
11) The maximum limit for this parameter is not a device limit. The device operates with a greater value for this parameter, but system performance (bus turnaround) degrades accordingly.

TABLE 20
AC Timing - Absolute Specifications for PC2100

Parameter	Symbol	–7		Unit	Note[1]/Test Condition
		DDR266A			
		Min.	Max.		
DQ output access time from CK/$\overline{CK}$	t_{AC}	–0.75	+0.75	ns	2)3)4)5)
CK high-level width	t_{CH}	0.45	0.55	t_{CK}	2)3)4)5)
Clock cycle time	t_{CK}	7.5	12	ns	CL = 3.0 2)3)4)5)
		7.5	12	ns	CL = 2.5 2)3)4)5)
		7.5	12	ns	CL = 2.0 2)3)4)5)
CK low-level width	t_{CL}	0.45	0.55	t_{CK}	2)3)4)5)
Auto precharge write recovery + precharge time	t_{DAL}	$(t_{WR}/t_{CK})+(t_{RP}/t_{CK})$	—	t_{CK}	2)3)4)5)6)
DQ and DM input hold time	t_{DH}	0.5	—	ns	2)3)4)5)
DQ and DM input pulse width (each input)	t_{DIPW}	1.75	—	ns	2)3)4)5)6)
DQS output access time from CK/$\overline{CK}$	t_{DQSCK}	–0.75	+0.75	ns	2)3)4)5)
DQS input low (high) pulse width (write cycle)	$t_{DQSL,H}$	0.35	—	t_{CK}	2)3)4)5)
DQS-DQ skew (DQS and associated DQ signals)	t_{DQSQ}	—	+0.5	ns	TSOPII 2)3)4)5)
Write command to 1st DQS latching transition	t_{DQSS}	0.75	1.25	t_{CK}	2)3)4)5)
DQ and DM input setup time	t_{DS}	0.5	—	ns	2)3)4)5)
DQS falling edge hold time from CK (write cycle)	t_{DSH}	0.2	—	t_{CK}	2)3)4)5)
DQS falling edge to CK setup time (write cycle)	t_{DSS}	0.2	—	t_{CK}	2)3)4)5)
Clock Half Period	t_{HP}	min. (t_{CL}, t_{CH})		ns	2)3)4)5)
Data-out high-impedance time from CK/$\overline{CK}$	t_{HZ}	–0.75	+0.75	ns	2)3)4)5)7)
Address and control input hold time	t_{IH}	0.9	—	ns	fast slew rate 3)4)5)6)8)
		1.0	—	ns	slow slew rate 3)4)5)6)8)
Control and Addr. input pulse width (each input)	t_{IPW}	2.2	—	ns	2)3)4)5)9)
Address and control input setup time	t_{IS}	0.9	—	ns	fast slew rate 3)4)5)6)8)
		1.0	—	ns	slow slew rate 3)4)5)6)8)
Data-out low-impedance time from CK/$\overline{CK}$	t_{LZ}	–0.75	+0.75	ns	2)3)4)5)7)

Parameter	Symbol	–7		Unit	Note[1]/Test Condition
		DDR266A			
		Min.	Max.		
Mode register set command cycle time	t_{MRD}	2	—	t_{CK}	2)3)4)5)
DQ/DQS output hold time	t_{QH}	$t_{HP} - t_{QHS}$		ns	2)3)4)5)
Data hold skew factor	t_{QHS}	—	0.75	ns	TSOPII 2)3)4)5)
Active to Read w/AP delay	t_{RAP}	t_{RCD}	—	ns	2)3)4)5)
Active to Precharge command	t_{RAS}	45	120E+3	ns	2)3)4)5)
Active to Active/Auto-refresh command period	t_{RC}	65	—	ns	2)3)4)5)
Active to Read or Write delay	t_{RCD}	20	—	ns	2)3)4)5)
Average Periodic Refresh Interval	t_{REFI}	7.8	—	µs	2)3)4)5)10)
Auto-refresh to Active/Auto-refresh command period	t_{RFC}	75	—	ns	2)3)4)5)
Precharge command period	t_{RP}	20	—	ns	2)3)4)5)
Read preamble	t_{RPRE}	0.9	1.1	t_{CK}	2)3)4)5)
Read postamble	t_{RPST}	0.4	0.6	t_{CK}	2)3)4)5)
Active bank A to Active bank B command	t_{RRD}	15	—	ns	2)3)4)5)
Write preamble	t_{WPRE}	0.25	—	t_{CK}	2)3)4)5)
Write preamble setup time	t_{WPRES}	0	—	ns	2)3)4)5)11)
Write postamble	t_{WPST}	0.4	—	t_{CK}	2)3)4)5)12)
Write recovery time	t_{WR}	15	—	ns	2)3)4)5)
Internal write to read command delay	t_{WTR}	1	—	t_{CK}	2)3)4)5)
Exit self-refresh to non-read command	t_{XSNR}	75		ns	2)3)4)5)13)
Exit self-refresh to read command	t_{XSRD}	200	—	t_{CK}	2)3)4)5)

1) V_{DDQ} = 2.5 V ± 0.2 V, V_{DD} = +2.5 V ± 0.2 V ; 0 °C ≤ T_A ≤ 70 °C
2) Input slew rate ≥ 1 V/ns
3) The CK/$\overline{CK}$ input reference level (for timing reference to CK/$\overline{CK}$) is the point at which CK and $\overline{CK}$ cross: the input reference level for signals other than CK/$\overline{CK}$, is V_{REF}. CK/$\overline{CK}$ slew rate are ≥ 1.0 V/ns.
4) Inputs are not recognized as valid until V_{REF} stabilizes.
5) The Output timing reference level, as measured at the timing reference point indicated in AC Characteristics (note 3) is V_{TT}.
6) For each of the terms, if not already an integer, round to the next highest integer. t_{CK} is equal to the actual system clock cycle time.
7) t_{HZ} and t_{LZ} transitions occur in the same access time windows as valid data transitions. These parameters are not referred to a specific voltage level, but specify when the device is no longer driving (HZ), or begins driving (LZ).
8) Fast slew rate ≥ 1.0 V/ns , slow slew rate ≥ 0.5 V/ns and < 1 V/ns for command/address and CK & $\overline{CK}$ slew rate > 1.0 V/ns, measured between $V_{IH(ac)}$ and $V_{IL(ac)}$.
9) These parameters guarantee device timing, but they are not necessarily tested on each device.
10) A maximum of eight Autorefresh commands can be posted to any given DDR SDRAM device.
11) The specific requirement is that DQS be valid (HIGH, LOW, or some point on a valid transition) on or before this CK edge. A valid transition is defined as monotonic and meeting the input slew rate specifications of the device. When no writes were previously in progress on the bus, DQS will be transitioning from Hi-Z to logic LOW. If a previous write was in progress, DQS could be HIGH, LOW, or transitioning from HIGH to LOW at this time, depending on t_{DQSS}.
12) The maximum limit for this parameter is not a device limit. The device operates with a greater value for this parameter, but system performance (bus turnaround) degrades accordingly.
13) In all circumstances, t_{XSNR} can be satisfied using $t_{XSNR} = t_{RFC,min} + 1 \times t_{CK}$

TABLE 21
I_{DD} Conditions

Parameter	Symbol
Operating Current: one bank; active/ precharge; $t_{RC} = t_{RCMIN}$; $t_{CK} = t_{CKMIN}$; DQ, DM, and DQS inputs changing once per clock cycle; address and control inputs changing once every two clock cycles.	I_{DD0}
Operating Current: one bank; active/read/precharge; Burst = 4; Refer to the following page for detailed test conditions.	I_{DD1}
Precharge Power-Down Standby Current: all banks idle; power-down mode; CKE ≤ V_{ILMAX}; $t_{CK} = t_{CKMIN}$	I_{DD2P}
Precharge Floating Standby Current: $\overline{CS}$ ≥ V_{IHMIN}, all banks idle; CKE ≥ V_{IHMIN}; $t_{CK} = t_{CKMIN}$, address and other control inputs changing once per clock cycle, $V_{IN} = V_{REF}$ for DQ, DQS and DM.	I_{DD2F}
Precharge Quiet Standby Current: $\overline{CS}$ ≥ V_{IHMIN}, all banks idle; CKE ≥ V_{IHMIN}; $t_{CK} = t_{CKMIN}$, address and other control inputs stable at ≥ V_{IHMIN} or ≤ V_{ILMAX}; $V_{IN} = V_{REF}$ for DQ, DQS and DM.	I_{DD2Q}
Active Power-Down Standby Current: one bank active; power-down mode; CKE ≤ V_{ILMAX}; $t_{CK} = t_{CKMIN}$; $V_{IN} = V_{REF}$ for DQ, DQS and DM.	I_{DD3P}
Active Standby Current: one bank active; $\overline{CS}$ ≥ V_{IHMIN}; CKE ≥ V_{IHMIN}; $t_{RC} = t_{RASMAX}$; $t_{CK} = t_{CKMIN}$; DQ, DM and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle.	I_{DD3N}
Operating Current: one bank active; Burst = 2; reads; continuous burst; address and control inputs changing once per clock cycle; 50% of data outputs changing on every clock edge; CL = 2 for DDR200 and DDR266A, CL = 3 for DDR333; $t_{CK} = t_{CKMIN}$; I_{OUT} = 0 mA	I_{DD4R}
Operating Current: one bank active; Burst = 2; writes; continuous burst; address and control inputs changing once per clock cycle; 50% of data outputs changing on every clock edge; CL = 2 for DDR200 and DDR266A, CL = 3 for DDR333; $t_{CK} = t_{CKMIN}$	I_{DD4W}
Auto-Refresh Current: $t_{RC} = t_{RFCMIN}$, burst refresh	I_{DD5}
Self-Refresh Current: CKE ≤ 0.2 V; external clock on; $t_{CK} = t_{CKMIN}$	I_{DD6}
Operating Current: four bank; four bank interleaving with BL = 4; Refer to the following page for detailed test conditions.	I_{DD7}

TABLE 22
I_{DD} Specification

	–7		–6		–5		Unit	Note[1]/Test Condition
	DDR266A		DDR333		DDR400B			
Symbol	Typ.	Max.	Typ.	Max.	Typ.	Max.		
I_{DD0}	65	78	75	90	80	100	mA	×4/×8 [2)3)]
	80	95	90	110	100	120	mA	×16 [3)]
I_{DD1}	75	90	85	100	90	110	mA	×4/×8 [3)]
	90	110	105	125	115	140	mA	×16 [3)]
I_{DD2P}	1.5	4	1.6	4	1.7	4	mA	[3)]
I_{DD2F}	20	24	25	30	30	36	mA	[3)]
I_{DD2Q}	15	21	17	24	19	26	mA	[3)]
I_{DD3P}	9	13	11	15	12	16	mA	[3)]
I_{DD3N}	29	35	35	41	39	47	mA	×4/×8 [3)]
	31	37	37	44	42	50	mA	×16 [3)]
I_{DD4R}	67	78	77	90	85	100	mA	×4/×8 [3)]
	85	100	105	125	120	145	mA	×16 [3)]
I_{DD4W}	71	83	81	95	90	105	mA	×4/×8 [3)]
	90	105	110	130	125	150	mA	×16 [3)]
I_{DD5}	170	205	185	220	205	245	mA	[3)4)]
I_{DD6}	2.6	5.0	2.7	5.0	2.8	5.0	mA	[3)]
	2.5	2.5	2.5	2.5	2.5	2.5	mA	low power
I_{DD7}	204	243	234	279	260	310	mA	×4/×8 [3)]
	215	255	255	310	285	340	mA	×16 [3)]

1) Test conditions for typical values: V_{DD} = 2.5 V (DDR266, DDR333), V_{DD} = 2.6 V (DDR400), T_A = 25 °C, test conditions for maximum values: V_{DD} = 2.7 V, T_A = 10 °C

2) I_{DD} specifications are tested after the device is properly initialized and measured at 133 MHz for DDR266, 166 MHz for DDR333, and 200 MHz for DDR400.

3) Input slew rate = 1 V/ns.

4) Enables on-chip refresh and address counters.

5 Package Outlines

There are two package types used for this product family each in lead-free and lead-containing assembly:

- P-TFBGA: Plastic Thin Fine-Pitch Ball Grid Array Package

TABLE 23
TFBGA Common Package Properties (non-green/green)

Description	Size	Units
Ball Size	0.460	mm
Recommended Landing Pad	0.350	mm
Recommended Solder Mask	0.450	mm

- P-TSOPII: Plastic Thin Small Outline Package Type II

FIGURE 4
Package Outline of P-TFBGA-60-[9/22] (green/non-green)

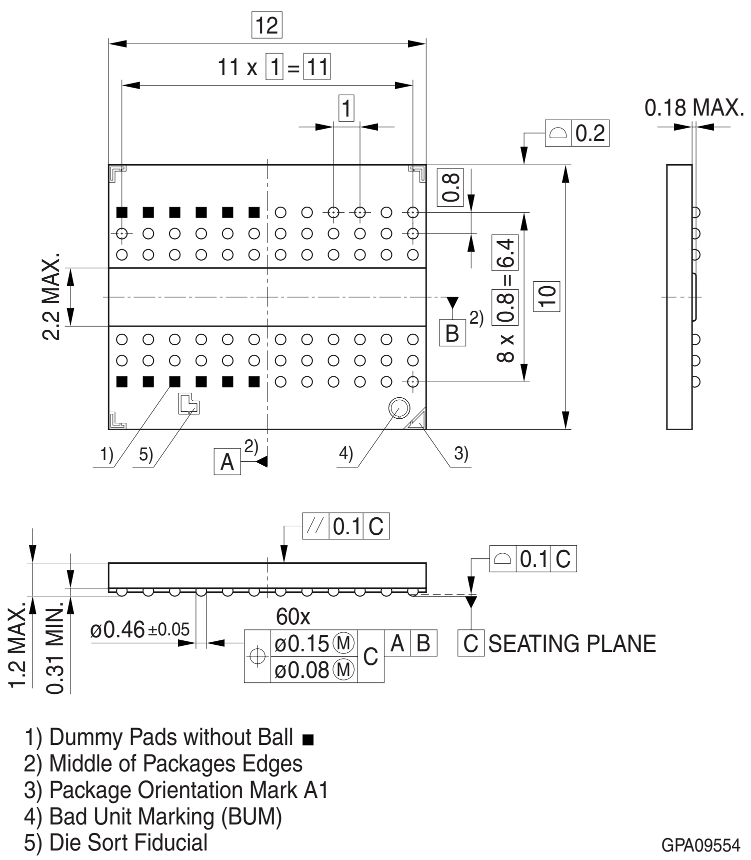
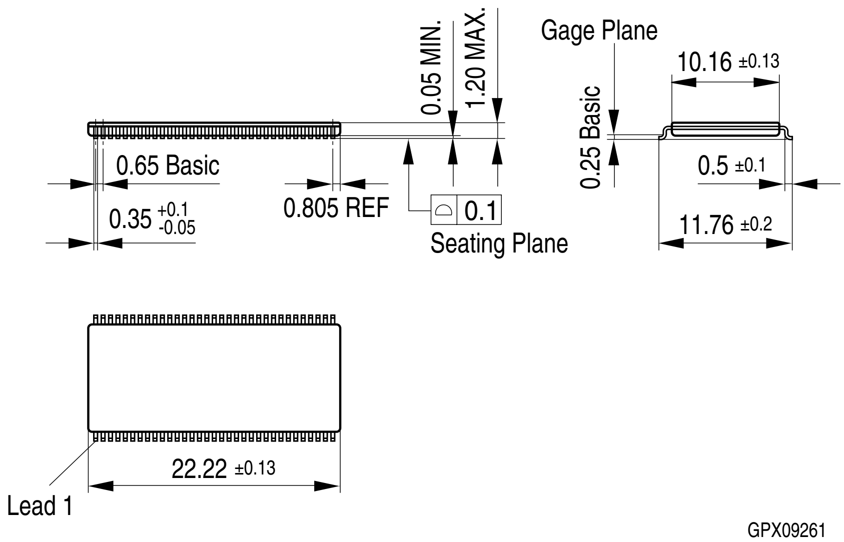


FIGURE 5
Package Outline of P-TSOPII-66-1 (Lead-Free/Lead-Containing)



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