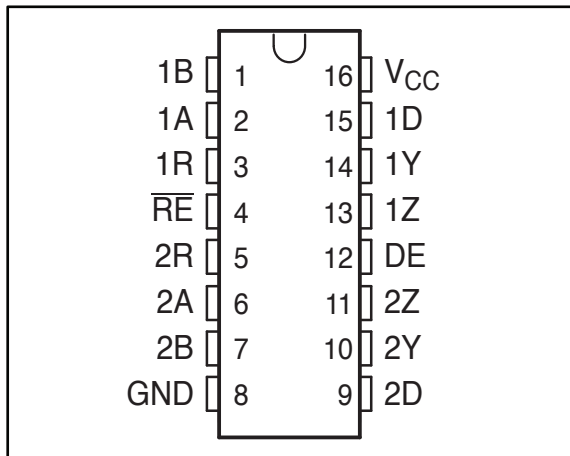


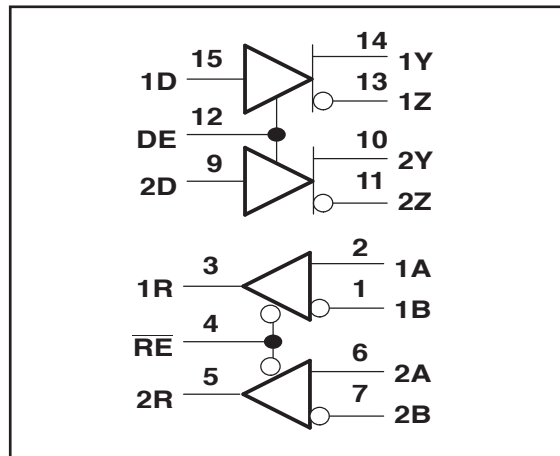
**Dual Differential LVDS/LVPECL/HSTL to LVTTTL Translator**  
**Dual LVTTTL/LVCMOS to Differential HSTL Translator**

FEATURES:	DESCRIPTION:
<ul style="list-style-type: none"> <li>• Patented Technology</li> <li>• Differential LVDS/LVPECL/HSTL to LVTTTL Translator               <ul style="list-style-type: none"> <li>- Operating frequency up to 1GHz with 2pf load</li> <li>- Operating frequency up to 800MHz with 5pf load</li> <li>- Operating frequency up to 450MHz with 15pf load</li> <li>- Very low output pin to pin skew &lt; 150ps</li> <li>- Propagation delay &lt; 1.8ns max with 15pf load</li> </ul> </li> <li>• LVTTTL/LVCMOS to Differential HSTL Translator               <ul style="list-style-type: none"> <li>- Operating frequency up to 1.65GHz with 5pf load</li> <li>- Operating frequency up to 500MHz with 15pf load</li> <li>- Very low output pin to pin skew &lt; 100ps</li> <li>- Propagation delay &lt; 1.4ns max with 15pf load</li> </ul> </li> <li>• 2.4V to 3.6V power supply</li> <li>• Industrial temperature range: -40°C to 85°C</li> <li>• Available in 16-pin 150ml SOIC package</li> </ul>	<p>Potato Semiconductor's PO100HSTL50A is designed for world top performance using submicron CMOS technology to achieve 1GHz LVTTTL output frequency with less than 1.8ns propagation delay and 1.65GHz HSTL output frequency with less than 1.4ns propagation delay.</p> <p>The PO100HSTL50A is a low-skew, The small outline 16 pin package and the low skew design to make it ideal for applications which require the translation of a clock or a data signal.</p>

**Pin Configuration**



**Logic Block Diagram**



**Pin Description**

RECEIVER INPUTS		RECEIVER OUTPUT
$V_{ID} = V_A - V_B$	$\overline{RE}$	R
$V_{ID} \geq 50 \text{ mV}$	L	H
$50 \text{ mV} < V_{ID} < 50 \text{ mV}$	L	?
$V_{ID} \leq -50 \text{ mV}$	L	L
Open	L	H
X	H	Z

DRIVER INPUTS		DRIVER OUTPUTS	
D	DE	Y	Z
L	H	L	H
H	H	H	L
Open	H	L	H
X	L	Z	Z

## Dual Differential LVDS/LVPECL/HSTL to LVTTTL Translator Dual LVTTTL/LVCMOS to Differential HSTL Translator

### Maximum Ratings

Description	Max	Unit
Storage Temperature	-65 to 150	°C
Operation Temperature	-40 to 85	°C
Operation Voltage	-0.5 to +4.6	V
Input Voltage	-0.5 to Vcc	V
Output Voltage	-0.5 to Vcc+0.5	V

#### Note:

stresses greater than listed under Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability specification is not implied.

### Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C <sub>IN</sub>	Input Capacitance			4		pF
R <sub>PULLUP</sub>	Input B Pullup Resistor			88		KΩ
R <sub>PULLDOWN</sub>	Input A Pulldown Resistor			88		KΩ

### DC Electrical Characteristics

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
V <sub>OH</sub>	Output High voltage	Vcc=3V Vin=VIH or VIL, IOH= -12mA	2.4	3	-	V
V <sub>OL</sub>	Output Low voltage	Vcc=3V Vin=VIH or VIL, IOH=12mA	-	0.3	0.5	V
V <sub>IH</sub>	Input High voltage	Guaranteed Logic HIGH Level (Input Pin)	2	-	Vcc	V
V <sub>IL</sub>	Input Low voltage	Guaranteed Logic LOW Level (Input Pin)	-0.5	-	0.8	V
I <sub>IH</sub>	Input High current	Vcc = 3.6V and Vin = Vcc	-	-	1	uA
I <sub>IL</sub>	Input Low current	Vcc = 3.6V and Vin = 0V	-	-	-1	uA
V <sub>IK</sub>	Clamp diode voltage	Vcc = Min. And IIN = -18mA	-	-0.7	-1.2	V

#### Notes:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 3.3V, 25 °C ambient.
3. This parameter is guaranteed but not tested.
4. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
5. VoH = Vcc - 0.6V at rated current

## Dual Differential LVDS/LVPECL/HSTL to LVTTTL Translator Dual LVTTTL/LVCMOS to Differential HSTL Translator

### Power Supply Characteristics

Symbol	Description	Test Conditions (1)	Min	Typ	Max	Unit
I <sub>ccQ</sub>	Quiescent Power Supply Current	V <sub>cc</sub> =Max, V <sub>in</sub> =V <sub>cc</sub> or GND	-	0.1	30	uA

#### Notes:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V<sub>cc</sub> = 3.3V, 25°C ambient.
3. This parameter is guaranteed but not tested.
4. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.

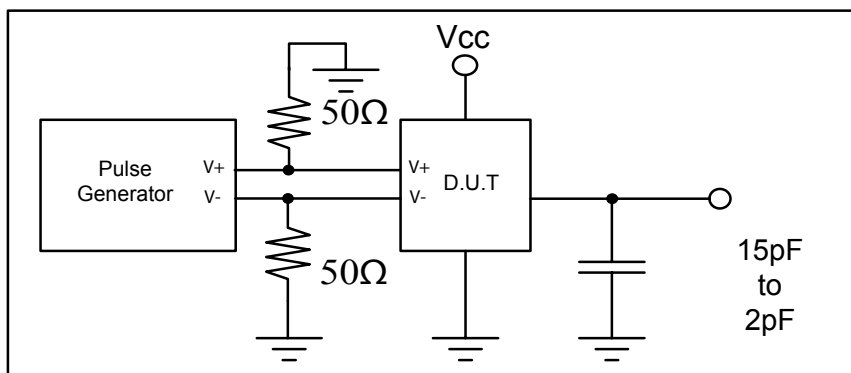
### Receiver Switching Characteristics

Symbol	Description	Test Conditions (1)	Max	Unit
t <sub>PD</sub>	Propagation Delay D to Output pair	CL = 15pF	1.8	ns
t <sub>PZH</sub> or t <sub>PZL</sub>	Output Enable Time	CL = 15pF	2.5	ns
t <sub>PHZ</sub> or t <sub>PLZ</sub>	Output Disable Time	CL = 15pF	2.5	ns
t <sub>r</sub> /t <sub>f</sub>	Rise/Fall Time	0.8V – 2.0V	0.8	ns
t <sub>sk(o)</sub>	Output Pin to Pin Skew (Same Package)	CL = 15pF, 125MHz	150	ps
t <sub>sk(pp)</sub>	Output Skew (Different Package)	CL = 15pF, 125MHz	300	ps
f <sub>max</sub>	Input Frequency	CL = 15pF	450	MHz
f <sub>max</sub>	Input Frequency	CL = 5pF	800	MHz
f <sub>max</sub>	Input Frequency	CL = 2pF	1000	MHz

#### Notes:

1. See test circuits and waveforms.
2. t<sub>pLH</sub>, t<sub>pHL</sub>, t<sub>sk(p)</sub>, and t<sub>sk(o)</sub> are production tested. All other parameters guaranteed but not production tested.
3. Airflow of 1m/s is recommended for frequencies above 133MHz

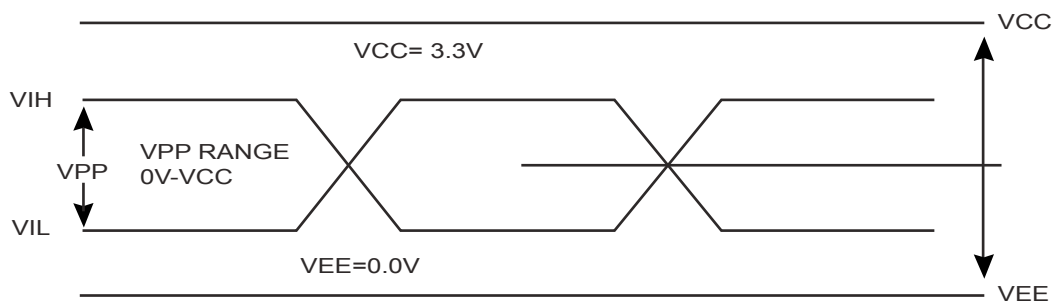
### Test Circuit



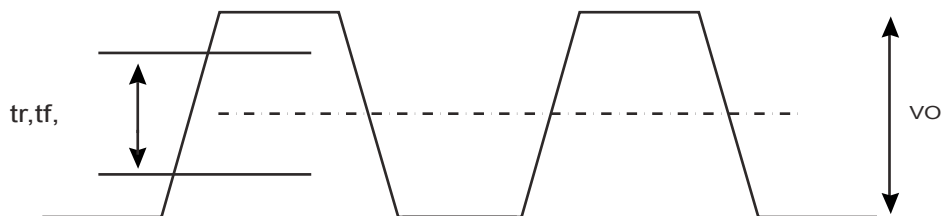
**Dual Differential LVDS/LVPECL/HSTL to LVTTTL Translator**  
**Dual LVTTTL/LVCMOS to Differential HSTL Translator**

## Test Waveforms

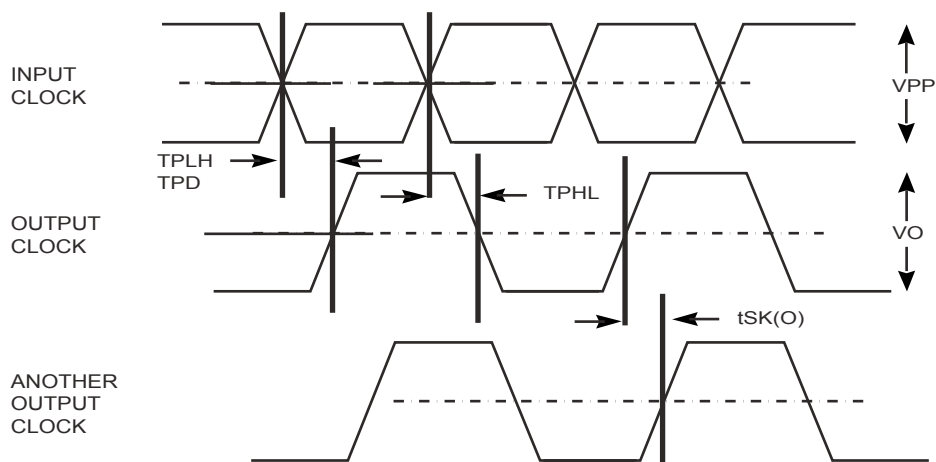
**FIGURE 1.**  
LVDS/ PECL/ ECL/ HSTL /DIFFERENTIAL INPUT WAVEFORM DEFINITIONS



**FIGURE 2.**  
LVTTTL OUTPUT



**FIGURE 3.**  
Propagation Delay, Output pulse skew, and output-to-output skew for D to output



## Dual Differential LVDS/LVPECL/HSTL to LVTTTL Translator Dual LVTTTL/LVCMOS to Differential HSTL Translator

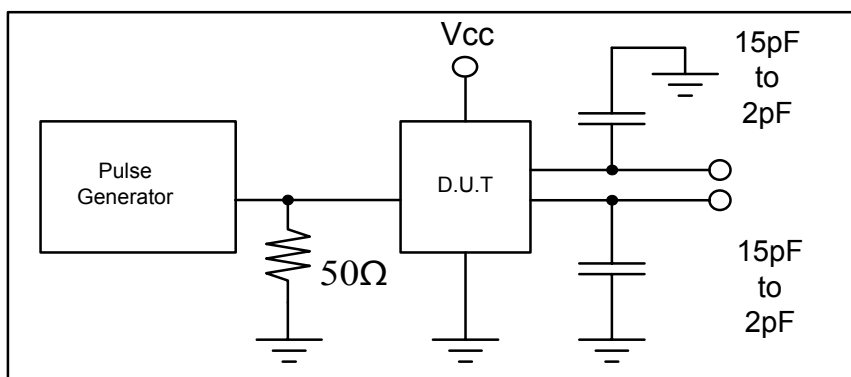
### Driver Switching Characteristics

Symbol	Description	Test Conditions (1)	Typ	Max	Unit
<b>tpD</b>	Propagation Delay D to Output pair	CL = 15pF		<b>1.4</b>	<b>ns</b>
<b>tpZH or tpZL</b>	Output Enable Time	CL = 15pF		<b>2.5</b>	<b>ns</b>
<b>tpHZ or tpLZ</b>	Output Disable Time	CL = 15pF		<b>2.5</b>	<b>ns</b>
<b>tr/tf</b>	Rise/Fall Time	0.8V – 2.0V		<b>0.8</b>	<b>ns</b>
<b>tsk(o)</b>	Output Pin to Pin Skew (Same Package)	CL = 15pF, 125MHz		<b>100</b>	<b>ps</b>
<b>tsk(pp)</b>	Output Skew (Different Package)	CL = 15pF, 125MHz		<b>250</b>	<b>ps</b>
<b>fmax</b>	Input Frequency	CL = 15pF		<b>500</b>	<b>MHz</b>
<b>fmax</b>	Input Frequency	CL = 5pF		<b>1.65</b>	<b>GHz</b>

#### Notes:

1. See test circuits and waveforms.
2. tpLH, tpHL, tsk(p), and tsk(o) are production tested. All other parameters guaranteed but not production tested.
3. Airflow of 1m/s is recommended for frequencies above 133MHz

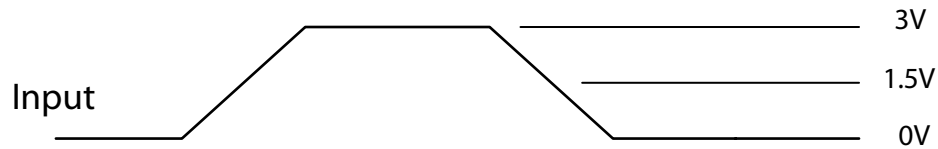
### Test Circuit



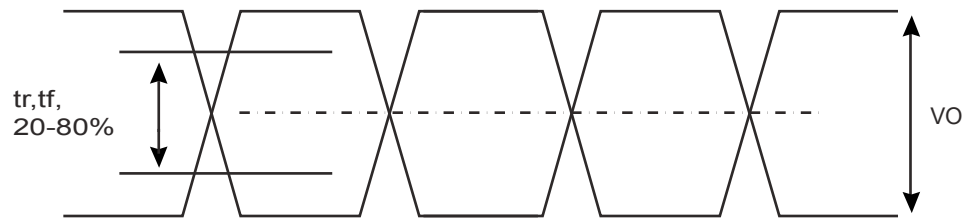
**Dual Differential LVDS/LVPECL/HSTL to LVTTTL Translator**  
**Dual LVTTTL/LVCMOS to Differential HSTL Translator**

**Test Waveforms**

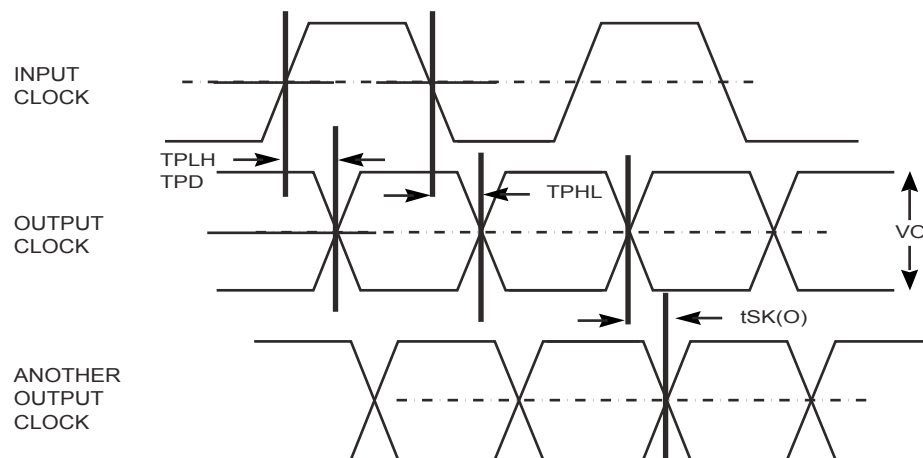
**FIGURE 1.  
LVTTTL/LVCMOS INPUT WAVEFORM DEFINITION**



**FIGURE 2.  
HSTL OUTPUT**

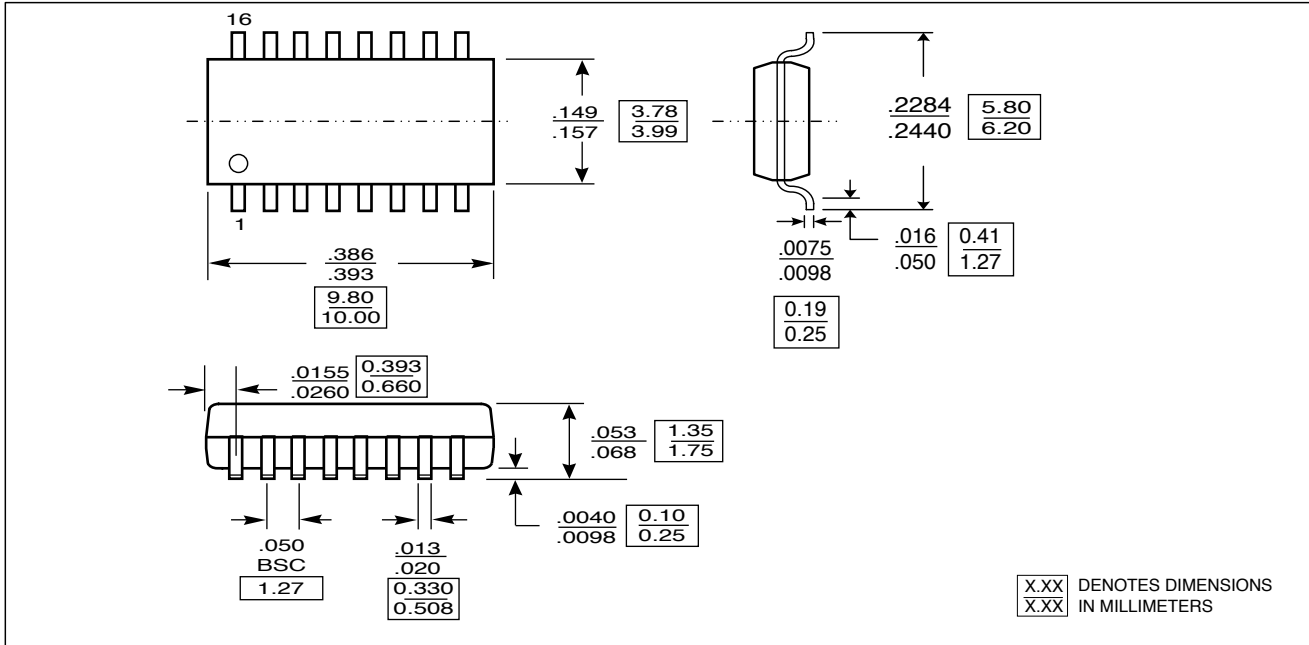


**FIGURE 3.  
Propagation Delay, Output pulse skew, and output-to-output skew for D to output pair**



**Dual Differential LVDS/LVPECL/HSTL to LVTTTL Translator**  
**Dual LVTTTL/LVCMOS to Differential HSTL Translator**

**Packaging Mechanical Drawing: 16 pin SOIC**



**Dual Differential LVDS/LVPECL/HSTL to LVTTTL Translator**  
**Dual LVTTTL/LVCMOS to Differential HSTL Translator**

**Ordering Information**

Ordering Code	Package			Top-Marking	T <sub>A</sub>
PO100HSTL50ASU	16 pin SOIC	Tube	Pb-free & Green	PO100HSTL23AS	-40°C to 85°C
PO100HSTL50ASR	16 pin SOIC	Tape and reel	Pb-free & Green	PO100HSTL23AS	-40°C to 85°C

**IC Package Information**

PACKAGE CODE	PACKAGE TYPE	TAPE WIDTH (mm)	TAPE PITCH (mm)	PIN 1 LOCATION	TAPE TRAILER LENGTH	QTY PER REEL	TAPE LEADER LENGTH	QTY PER TUBE
S	SOIC 16	16	8	Top Left Corner	39 (12")	3000	64 (20")	48