

# SANYO Semiconductors DATA SHEET

Monolithic Linear IC

# **LA6574D** — Five-Channel Driver (four BTL channels plus one H bridge channel) for MD and CD Player

#### Overview

The LA6574D is a motor driver IC for MD and CD players with four BTL channels and one H bridge channel. The LA6574D features a separate power supply for the H bridge block, an output adjustment pin, and a 3.3V regulator to support a wide range of applications.

#### **Features and Features**

- Four power amplifier channels plus one H bridge channel
- IO max: 700mA (each channel)
- Built-in level shifting circuits for the BLT amplifiers
- Thermal protection circuit (Thermal shutdown circuit)
- Separate loading block power supply
- Built-in 3.3V regulator
- Provides a dedicated pin for adjusting the loading block output

#### **Specifications**

#### **Maximum Ratings** at $Ta = 25^{\circ}C$

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V <sub>CC</sub> max		14	V
Allowable power dissipation	Pd max	Independent IC	1.2	W
		Mounted on a specified board	2.0	W
Maximum output current	I <sub>O</sub> max	Each channel for CH1 to CH5	0.7	Α
Maximum input voltage	VINB		13	V
MUTE pin voltage	VMUTE		13	V
Operating temperature	Topr		-30 to +85	°C
Storage temperature	Tstg		-55 to +150	°C

<sup>\*</sup> Mounted on a specified board: 76.1mm×114.3mm×1.6mm glass epoxy

- Any and all SANYO Semiconductor Co.,Ltd. products described or contained herein are, with regard to "standard application", intended for the use as general electronics equipment (home appliances, AV equipment, communication device, office equipment, industrial equipment etc.). The products mentioned herein shall not be intended for use for any "special application" (medical equipment whose purpose is to sustain life, aerospace instrument, nuclear control device, burning appliances, transportation machine, traffic signal system, safety equipment etc.) that shall require extremely high level of reliability and can directly threaten human lives in case of failure or malfunction of the product or may cause harm to human bodies, nor shall they grant any guarantee thereof. If you should intend to use our products for applications outside the standard applications of our customer who is considering such use and/or outside the scope of our intended standard applications, please consult with us prior to the intended use. If there is no consultation or inquiry before the intended use, our customer shall be solely responsible for the use.
- Specifications of any and all SANYO Semiconductor Co.,Ltd. products described or contained herein stipulate the performance, characteristics, and functions of the described products in the independent state, and are not guarantees of the performance, characteristics, and functions of the described products as mounted in the customer's products or equipment. To verify symptoms and states that cannot be evaluated in an independent device, the customer should always evaluate and test devices mounted in the customer's products or equipment.

#### **Recommended Operating Conditions** at $Ta = 25^{\circ}C$

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V <sub>CC</sub>		5.6 to 13	V

#### **Electrical Characteristics** at Ta = 25°C, $V_{CC}1 = V_{CC}2 = 8V$ , VREF = 1.65V

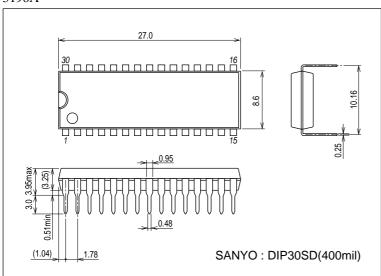
De servente e	O. make al	O - maliai - m -	Ratings			1.1:4
Parameter	Symbol	Symbol Conditions		typ	max	Unit
[Overall Characteristics]						
No load current drain - I <sub>CC</sub> on	I <sub>CC</sub> -ON	All outputs on, FWD = REV = 0V *1		30	50	mA
VREF input voltage range	VREF-IN		1		V <sub>CC</sub> -1.5	V
[BTL Amplifier Block]						
Output offset voltage	VOFF	BTL amplifiers, the voltage difference across each channel's output	-50		50	mV
Input voltage range	VIN	Input resistance: 11kΩ	0		V <sub>CC</sub>	V
Output voltage	Vo	The voltage between each of the V_O+/V_O- pairs when R_L is $8\Omega$ .	4	5		V
Closed loop voltage gain	VG	Gain from input to output		4		Times
Slew rate	SR	With the amplifier operating independently, twice the value measured between outputs *3		0.5		V/μs
[H Bridge Block]						
Output voltage	V <sub>O</sub> -LOAD	The voltage between each of the $V_{O}$ +/ $V_{O}$ - pairs when $R_{L}$ is $8\Omega$ .		6		V
Low-level input voltage	V <sub>IN</sub> -L				1	V
High-level input voltage	V <sub>IN</sub> -H		2			V
Output control voltage	VCONT	VCONT = 3V *2		3.5		V
[Regulator Block]						
Output voltage	Vreg	I <sub>L</sub> = 100mA 3.05		3.3	3.55	V
Load regulation	ΔVRL	I <sub>L</sub> = 0 to 200mA	-50	0	10	mV
Line regulation	ΔVV <sub>CC</sub>	$V_{CC} = 6$ to 12V, $I_L = 100$ mA	-15	21	60	mV

Note \*1: The total current drain for  $\text{V}_{CC}\text{1}$  and  $\text{V}_{CC}\text{2}$  with no load.

- \*2: Voltage difference across the load (8 $\Omega$ ). With the outputs in the saturated state. \*3: Design guarantee value

#### **Package Dimensions**

unit: mm (typ) 3196A



#### **LA6574D**

#### **Pin Functions**

Pin No.	Pin Name	Description			
1	REV	5CH (VLO) Output change pin (REV), Logic input for loading block			
2	FWD	5CH (VLO) Output change pin (FWD), Logic input for loading block			
3	S-GND	Signal system GND			
4	VCONT	Channel 5 (VLO) output voltage control			
5	V <sub>IN</sub> 4	Input pin for channel 4			
6	V <sub>IN</sub> 4G	Input pin for channel 4 (for gain control)			
7	V <sub>CC</sub> -S	Signal system power (V <sub>CC</sub> 1 and V <sub>CC</sub> 2 short-circuited)			
8	VREF-IN	Reference voltage input pin			
9	REG-OUT	Regulator pin (External PNP collector)			
10	REG-IN	Regulator pin (External PNP base)			
11	V <sub>IN</sub> 3G	Input pin for channel 3 (for gain control)			
12	V <sub>IN</sub> 3	Input pin for channel 3			
13	V <sub>IN</sub> 2G	Input pin for channel 2 (for gain control)			
14	V <sub>IN</sub> 2	Input pin for channel 2			
15	V <sub>IN</sub> 1G	Input pin for channel 1 (for gain control)			
16	V <sub>IN</sub> 1	Input pin for channel 1			
17	V <sub>CC</sub> 1	Power for channels 1 and 2 (BTL), (V <sub>CC</sub> -S and V <sub>CC</sub> 2 short-circuited)			
18	(NC)	No connect			
19	V <sub>O</sub> 1⁻	Output pin (-) for channel 1			
20	V <sub>O</sub> 1+	Output pin (+) for channel 1			
21	V <sub>O</sub> 2-	Output pin (-) for channel 2			
22	V <sub>O</sub> 2+	Output pin (+) for channel 2			
23	P-GND	Power GND			
24	V <sub>O</sub> 3-	Output pin (-) for channel 3			
25	V <sub>O</sub> 3+	Output pin (+) for channel 3			
26	V <sub>O</sub> 4⁻	Output pin (-) for channel 4			
27	V <sub>O</sub> 4+	Output pin (+) for channel 4			
28	V <sub>O</sub> 5+	Loading output (+)			
29	V <sub>O</sub> 5 <sup>-</sup>	Loading output (-)			
30	V <sub>CC</sub> 2	Power for channels 3, 4, and 5 (V <sub>CC</sub> 1 and V <sub>CC</sub> -S short-circuited)			

<sup>\*</sup>The P-GND functions as power system GND. Set this to the minimum potential together with S-GND.

<sup>\*</sup>Short-circuit three pins of power system, V<sub>CC</sub>-S, V<sub>CC</sub>1, and V<sub>CC</sub>2, externally before use.

# **Pin Description**

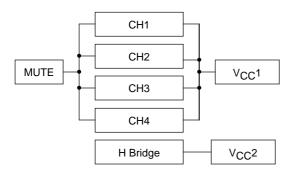
Pin No.	Symbol	Pin Name	Description	Equivalent Circuit
5	V <sub>IN</sub> 4	Input	Input pin for each channel	
6	V <sub>IN</sub> 4G			VIN 0
11	V <sub>IN</sub> 3G			V <sub>IN</sub> GO
12	$V_{IN}3$			V <sub>IN</sub> G O V <sub>CC</sub> -S
13	V <sub>IN</sub> 2G			
14	$V_{IN}^2$			
15	V <sub>IN</sub> 1G			
16	V <sub>IN</sub> 1			
				Vref O
				$igl \ igl \ igl \ \ igl \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \$
19	V <sub>O</sub> 1 <sup>-</sup>	Output	Each output	
20 21	V <sub>O</sub> 1+ V <sub>O</sub> 2⁻			
22	V <sub>O</sub> 2+			
24	V <sub>O</sub> 3⁻			<b>↓</b>
25	V <sub>O</sub> 3+			
26	V <sub>O</sub> 4⁻			OUT
27	V <sub>O</sub> 4+			
28 29	V <sub>O</sub> 5+ V <sub>O</sub> 5⁻	V <sub>O</sub> 5	H bridge output	
4	VCONT			
				<b>│</b>
				*
				Ó Ó Ó V <sub>O</sub> 5⁺ V <sub>O</sub> 5⁻ VCONT
				AO2. AO2 ACOMI
2	FWD	FWD	H bridge input	
1	REV	REV		V <sub>CC</sub> 2
				<b> </b>
				<u> </u>
				FWD
				}

## **H Bridge Block**

FWD	REV	V <sub>O</sub> 5+	V <sub>O</sub> 5-	Mode
L	L	OFF	OFF	Open *1
L	Н	Н	L	Forward
Н	L	L	Н	Reverse
Н	Н	L	L	Brake *2

<sup>\*1:</sup> Output: High impedance

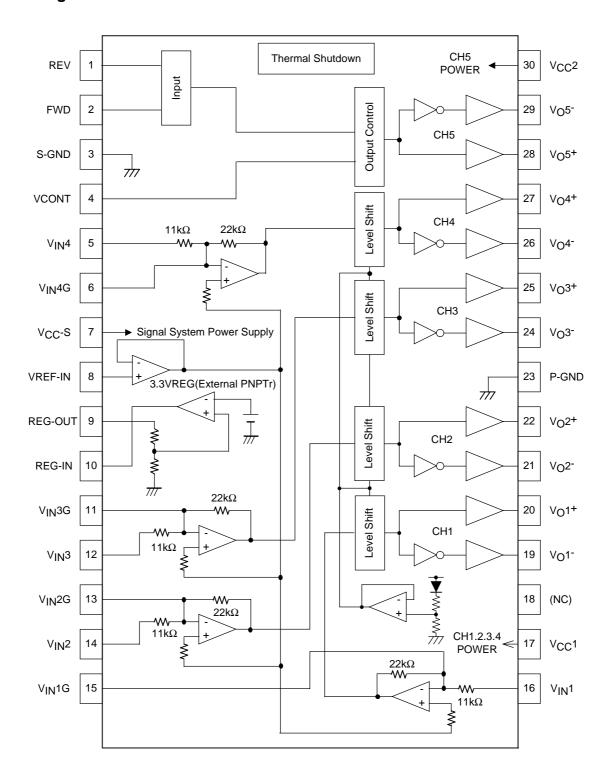
## Relationship between the MUTE pin and the power supplies (VCC\*)



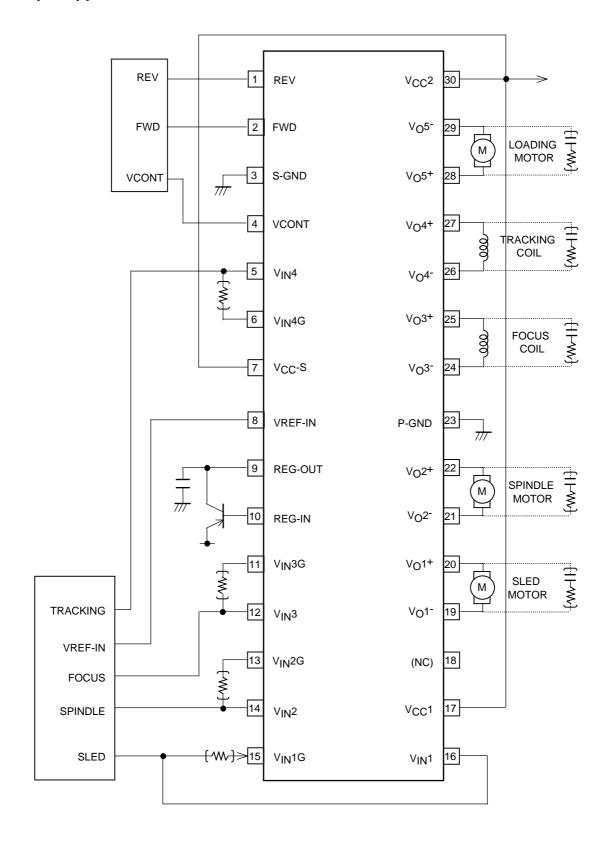
<sup>\*2:</sup> In case of braking, the SINK side transistor is turned ON (short brake). VLO+ and VLO- are approximately on the GND level.

<sup>\*3:</sup> VCONT (output voltage setting pin) and VLO have the following relationship: VLO = VCONT - 1V (typical)

#### **Block Diagram**



# **Sample Application Circuit**



- SANYO Semiconductor Co.,Ltd. assumes no responsibility for equipment failures that result from using products at values that exceed, even momentarily, rated values (such as maximum ratings, operating condition ranges, or other parameters) listed in products specifications of any and all SANYO Semiconductor Co.,Ltd. products described or contained herein.
- SANYO Semiconductor Co.,Ltd. strives to supply high-quality high-reliability products, however, any and all semiconductor products fail or malfunction with some probability. It is possible that these probabilistic failures or malfunction could give rise to accidents or events that could endanger human lives, trouble that could give rise to smoke or fire, or accidents that could cause damage to other property. When designing equipment, adopt safety measures so that these kinds of accidents or events cannot occur. Such measures include but are not limited to protective circuits and error prevention circuits for safe design, redundant design, and structural design.
- In the event that any or all SANYO Semiconductor Co.,Ltd. products described or contained herein are controlled under any of applicable local export control laws and regulations, such products may require the export license from the authorities concerned in accordance with the above law.
- No part of this publication may be reproduced or transmitted in any form or by any means, electronic or mechanical, including photocopying and recording, or any information storage or retrieval system, or otherwise, without the prior written consent of SANYO Semiconductor Co..Ltd.
- Any and all information described or contained herein are subject to change without notice due to product/technology improvement, etc. When designing equipment, refer to the "Delivery Specification" for the SANYO Semiconductor Co.,Ltd. product that you intend to use.
- Information (including circuit diagrams and circuit parameters) herein is for example only; it is not guaranteed for volume production.
- Upon using the technical information or products described herein, neither warranty nor license shall be granted with regard to intellectual property rights or any other rights of SANYO Semiconductor Co.,Ltd. or any third party. SANYO Semiconductor Co.,Ltd. shall not be liable for any claim or suits with regard to a third party's intellectual property rights which has resulted from the use of the technical information and products mentioned above.

This catalog provides information as of April, 2007. Specifications and information herein are subject to change without notice.