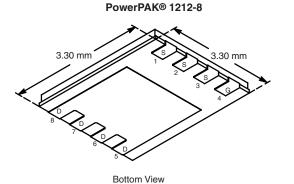


Vishay Siliconix

COMPLIANT

N-Channel 30-V (D-S) MOSFET

PRODUCT SUMMARY						
V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A) ^{a, g}	Q _g (Typ.)			
30	0.0075 at V _{GS} = 10 V	35	10.2 nC			
	0.0098 at V_{GS} = 4.5 V	35	10.2 110			

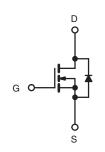


FEATURES

- Halogen-free
- TrenchFET[®] Power MOSFET
- 100 % R_q Tested
- 100 % UIS Tested

APPLICATIONS

• Synchronous Rectification



Ordering Information: Si7114ADN-T1-GE3 (Lead (Pb)-free and Halogen-free)

N-Channel MOSFET

ABSOLUTE MAXIMUM RATIN	I GS T _A = 25 °C,	unless othe	rwise noted		
Parameter		Symbol	Limit	Unit	
Drain-Source Voltage		V _{DS}	30	V	
Gate-Source Voltage		V _{GS}	± 20	V	
	T _C = 25 °C		35 ^g		
Continuous Drain Current (T 150 °C)	T _C = 70 °C	1	35 ^g		
Continuous Drain Current ($T_J = 150 \ ^{\circ}C$)	T _A = 25 °C	I _D	18 ^{b, c}	Α	
	T _A = 70 °C		14.5 ^{b, c}	A	
Pulsed Drain Current		I _{DM}	60		
Avalanche Current	L = 0.1 mH	I _{AS}	30		
Avalanche Energy		E _{AS}	45	mJ	
Continuous Source-Drain Diode Current	T _C = 25 °C	L.	32	A	
Continuous Source-Drain Diode Current	T _A = 25 °C	- I _S	3.2 ^{b, c}	A	
	T _C = 25 °C		39		
Maximum Bawar Dissinction	T _C = 70 °C	Б	25	w	
Maximum Power Dissipation	T _A = 25 °C	PD	3.7 ^{b, c}	vv	
	T _A = 70 °C		2.4 ^{b, c}		
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to 150	°C	
Soldering Recommendations (Peak Temperature) ^{d, e}			260		

THERMAL RESISTANCE RATINGS

Parameter		Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient ^{b, f}	t ≤ 10 s	R _{thJA}	26	34	°C/W	
Maximum Junction-to-Case (Drain)	Steady State	R _{thJC}	2.4	3.2	0/11	

Notes:

a. Based on $T_C = 25 \ ^{\circ}C$.

b. Surface Mounted on 1" x 1" FR4 board.

c. t = 10 s.

- d. See Solder Profile (http://www.vishay.com/ppg?73257). The PowerPAK 1212 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- e. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.
- f. Maximum under Steady State conditions is 81 °C/W.

g. Package limited.

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Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static				•			
Drain-Source Breakdown Voltage	V _{DS}	$V_{GS} = 0 \text{ V}, \text{ I}_{D} = 250 \mu\text{A}$	30			V	
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$	I _D = 250 μA		33			
V _{GS(th)} Temperature Coefficient				- 6		mV/°C	
Gate-Source Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}$, $I_D = 250 \ \mu A$	1.2		2.5	V	
Gate-Source Leakage	I _{GSS}	$V_{DS} = 0 V, V_{GS} = \pm 20 V$			± 100	nA	
Zero Gate Voltage Drain Current		$V_{DS} = 30 \text{ V}, \text{ V}_{GS} = 0 \text{ V}$			1	μΑ	
	IDSS	V_{DS} = 30 V, V_{GS} = 0 V, T_{J} = 55 °C			5		
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = 10 V, I _D = 18 A		0.0062	0.0075	- Ω	
		V _{GS} = 4.5 V, I _D = 16 A		0.0081	0.0098		
Forward Transconductance ^a	9 _{fs}	V _{DS} = 15 V, I _D = 18 A		50		S	
Dynamic ^b				•			
Input Capacitance	C _{iss}			1230		pF	
Output Capacitance	C _{oss}	V _{DS} = 15 V, V _{GS} = 0 V, f = 1 MHz		275			
Reverse Transfer Capacitance	C _{rss}			105			
T + 1 0 + 01		V _{DS} = 15 V, V _{GS} = 10 V, I _D = 19 A		21	32	nC	
Total Gate Charge	Qg			10.2	20		
Gate-Source Charge	Q _{gs}	V _{DS} = 15 V, V _{GS} = 4.5 V, I _D = 19 A		3.9			
Gate-Drain Charge	Q _{gd}			3.2			
Gate Resistance	R _g	f = 1 MHz	0.3	1.6	3.2	Ω	
Turn-On Delay Time	t _{d(on)}			20	30	ns	
Rise Time	t _r	V_{DD} = 15 V, R_{L} = 1.5 Ω		14	21		
Turn-Off Delay Time	t _{d(off)}	$\text{I}_\text{D} \cong$ 10 A, V_GEN = 4.5 V, R_g = 1 Ω		20	30		
Fall Time	t _f			10	20		
Turn-On Delay Time	t _{d(on)}			11	20		
Rise Time	t _r	V_{DD} = 15 V, R _L = 1.5 Ω		8	16		
Turn-Off Delay Time	t _{d(off)}	$I_D \cong 10$ Å, $V_{GEN} = 10$ V, $R_g = 1$ Ω		20	30		
Fall Time	t _f			7	14		
Drain-Source Body Diode Characteristic	cs				1 1		
Continuous Source-Drain Diode Current	۱ _S	T _C = 25 °C			32	۸	
Pulse Diode Forward Current	I _{SM}				60	A	
Body Diode Voltage	V _{SD}	$I_{S} = 10 \text{ A}, V_{GS} = 0 \text{ V}$		0.8	1.2	V	
Body Diode Reverse Recovery Time	t _{rr}			24	36	ns	
Body Diode Reverse Recovery Charge	Q _{rr}			20	30	nC	
Reverse Recovery Fall Time	t _a	I _F = 10 A, dl/dt = 100 A/μs, T _J = 25 °C		16		ns	
Reverse Recovery Rise Time	t _b	1		8			

Notes:

a. Pulse test; pulse width \leq 300 $\mu s,$ duty cycle \leq 2 %.

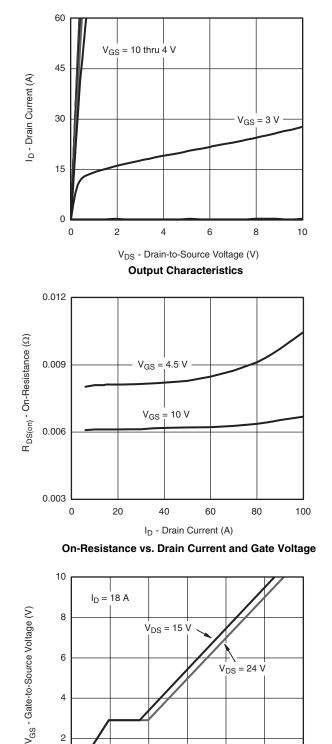
b. Guaranteed by design, not subject to production testing.

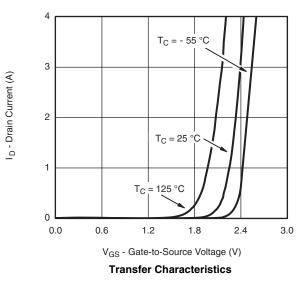
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

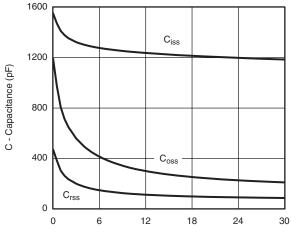


Si7114ADN Vishay Siliconix

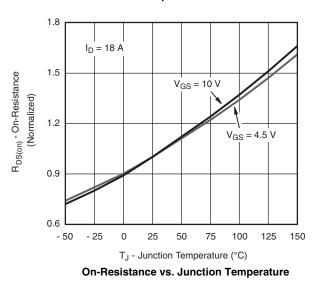
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted











Document Number: 68932 S-82616-Rev. B, 03-Nov-08

2

0

0

4

8

12

Q_q - Total Gate Charge (nC)

Gate Charge

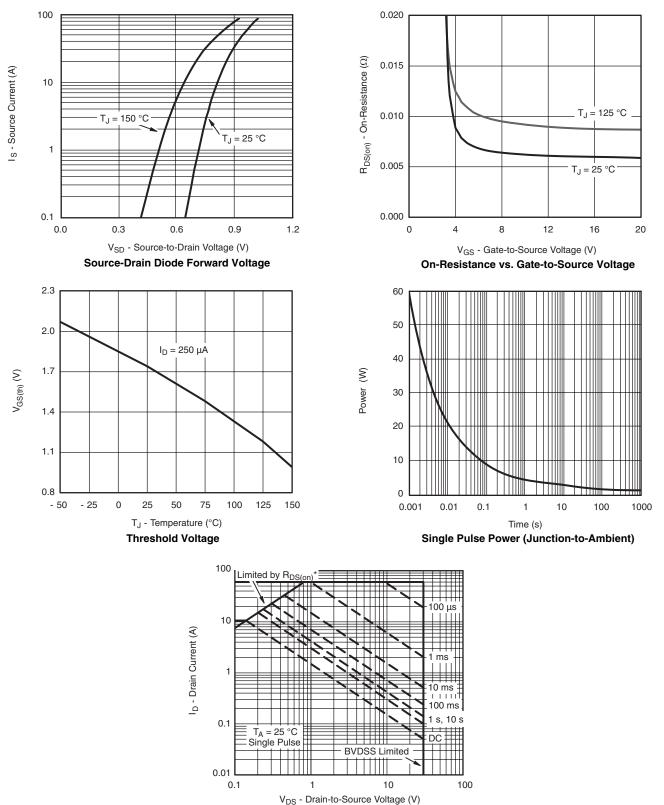
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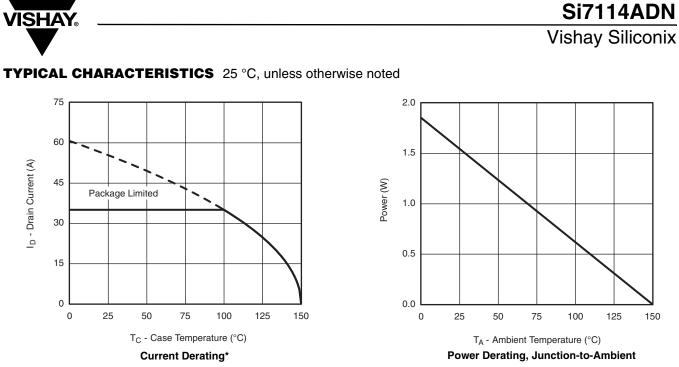
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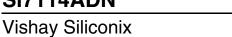




* V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified Safe Operating Area, Junction-to-Ambient **VISHAY**

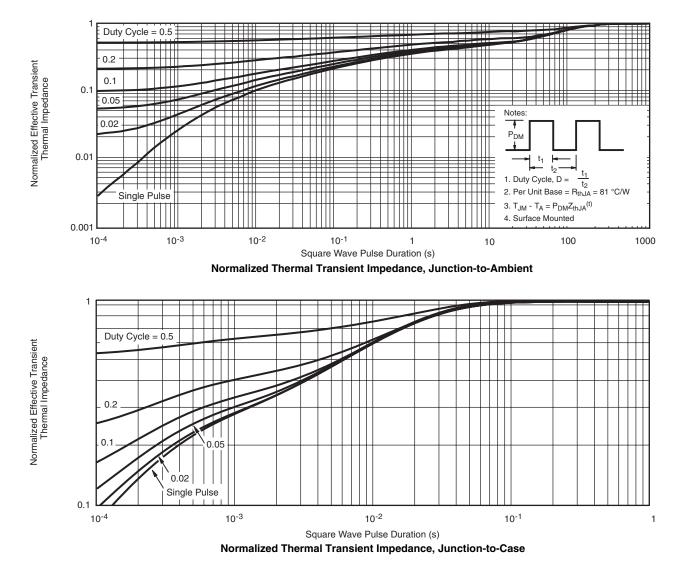


* The power dissipation P_D is based on $T_{J(max)}$ = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.





TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see http://www.vishay.com/ppg?68932.



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