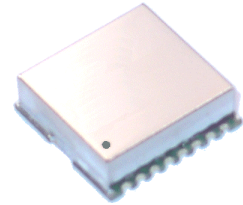


Features

- 3 dBm Output Level at 1945.3 MHz
- Channel Step Size : 1000 kHz
- 2nd Harmonic : < -25 dBc
- Spurious Level : < -70 dBc
- Lock Time : < 10 ms
- 25 mA Current Consumption

Description

The plerow™ PLL synthesizer module was designed for use in wireless and wireline systems in a wide range of frequency from 50 MHz to 6 GHz. ASB's PLL provides exceptionally low spurious and phase noise performance with fast locking time and low current consumption. All products are available in a surface-mount type package.



Specifications

Parameter	Unit	Min.	Typical	Max.
Frequency Range	MHz		1945.3	
Output Power	dBm	1	3	5
Supply Voltage	V	4.7	5	5.3
Current Consumption	mA		25	35
Channel Step Size	kHz		1000	
2 nd Harmonics	dBc		-25	-20
Spurious Level	dBc		-70	-65
Lock Time	ms		3	10
Reference Frequency	MHz		10	
Reference Input Level	dBm	-5	2	7
Phase Noise (C / N)				
@ 1 kHz	dBc/Hz		-75	-68
@ 10 kHz			-103	-100
@ 100 kHz			-120	-115
Output Impedance	Ω		50	
Operating Temp. Range	°C	-40	25	85
Package Type & Size	mm	SMT, 19.0W×19.0L×5.8H		

1) Measurement conditions are as follows: T = 25°C, V_{CC} = 5 V, Freq. = 1945.3 MHz, 50 ohm system.

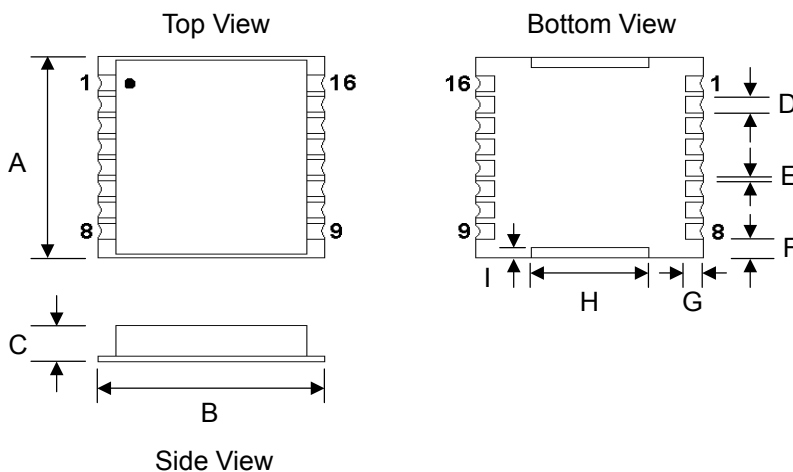
More Information

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Outline Drawing



Pin Configuration		Dimension (mm)	
1	CLOCK	A	19.0
2	DATA	B	19.0
3	ENABLE	C	5.8
4	OSC IN	D	1.5
9	VCC (VCO)	E	0.5
13	RF OUT	F	1.75
15	VCP (PLL)	G	1.35
16	LOCK DETECT	H	15.0
Others	Ground	I	0.9
		Tolerance: ± 0.2	