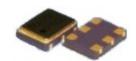


# 7 x 5 x 1.8mm 6 pad SMD





## Frequency range 0.625MHz to 50.0MHz

#### **CMOS/TTL Output**

- Supply Voltage 5.0 V or 3.3 VDC
- **Integrated Phase Jitter 1ps typical**
- Low cost unit

#### **DESCRIPTION**

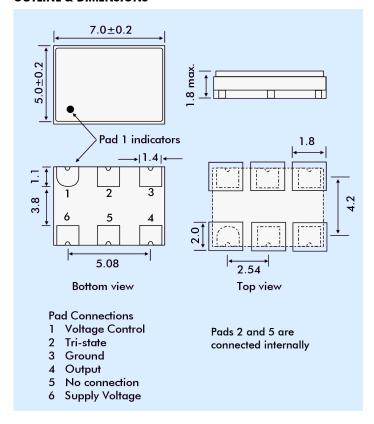
G576 VCXOs, are packaged in a miniature 7mm x 5mm x 1.8mm 6 pad SMD package. Typical phase jitter for G series VCXOs is <1 ps, output CMOS/TTL. G series VCXOs use fundamental mode crystal osccillators. Applications include phase lock loop, SONET/ATM, settop boxes, MPEG, audio/video modulation, video game consoles and HDTV.

#### **SPECIFICATION**

Frequency Range	
Vdd = +3.3VDC:	0.625MHz to 50.0MHz
Vdd = +5.0VDC:	1.0MHz to 50.0MHz
Supply Voltage:	+3.3 VDC ±5% or +5.0VDC±5%
Output Logic:	TTL/HCMOS
Integrated Phase Jitter:	1.0ps maximum 12kHz to 20MHz
Period Jitter RMS:	2.0ps typical
Period Jitter Peak to Peak:	14ps maximum
Phase Noise:	See table below
Initial Frequency Accuracy	
Tune to the nominal frequency wit	th:
+3.3VDC:	$Vc = 1.65V \pm 0.2V$
+5.0 VDC:	$Vc = 2.5V \pm 0.2V$
Output Voltage HIGH (1):	90% Vdd minimum
Output Voltage LOW (0):	10% Vdd maximum
Control Voltage Centre	
+3.3VDC:	1.65V
+5.0VDC:	2.5V
Control Voltage Range	
+3.3VDC:	0.3V to 3.0V
+5.0VDC:	0.5V to 4.5V
Pulling Range	
+3.3VDC	$\pm 80$ ppm to $\pm 120$ ppm (standard)
+5.0VDC:	±80ppm to ±150ppm
	(±200ppm available)
Temperature Stability:	
Temperature Stability: Output Load:	See table
Output Load:	See table CMOS = 15pF, TTL = 2 gates
Output Load: Start-up Time:	See table CMOS = 15pF, TTL = 2 gates 10ms maximum, 5ms typical
Output Load: Start-up Time: Duty Cycle:	See table CMOS = 15pF, TTL = 2 gates 10ms maximum, 5ms typical 50% ±5% measured at 50% Vdd
Output Load: Start-up Time: Duty Cycle: Rise/Fall Times:	See table  CMOS = 15pF, TTL = 2 gates  10ms maximum, 5ms typical  50% ±5% measured at 50% Vdd  0.7ns typical (15pF load)
Output Load: Start-up Time: Duty Cycle:	See table  CMOS = 15pF, TTL = 2 gates  10ms maximum, 5ms typical  50% ±5% measured at 50% Vdd  0.7ns typical (15pF load)  10 to 45mA, frequency
Output Load: Start-up Time: Duty Cycle: Rise/Fall Times: Current Consumption:	See table  CMOS = 15pF, TTL = 2 gates  10ms maximum, 5ms typical  50% ±5% measured at 50% Vdd  0.7ns typical (15pF load)  10 to 45mA, frequency dependent
Output Load: Start-up Time: Duty Cycle: Rise/Fall Times: Current Consumption: Linearity:	See table  CMOS = 15pF, TTL = 2 gates  10ms maximum, 5ms typical  50% ±5% measured at 50% Vdd  0.7ns typical (15pF load)  10 to 45mA, frequency dependent  10% maximum, 6% typical
Output Load: Start-up Time: Duty Cycle: Rise/Fall Times: Current Consumption: Linearity: Modulation Bandwidth:	See table  CMOS = 15pF, TTL = 2 gates  10ms maximum, 5ms typical  50% ±5% measured at 50% Vdd  0.7ns typical (15pF load)  10 to 45mA, frequency dependent  10% maximum, 6% typical  10kHz minimum
Output Load: Start-up Time: Duty Cycle: Rise/Fall Times: Current Consumption: Linearity: Modulation Bandwidth: Input Impedance:	See table  CMOS = 15pF, TTL = 2 gates  10ms maximum, 5ms typical  50% ±5% measured at 50% Vdd  0.7ns typical (15pF load)  10 to 45mA, frequency dependent  10% maximum, 6% typical  10kHz minimum  1 MΩ minimum
Output Load: Start-up Time: Duty Cycle: Rise/Fall Times: Current Consumption: Linearity: Modulation Bandwidth: Input Impedance: Slope Polarity:	See table  CMOS = 15pF, TTL = 2 gates  10ms maximum, 5ms typical  50% ±5% measured at 50% Vdd  0.7ns typical (15pF load)  10 to 45mA, frequency dependent  10% maximum, 6% typical  10kHz minimum  1 MΩ minimum  Monotonic and Positive. (An
Output Load: Start-up Time: Duty Cycle: Rise/Fall Times: Current Consumption: Linearity: Modulation Bandwidth: Input Impedance:	See table  CMOS = 15pF, TTL = 2 gates  10ms maximum, 5ms typical  50% ±5% measured at 50% Vdd  0.7ns typical (15pF load)  10 to 45mA, frequency dependent  10% maximum, 6% typical  10kHz minimum  1 MΩ minimum  Monotonic and Positive. (An increase of control voltage
Output Load: Start-up Time: Duty Cycle: Rise/Fall Times: Current Consumption: Linearity: Modulation Bandwidth: Input Impedance: Slope Polarity:	See table CMOS = 15pF, TTL = 2 gates 10ms maximum, 5ms typical 50% ±5% measured at 50% Vdd 0.7ns typical (15pF load) 10 to 45mA, frequency dependent 10% maximum, 6% typical 10kHz minimum 1 MΩ minimum Monotonic and Positive. (An increase of control voltage always increases output
Output Load: Start-up Time: Duty Cycle: Rise/Fall Times: Current Consumption: Linearity: Modulation Bandwidth: Input Impedance: Slope Polarity: (Transfer function)	See table  CMOS = 15pF, TTL = 2 gates  10ms maximum, 5ms typical  50% ±5% measured at 50% Vdd  0.7ns typical (15pF load)  10 to 45mA, frequency dependent  10% maximum, 6% typical  10kHz minimum  1 M\Omega minimum  Monotonic and Positive. (An increase of control voltage always increases output frequency.)
Output Load: Start-up Time: Duty Cycle: Rise/Fall Times: Current Consumption: Linearity: Modulation Bandwidth: Input Impedance: Slope Polarity: (Transfer function) Storage Temperature:	See table CMOS = 15pF, TTL = 2 gates 10ms maximum, 5ms typical 50% ±5% measured at 50% Vdd 0.7ns typical (15pF load) 10 to 45mA, frequency dependent 10% maximum, 6% typical 10kHz minimum 1 MΩ minimum Monotonic and Positive. (An increase of control voltage always increases output frequency.) -50° to +100°C
Output Load: Start-up Time: Duty Cycle: Rise/Fall Times: Current Consumption: Linearity: Modulation Bandwidth: Input Impedance: Slope Polarity: (Transfer function)	See table  CMOS = 15pF, TTL = 2 gates  10ms maximum, 5ms typical  50% ±5% measured at 50% Vdd  0.7ns typical (15pF load)  10 to 45mA, frequency dependent  10% maximum, 6% typical  10kHz minimum  1 M\Omega minimum  Monotonic and Positive. (An increase of control voltage always increases output frequency.)

PHASE NOISE		
Offset	Frequency 27.0MHz	
10Hz	-70dBc/Hz	
100Hz	-105dBc/Hz	
1kHz	-132dBc/Hz	
10kHz	-142dBc/Hz	
1MHz	-150dBc/Hz	

#### **OUTLINE & DIMENSIONS**



### **FREQUENCY STABILITY**

Stability Code	Stability ±ppm	Temp. Range
Α	25	0°∼+70°C
В	50	0°~+70°C
С	100	0°∼+70°C
D	25	-40°∼+85°C
E	50	-40°~+85°C
F	100	-40°~+85°C
16 . 1 . 6		

If non-standard frequency stability is required Use 'I' followed by stability, i.e. I20 for ±20ppm

# **PART NUMBERING**

