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SANYO Semiconductors
DATA SHEET

LC07422T — CMOS IC
Audio CODEC with Video Driver

Overview

The LC07422T is an audio CODEC that has a built-in speaker amplifier and headphone amplifier and incorporates a video driver.

A 2-input line selector and ALC circuit are provided in the audio recording system.

A speaker amplifier with EVR, headphone amplifier, and line output are provided in the playback system. A video driver that obviates the need for an output coupling capacitor is also included to enable AV playback processing with the single chip.

Features

- Audio systems can be configured using this single chip since almost all the audio system circuits are provided.
- A video driver obviating the need for an output coupling capacitor is included.
- A high-performance ALC/limiter circuit that meets a variety of different conditions is incorporated.
- A wide range of different functions can be set using parameter settings.

Functions

- The input signals for the speaker amplifier and headphone amplifier can be selected (DAC or PGA output).
- Power-down control of individual function block and be exercised.
- COCEC
  ADC for the digital recording of analog input signals
  DAC for outputting analog signals from the digital playback data
- De-emphasis filter
- When Y/C video signals are input, composite signals can be generated, and 3-system driver signals can be output.

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LC07422T

Main Circuits

- Line selector   : 2 stereo inputs
- ALC/Limiter   : 1 stereo circuit
- EVR (analog volume)   : 1 stereo circuit
- $\Delta\Sigma$ type 16bit ADC/DAC : 1 stereo circuit
- Headphone amplifier   : 1 stereo circuit
- Speaker amplifier   : 1 stereo circuit
- Video driver   : 3 circuits (Y,C,V)
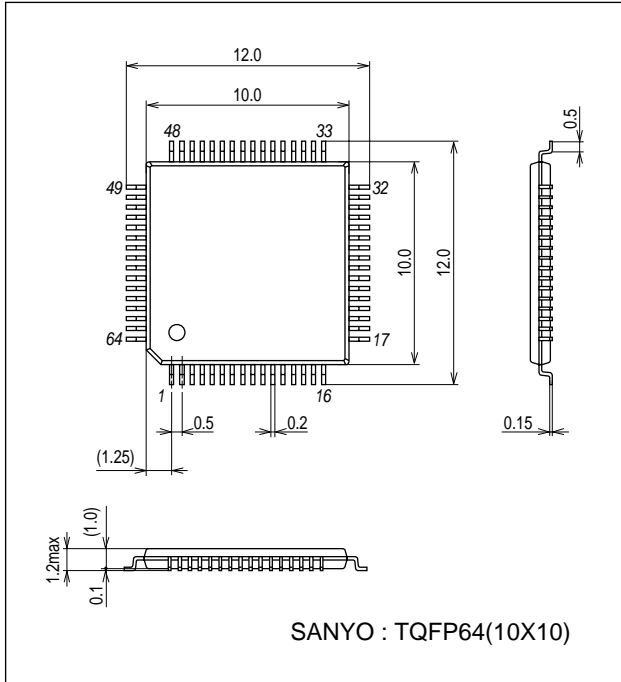
Power Supply Voltage

V_{DD}(digital) = 2.8V(2.6 to 3.2V)
V_{DD}io(digital IO) = 1.8V(1.71 to 3.2V)
V_{DD}ana(analog) = 2.8V(2.6 to 3.2V)
V_{DD}sp(speaker) = 2.8V(2.6 to 3.2V)
V_{DD}h1,V_{DD}h2(analog) = 4.8V(4.5 to 5.5V)
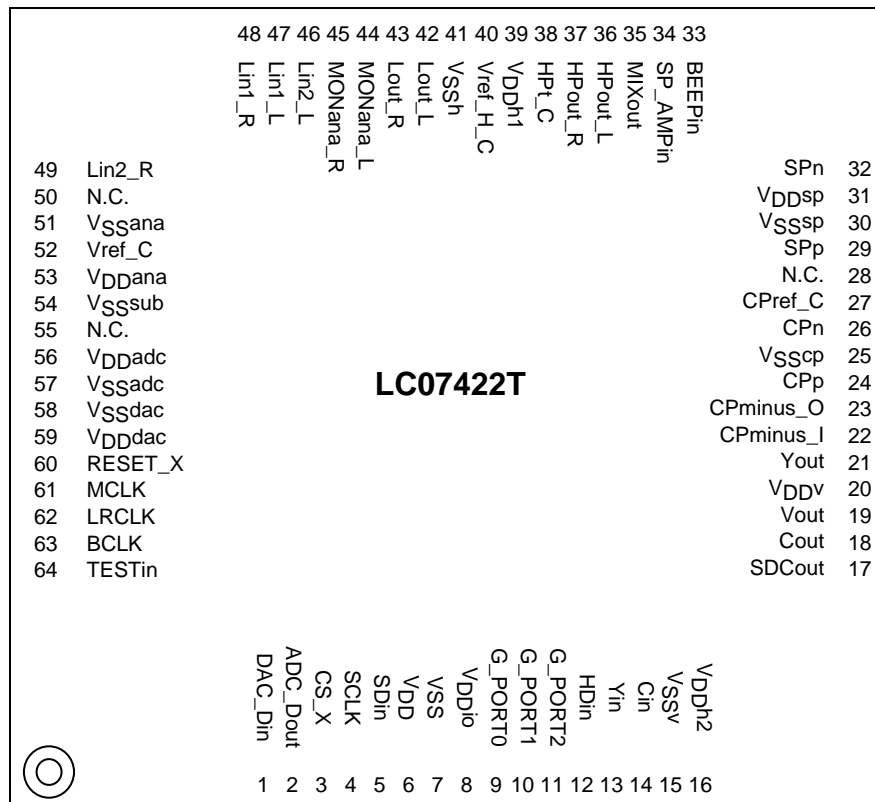V_{DD}v(video) = 2.8V(2.6 to 3.2V)

Package Dimensions

unit : mm (typ)
3296

SANYO : TQFP64(10X10)

Pin Assignment

Top view

LC07422T

Pin Description

(Note) I/O: I=> input, Is=> Schmitt input, O=> output, IOs=> input/output

| PIN No.	I/O	Pin Name	Description
Digital System			
60	Is	RESET_X	Reset (negative polarity)
61	I	MCLK	Master Clock
62	IOs	LRCLK	LR Clock (sample rate clock) Audio IF
63	IOs	BCLK	B Clock (serial data bit clock) Audio IF
64	I	TESTin	For IC testing (V_{SS} fixed in normal operation)
1	Is	DAC_Din	DAC serial data input Audio IF
2	O	ADC_Dout	ADC serial data output Audio IF
3	Is	CS_X	Chip select (negative polarity) Microcontroller IF
4	Is	SCLK	Serial clock Microcontroller IF
5	Is	SDin	Serial data input Microcontroller IF
9	IOs	G_PORT0	For IC testing (open in normal operation)
10	IOs	G_PORT1	For IC testing (open in normal operation)
11	IOs	G_PORT2	For IC testing (open in normal operation)
12	Is	HDin	HD signal pulse input (for test / Y signal clamp)
6	-	V_{DD}	Digital power supply
7	-	V_{SS}	Digital ground
8	-	$V_{DD}io$	Digital IO power supply
Analog system			
13	I	Yin	Y signal input
14	I	Cin	C signal input
17	O	SDCout	DC output for SDC signal
18	O	Cout	C signal output
19	O	Vout	Video signal output
21	O	Yout	Y signal output
22	I	CPminus_I	Connect to CPminus O pin
23	O	CPminus_O	Reference voltage (minus) Connect an external capacitor
24	IO	CPp	Charge pump pin Connect an external capacitor
26	IO	CPn	Charge pump pin Connect an external capacitor
27	O	CPref_C	Reference voltage Connect an external capacitor
29		SPp	Speaker output
32		SPn	Speaker output
33	I	BEEPin	BEEP signal input
34	I	SP_AMPin	Speaker amplifier input
35	O	MIXout	Mixing circuit (L+R) output
36	O	HPout_L	Headphone output, Left channel
37	O	HPout_R	Headphone output, Right channel
38	O	HPt_C	Time constant setting Connect an external capacitor
40	O	Vref_H_C	Reference voltage (4.8V system) Connect an external capacitor
42	O	Lout_L	Line output, Left channel
43	O	Lout_R	Line output, Right channel
44	O	MONana_L	For IC testing (open in normal operation)

Continued from preceding page.

PIN No.	I/O	Pin Name	Description
Analog system			
45	O	MONana_R	For IC testing (open in normal operation)
46	I	Lin2_L	Line input, Left channel 2
47	I	Lin1_L	Line input, Left channel 1
48	I	Lin1_R	Line input, Right channel 1
49	I	Lin2_R	Line input, Right channel 2
52	O	Vref_C	Reference voltage (2.8V system) Connect an external capacitor
15	-	$V_{SS}v$	Analog ground for video driver
16	-	$V_{DD}h2$	4.8V system analog power supply (for SDC circuit)
20	-	$V_{DD}v$	Analog power supply for video driver
25	-	$V_{SS}cp$	Ground for charge pump
30	-	$V_{SS}sp$	Speaker analog ground
31	-	$V_{DD}sp$	Speaker analog power supply
39	-	$V_{DD}h1$	4.8V system analog power supply
41	-	$V_{SS}h$	4.8V system analog ground
51	-	$V_{SS}ana$	Analog ground
53	-	$V_{DD}ana$	Analog power supply
54	-	$V_{SS}sub$	Ground
56	-	$V_{DD}adc$	ADC analog power supply
57	-	$V_{SS}adc$	ADC analog ground
58	-	$V_{SS}dac$	DAC analog ground
59	-	$V_{DD}dac$	DAC analog power supply

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Block Diagram
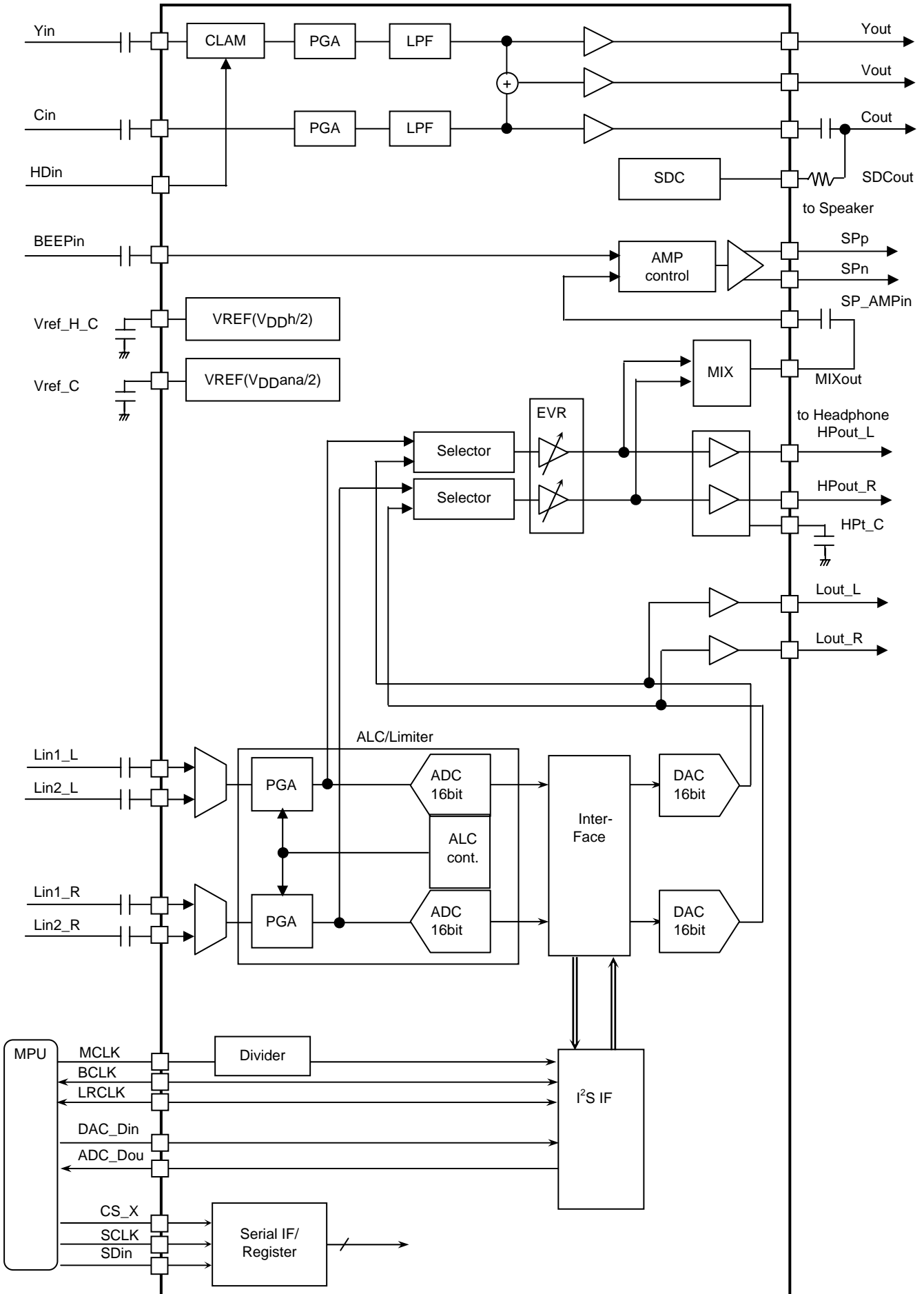
General specifications (* fs = sampling frequency)

Audio block

- $\Delta\Sigma$ type 16-bit stereo ADC : THD+N = 80dB (typ, with -1dBfs input)
- $\Delta\Sigma$ type 16-bit stereo DAC : THD+N = 80dB (typ, with 0dBfs input)
- PGA for ALC/limiter : Amplifier gain => +34 to -14dB (in 0.5dB steps)
- EVR (analog volume) : Amplifier gain => 0 to -65dB
  (The gain can be varied in steps from approx. 0.1 to 3.0dB; see characteristics diagram.)
- Line output : Built-in pop noise suppression circuit
- Speaker amplifier (monaural) : BTL drive, 250mW (3dBV, V_{DD} = 2.8V, 8Ω, THD+N = 1%)
- Headphone amplifier : Output level => 2dBV (typ, 108Ω, V_{DD}h = 4.8V)
- Sampling frequency : 48, 32kHz (44.1kHz supported by DAC only)
- Audio data format
 I^2S, left justification, right justification, BCLK: 64fs, 32fs, master/slave mode

Video block

- No need for output coupling capacitor, no generation of V sag
- LPF : fc = 8MHz
- Amplifier gain : 6.5dB±1.7dB, 0.1dB/step
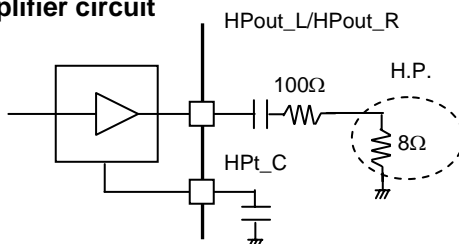- 75Ω driver : 3 systems (Y, C, V)

Common units

- Master clock (MCLK pin input) : 256fs or 512fs, duty ratio = 50% (typ)
- Microcontroller serial data format (register settings) : 3-line system
  (Chip select, clock, data)
  The maximum clock frequency is (1/4) MCLK.

Video driver circuit

[xxxx]: Resister setting

[VD_SDC_SW]	SDCout
11	Hi-Z
10	V_{DD}h
01	2.3V
00	0.0V
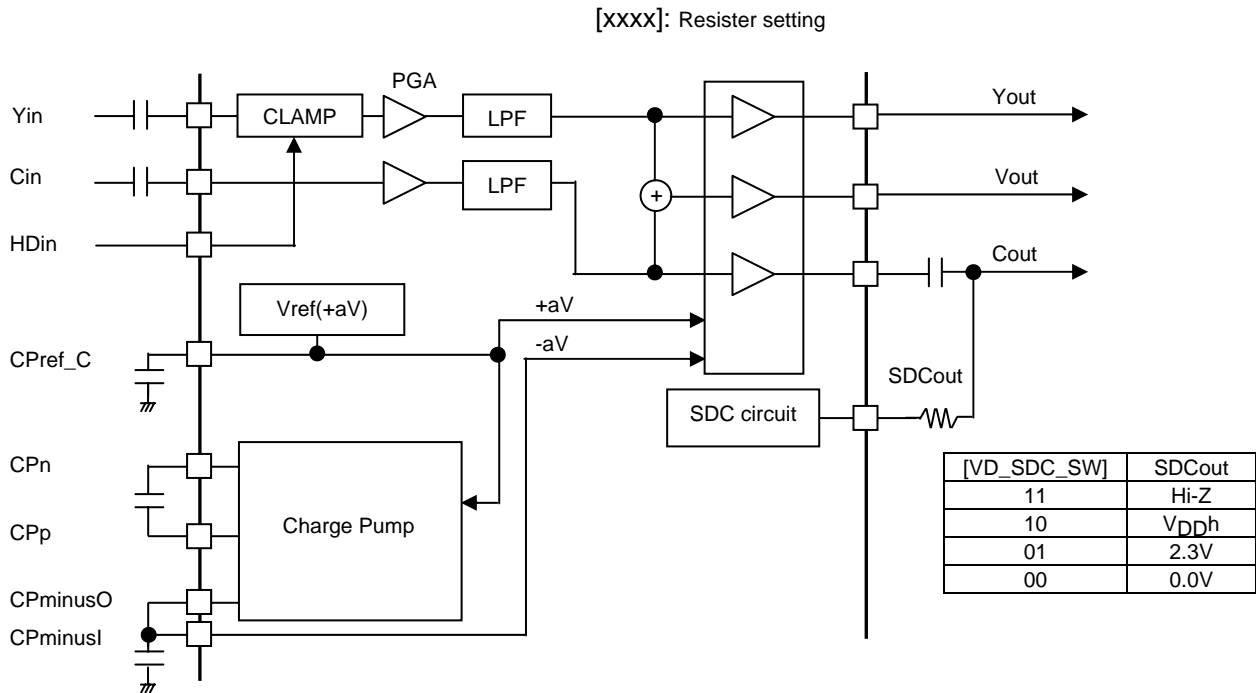
Headphone amplifier circuit

Outline of operation

1. System reset/power-down

When the RESET_X pin is set to "V_{SS}," the system is reset, and all the circuits go into the power-down mode. After the power is turned on, perform this operation once without fail.

When the system is reset, the contents of the register are initialized. (See register tables.)

For the subsequent startup of each function, refer to the section "Control/start/stop sequence for reducing pop noise."

2. ALC

When the ALC is active, the PGA (programmable gain amplifier) gain value is automatically adjusted so that the audio level becomes the preset value. The PGA gain can be adjusted in a range from +34 to -14dB.

By limiting the gain adjustment range to 0 to -14dB, this adjustment function can be made to work as a limiter function.

The ALC operation can be stopped by a register setting. The ALC is then placed in the manual mode, and the PGA gain is adjusted by the register setting. For details, refer to the section "Description of ALC/limiter operation."

3. A/D converter

The A/D converter converts the analog PGA output signals into digital data, and the digital data is then output as 16-bit serial audio data.

There are three formats supported: I^2S, left justification and right justification.

The A/D converter incorporates a high-pass filter for canceling DC offset.

The analog input range of the ADC is $0.6V_{DD}$adc. When V_{DD}adc is 2.8V, 0dBfs is 1.68V.

4. D/A converter

The D/A converter converts the digital 16-bit serial audio data into analog signals.

There are three formats supported: I^2S, left justification and right justification.

The D/A converter incorporates a high-pass filter for canceling DC offset.

The analog input range of the ADC is $0.6V_{DD}$adc. When V_{DD}adc is 2.8V, 0dBfs is 1.68V.

5. EVR

This is an analog EVR. The gain can be set within a range from 0 dB to -65dB or mute (adjustable in steps). It is incorporated in the headphone and speaker amplifier path so that the output level of the headphones and speaker can be controlled separately from the line-out output.

6. Selector

This selector is for selecting either the DAC or PGA output of the ALC. When the DAC output has been selected, the DAC output signals are output as the speaker amplifier and headphone amplifier output signals. When the PGA output has been selected, the signals from line input are all turned into analog signals to become the speaker amplifier and headphone amplifier output signals.

7. MIX

This is the mixing circuit for the left- and right-channel audio signals. In other words, this functions as a monaural signal generator circuit to provide a monaural speaker amplifier input. The left- and right-channel signals are mixed on a 1:1 basis and then output through the -2dB amplifier.

If the left- and right-channel signals are identical, the total gain becomes 4dB (= 6dB(doubled) -2dB).

8. SP AMP

This is the monaural speaker amplifier. Its maximum output is 250mW (typ V_{DD}=2.8V, 8Ω, THD+N = 10%).

Inputs to the amplifier are the audio signal SP_AMPin pin and BEEPin pin signals.

For the BEEPin pin signal, the mixing can be set ON or OFF, and the gain level can be selected (from –21 to –12dB).

A thermal shutdown function is provided. When it is left enabled, the speaker amplifier operation is automatically shut down when the chip temperature has reached a high level.

9. Video driver

Negative power is generated by the charge pump circuit and supplied to the video driver. Therefore, the video driver operates on the positive and negative power supplies.
The video signals are output with no DC components for the ground reference. As a result, with 75Ω termination, there is no need for an output coupling capacitor.
In principle, no V sag is generated.

10. Register settings

This is a 3-line system serial control circuit. The three lines are CS_X (Chip Select/low active), SCLK (Serial Clock) and SDin (Serial Data). Data can only be written into the register: The register data cannot be read out.
The data transfer rate—in other words, the maximum SCLK frequency—depends on the MCLK pin clock. For details, refer to the section "Switching characteristics."

11. Master clock

The master clock frequency is 256fs. This clock signal must be input from the MCLK pin.
A frequency divider (1/2) incorporated so an input with a frequency of 512fs can also be supplied.

12. Audio data formats

I^2S, left justification and right justification modes are supported. It is possible to select master or slave mode for BCLK and LRCLK. For details, refer to the section "Audio data formats."

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Register Table

ADRS(Address): displayed in hexadecimal notation, Init (initial value): displayed in hexadecimal notation

"0" settings are used for registers indicated with "0". The shaded registers are for IC chip testing. Their initial values are fixed. Data must be set in all the registers.

(The TEST1-8 addresses, including the registers for test purposes, are set in the sequence of 16 h to 1 Dh.)

Function	ADRS [7:0]	INIT	Register Data D[7:0]							
			7	6	5	4	3	2	1	0
PM1	00h	00h	VREF_BIAS[1]	VREF_BIAS[0]	SYNC_CLR	SEL_PDX	ALC_PDX	ADC_A_PDX	DAC_A_PDX	VIDEO_PDX
PM2	01h	00h	SP_OUTEN	SP_PDX	MIX_PDX	HP_PDX	LO_PDX	ADC_D_PDX	DAC_D_PDX	EVR_PDX
ALC1	02h	11h	0	0	LI_SEL_L[2]	LI_SEL_L[1]	0	0	LI_SEL_R[2]	LI_SEL_R[1]
ALC2	03h	3Dh	ALC_VAL[2]	ALC_VAL[1]	ALC_VAL[0]	ALC_FA[1]	ALC_FA[0]	ALC_FR[2]	ALC_FR[1]	ALC_FR[0]
ALC3	04h	86h	ALC_ZCD	ALC_ZCDTM[1]	ALC_ZCDTM[0]	ALC_FULLEN	ALC_ATLIM[1]	ALC_ATLIM[0]	ALC_RWT[1]	ALC_RWT[0]
ALC4	05h	0Eh	ALC_OFF	ALC_VMAX[6]	ALC_VMAX[5]	ALC_VMAX[4]	ALC_VMAX[3]	ALC_VMAX[2]	ALC_VMAX[1]	ALC_VMAX[0]
ALC5	06h	0Eh	ALC_MUTE_L	ALC_DVL[6]	ALC_DVL[5]	ALC_DVL[4]	ALC_DVL[3]	ALC_DVL[2]	ALC_DVL[1]	ALC_DVL[0]
ALC6	07h	0Eh	ALC_MUTE_R	ALC_DVR[6]	ALC_DVR[5]	ALC_DVR[4]	ALC_DVR[3]	ALC_DVR[2]	ALC_DVR[1]	ALC_DVR[0]
TEST0	08h	04h	TEST0[7]	TEST0[6]	TEST0[5]	TEST0[4]	TEST0[3]	TEST0[2]	TEST0[1]	TEST0[0]
CODEC1	09h	00h	0	0	0	ADF_BCLK	MCLK_DIV[1]	MCLK_DIV[0]	ADF_MODE[1]	ADF_MODE[0]
CODEC2	0Ah	00h	DAC_INV	ADC_INV	0	DE_EN	ADF_FS[1]	ADF_FS[0]	ADF_LB	ADF_MASTER
SEL/MIX	0Bh	A3h	SEL_L[1]	SEL_L[0]	SEL_R[1]	SEL_R[0]	0	0	MIX_MONO[1]	MIX_MONO[0]
EVR1	0Ch	80h	EVR_MUTE_L	0	EVR_GAIN_L[5]	EVR_GAIN_L[4]	EVR_GAIN_L[3]	EVR_GAIN_L[2]	EVR_GAIN_L[1]	EVR_GAIN_L[0]
EVR2	0Dh	80h	EVR_MUTE_R	0	EVR_GAIN_R[5]	EVR_GAIN_R[4]	EVR_GAIN_R[3]	EVR_GAIN_R[2]	EVR_GAIN_R[1]	EVR_GAIN_R[0]
EVR3	0Eh	2Eh	0	0	EVR_ZCD	EVR_ZCDTM[1]	EVR_ZCDTM[0]	EVR_SOFTSW	EVR_SSC[1]	EVR_SSC[0]
LINE	0Fh	0Bh	0	0	0	0	LO_GAIN[1]	LO_GAIN[0]	LO_VREFSW	LO_MUTE
HP	10h	01h	0	0	0	0	0	HP_PDNHIZ	HP_REFEN	HP_MUTE
SPK	11h	18h	SP_EXTBP_EN	SP_EXTBP_G[1]	SP_EXTBP_G[0]	SP_TSD_EN	SP_IDL[1]	SP_IDL[0]	SP_BIAS[1]	SP_BIAS[0]
VIDEO1	12h	11h	0	0	VD_Y_GAIN[5]	VD_Y_GAIN[4]	VD_Y_GAIN[3]	VD_Y_GAIN[2]	VD_Y_GAIN[1]	VD_Y_GAIN[0]
VIDEO2	13h	11h	0	0	VD_C_GAIN[5]	VD_C_GAIN[4]	VD_C_GAIN[3]	VD_C_GAIN[2]	VD_C_GAIN[1]	VD_C_GAIN[0]
VIDEO3	14h	30h	0	0	VD_SDC_SW[1]	VD_SDC_SW[0]	0	0	VD_V_EN	VD_YC_EN
VIDEO4	15h	56h	0	VD_CP_CLK[2]	VD_CP_CLK[1]	VD_CP_CLK[0]	0	VD_CLP_W	VD_CLP_POS	VD_TEST_CLP
TEST1	16h	00h	TEST1[7]	TEST1[6]	TEST1[5]	TEST1[4]	TEST1[3]	TEST1[2]	TEST1[1]	TEST1[0]
TEST2	17h	00h	TEST2[7]	TEST2[6]	TEST2[5]	TEST2[4]	TEST2[3]	TEST2[2]	TEST2[1]	TEST2[0]
TEST3	18h	00h	TEST3[7]	TEST3[6]	TEST3[5]	TEST3[4]	TEST3[3]	TEST3[2]	TEST3[1]	TEST3[0]
TEST4	19h	04h	TEST4[7]	TEST4[6]	TEST4[5]	TEST4[4]	TEST4[3]	TEST4[2]	TEST4[1]	TEST4[0]
TEST5	1Ah	00h	TEST5[7]	TEST5[6]	TEST5[5]	TEST5[4]	TEST5[3]	TEST5[2]	TEST5[1]	TEST5[0]
TEST6	1Bh	00h	TEST6[7]	TEST6[6]	TEST6[5]	TEST6[4]	TEST6[3]	TEST6[2]	TEST6[1]	TEST6[0]
TEST7	1Ch	01h	TEST7[7]	TEST7[6]	TEST7[5]	TEST7[4]	TEST7[3]	TEST7[2]	TEST7[1]	TEST7[0]
TEST8	1Dh	00h	TEST8[7]	TEST8[6]	TEST8[5]	TEST8[4]	TEST8[3]	TEST8[2]	TEST8[1]	TEST8[0]

ADRS	=Address	PGA	=Programmable Gain Amplifier
INIT	=Initial value	Lch	=Left channel
PM	=Power Management	Rch	=Right channel
ALC	=Automatic Level Control	2^n	=2^n (ex. 2^{10} = 1024)
ADC	=AD Converter	Nh	= N denotes a hexadecimal number.
DAC	=DA Converter	Nb	= N denotes a binary number.
EVR	=Electronic Variable Resistor	ABC[n]	= Register with a multiple number of bits.
ADF	=Audio Data Format		ABC is the register name, and "n" is the number of bits.

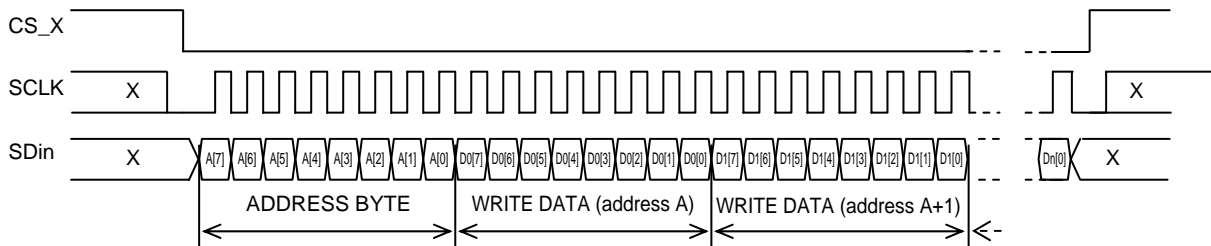## Microcontroller Serial Interface

The internal registers values are written by the serial interface consisting of the three CS_X, SCLK, and SDin lines. When the CS_X pin is set low, the LC07422T is switched into the mode that enables operation. The data is received on a byte basis with MSB first. Continuous access (burst access) is also possible, and the addresses incremented by 1 are accessed in sequence with each byte following access to the register specified by the address byte.

If the size of data exceeding the highest address (1D) is accessed in this process, the data concerned is treated as invalid. In other word, the address never wraps around to 00 (HEX). The maximum data transfer rate (maximum SCLK frequency) depends on the MCLK pin clock. Refer to the section "Switching characteristics."

- Transferring data to one address: Data (D) is written in address (A)

A[7:0]   : Designated address
D[7:0]   : Register data
X   : Invalid
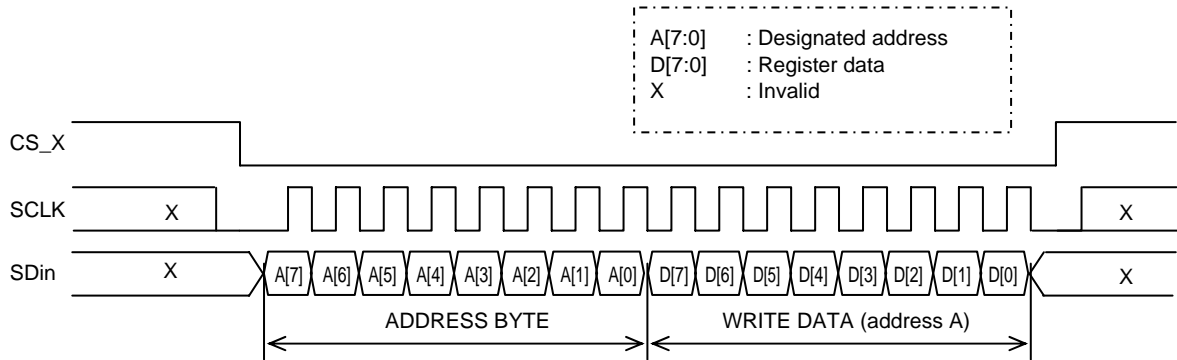
- Transferring data to contiguous addresses: Data (D0) is written in address (A),
  and data (D1) is written into address (A+1).

This catalog provides information as of October, 2007. Specifications and information herein are subject to change without notice.