CBT3126

Quad FET bus switch

Rev. 03 — 9 December 2008 Product data sheet

1. General description

The CBT3126 is a quad FET bus switch with independent line switches. Each switch is disabled when the associated Output Enable (OE) input is LOW.

The CBT3126 is characterized for operation from –40 °C to +85 °C.

2. Features

- Standard ’126-type pinout
- Multiple package options
- 5 Ω switch connection between two ports
- TTL-compatible input levels
- Minimal propagation delay through the switch
- Latch-up protection exceeds 500 mA per JEDEC standard JESD78 class II level A
- ESD protection:
  - HBM JESD22-A114E exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
  - CDM JESD22-C101C exceeds 1000 V
- Specified from –40 °C to +85 °C

3. Ordering information

Table 1. Ordering information

Type number	Temperature range	Package		
		Name	Description	Version
CBT3126D	–40 °C to +85 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
CBT3126DB	–40 °C to +85 °C	SSOP14	plastic shrink small outline package; 14 leads; body width 5.3 mm	SOT337-1
CBT3126PW	–40 °C to +85 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
CBT3126DS	–40 °C to +85 °C	SSOP16[1]	plastic shrink small outline package; 16 leads; body width 3.9 mm; lead pitch 0.635 mm	SOT519-1

[1] Also known as QSOP16.

4. Functional diagram

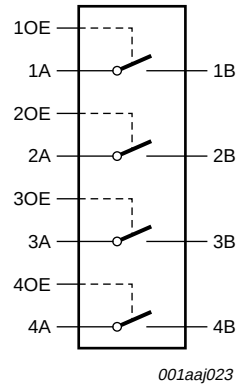
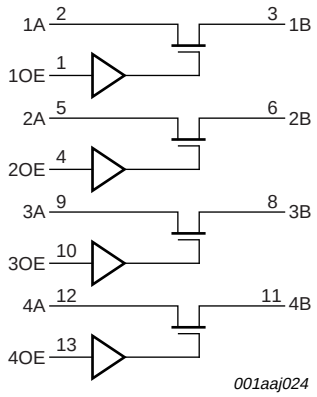


Fig 1. Logic symbol



Pin numbers are for the 14 pin packages.

Fig 2. Logic diagram

5. Pinning information

5.1 Pinning

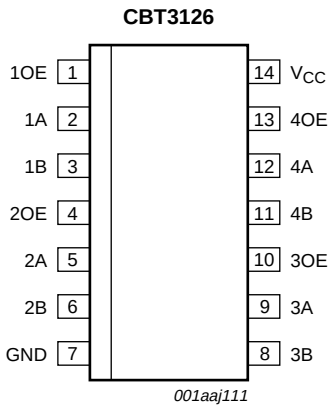


Fig 3. Pin configuration SOT108-1 (SO14)

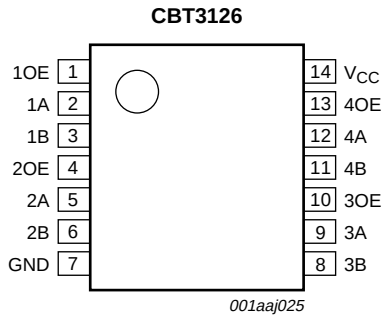


Fig 4. Pin configuration SOT337-1 (SSOP14) and SOT402-1 (TSSOP14)

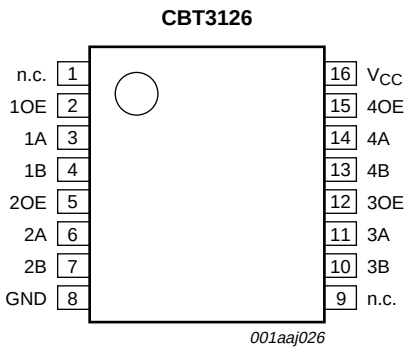


Fig 5. Pin configuration SOT519-1 (SSOP16)

5.2 Pin description

Table 2. Pin description

Symbol	Pin		Description
	SOT108-1 SOT337-1 and SOT402-1	SOT519-1	
1OE to 4OE	1, 4, 10, 13	2, 5, 12, 15	output enable input
1A to 4A,	2, 5, 9, 12	3, 6, 11, 14	A input/output
1B to 4B	3, 6, 8, 11	4, 7, 10, 13	B output/input

Table 2. Pin description *...continued*

Symbol	Pin		Description
	SOT108-1 SOT337-1 and SOT402-1	SOT519-1	
GND	7	8	ground (0 V)
V_{CC}	14	16	positive supply voltage
n.c.	-	1, 9	not connected

6. Functional description

Table 3. Function selection

H = HIGH voltage level; L = LOW voltage level.

Inputs	Switch
nOE	
L	nA to nB disconnected
H	nA to nB connected

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			–0.5	+7.0	V
V_I	input voltage		[1]	–0.5	+7.0	V
I_{CC}	supply current	continuous current through each V_{CC} or GND pin		-	128	mA
I_{IK}	input clamping current	$V_I < 0$ V		–50	-	mA
T_{stg}	storage temperature			–65	+150	°C
P_{tot}	total power dissipation	T_{amb} = –40 °C to +125 °C	[2]			
		SO14 package	[3]	-	500	mW
		SSOP14 and SSOP16 package	[4]	-	500	mW
		TSSOP14 package	[4]	-	500	mW

[1] The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

[2] The package thermal impedance is calculated from JESD51-7.

[3] For SO14 package; P_{tot} derates linearly with 8 mW/K above 70 °C.

[4] For SSOP14, SSOP16 and TSSOP14 packages; P_{tot} derates linearly with 5.5 mW/K above 70 °C.

8. Recommended operating conditions

Table 5. Operating conditions

All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		4.5	5.5	V
V_{IH}	HIGH-level input voltage		2.0	-	V
V_{IL}	LOW-level input voltage		-	0.8	V
T_{amb}	ambient temperature	operating in free-air	–40	+85	°C

9. Static characteristics

Table 6. Static characteristics

T_{amb} = –40 °C to +85 °C.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
V_{IK}	input clamping voltage	V_{CC} = 4.5 V; I_I = –18 mA		-	-	–1.2	V
V_{pass}	pass voltage	V_I = V_{CC} = 5.0 V; I_O = –100 µA		-	3.8	-	V
I_I	input leakage current	V_{CC} = 5.5 V; V_I = GND or 5.5 V		-	-	±1	µA
I_{CC}	supply current	V_{CC} = 5.5 V; I_O = 0 mA; V_I = V_{CC} or GND		-	-	3	µA
ΔI_{CC}	additional supply current	control pins; per input; V_{CC} = 5.5 V; one input at 3.4 V, other inputs at V_{CC} or GND	[2]	-	-	2.5	mA
C_I	input capacitance	control pins; V_I = 3 V or 0 V		-	1.7	-	pF
$C_{io(off)}$	off-state input/output capacitance	V_O = 3 V or 0 V; OE = V_{CC}		-	3.4	-	pF
R_{ON}	ON resistance	V_{CC} = 4.0 V	[3]				
		V_I = 2.4 V; I_I = 15 mA		-	16	22	Ω
		V_{CC} = 4.5 V					
		V_I = 0 V; I_I = 64 mA		-	5	7	Ω
		V_I = 0 V; I_I = 30 mA		-	5	7	Ω
		V_I = 2.4 V; I_I = 15 mA		-	10	15	Ω

[1] All typical values are measured at V_{CC} = 5 V; T_{amb} = 25 °C.

[2] This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

[3] Measured by the voltage drop between the A and the B terminals at the indicated current through the switch. ON resistance is determined by the lowest voltage of the two (A or B) terminals.

10. Dynamic characteristics

Table 7. Dynamic characteristics

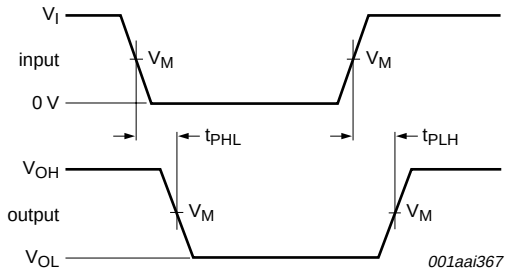
T_{amb} = –40 °C to +85 °C; V_{CC} = 4.5 V to 5.5 V; for test circuit see Figure 8.

Symbol	Parameter	Conditions		Min	Max	Unit
t_{pd}	propagation delay	nA to nB or nB to nA; see Figure 6	[1][2]	-	0.25	ns
t_{en}	enable time	OE to nA or nB; see Figure 7	[2]	1.6	4.5	ns
t_{dis}	disable time	OE to nA or nB; see Figure 7	[2]	1.0	5.4	ns

[1] This parameter is warranted but not production tested. The propagation delay is based on the RC time constant of the typical ON resistance of the switch and a load capacitance, when driven by an ideal voltage source (zero output impedance).

[2] t_{PLH} and t_{PHL} are the same as t_{pd};
t_{PZL} and t_{PZH} are the same as t_{en};
t_{PLZ} and t_{PHZ} are the same as t_{dis}.

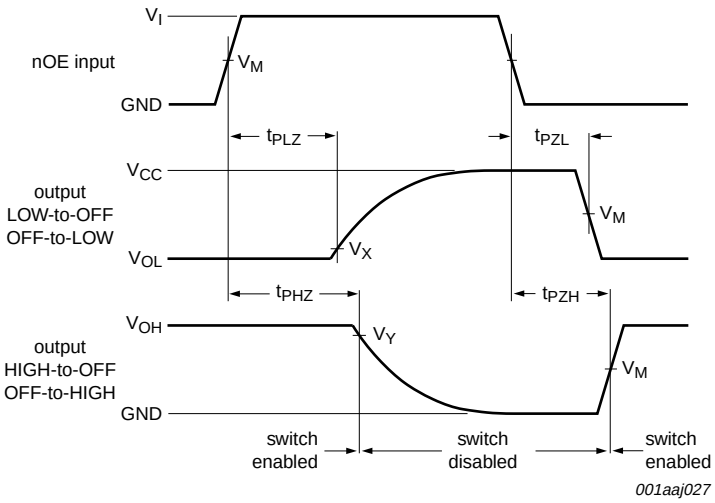
11. AC waveforms



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 6. The input (nA, nB) to output (nB, nA) propagation delay times



Measurement points are given in Table 8.

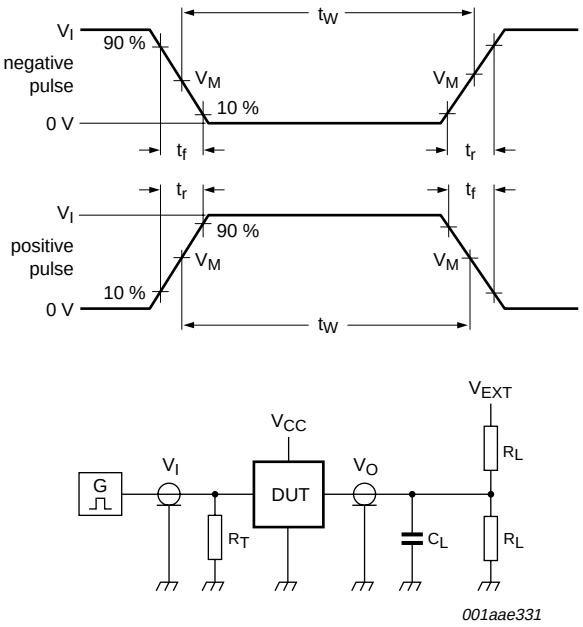
V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 7. Enable and disable times

Table 8. Measurement points

Input	Output		
V_M	V_M	V_X	V_Y
1.5 V	1.5 V	V_{OL} + 0.3 V	V_{OH} – 0.3 V

12. Test information



Test data is given in Table 9.

Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

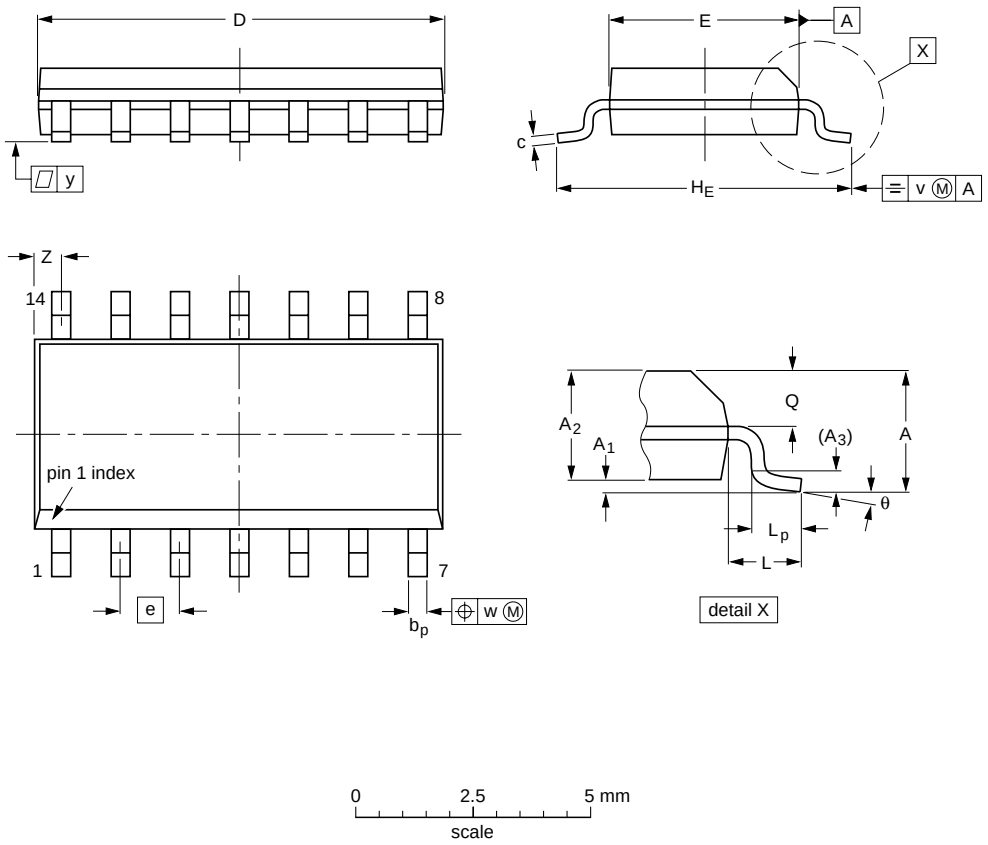
Fig 8. Test circuit for measuring switching times

Table 9. Test data

Supply voltage	Input		Load		V_{EXT}		
V_{CC}	V_I	t_r, t_f	C_L	R_L	t_{PLH}, t_{PHL}	t_{PLZ}, t_{PZL}	t_{PHZ}, t_{PZH}
4.5 V to 5.5 V	GND to 3.0 V	≤ 2.5 ns	50 pF	500 Ω	open	7.0 V	open

13. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm **SOT108-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

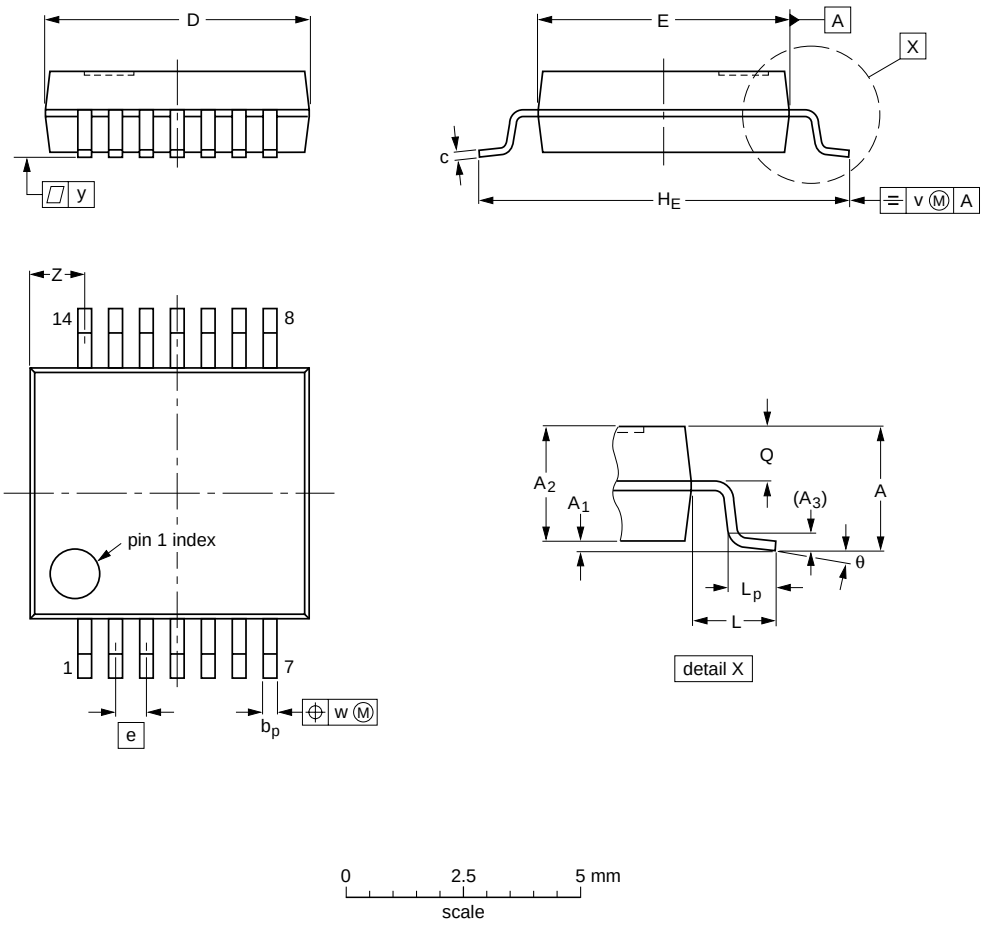
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT108-1	076E06	MS-012				~~99-12-27~~ 03-02-19

Fig 9. Package outline SOT108-1 (SO14)

SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm **SOT337-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.4 0.9	8^o 0^o

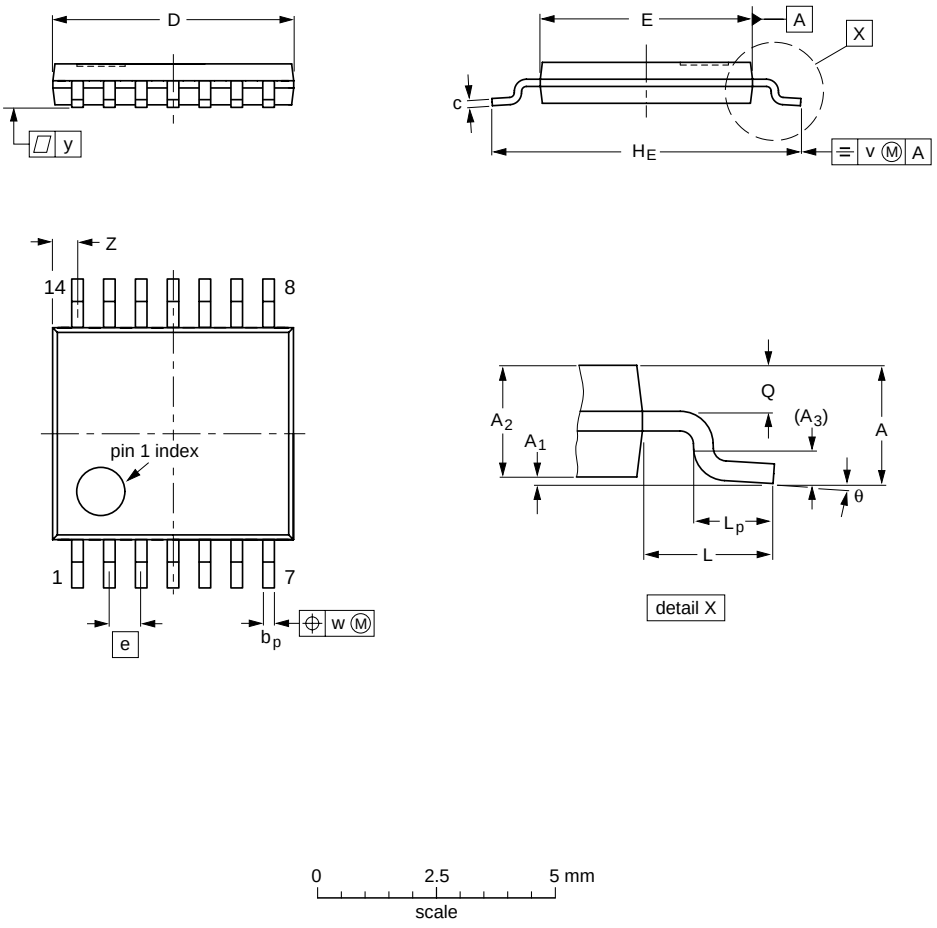
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT337-1		MO-150				~~99-12-27~~ 03-02-19

Fig 10. Package outline SOT337-1 (SSOP14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm **SOT402-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8^o 0^o

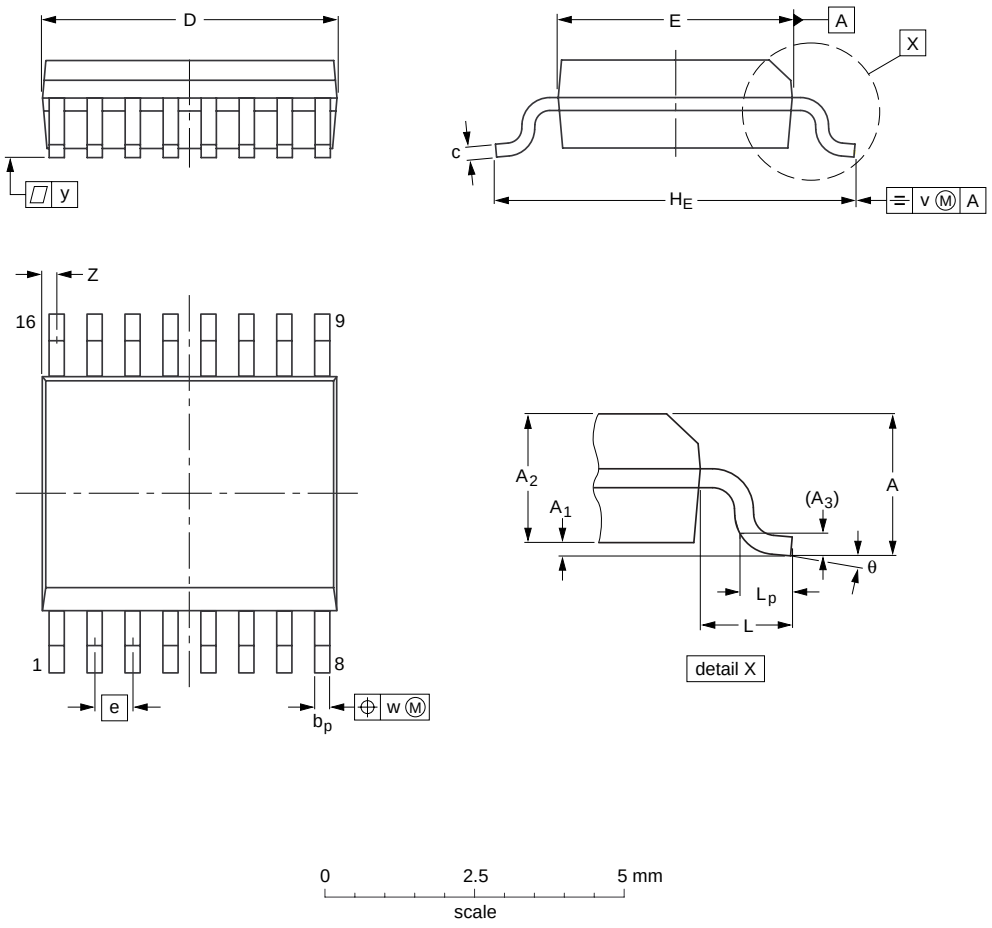
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT402-1		MO-153				~~99-12-27~~ 03-02-18

Fig 11. Package outline SOT402-1 (TSSOP14)

SSOP16: plastic shrink small outline package; 16 leads; body width 3.9 mm; lead pitch 0.635 mm **SOT519-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	v	w	y	Z (1)	θ
mm	1.73	0.25 0.10	1.55 1.40	0.25	0.31 0.20	0.25 0.18	5.0 4.8	4.0 3.8	0.635	6.2 5.8	1	0.89 0.41	0.2	0.18	0.09	0.18 0.05	8^o 0^o

Note

1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT519-1						~~99-05-04~~ 03-02-18

Fig 12. Package outline SOT519-1 (SSOP16)

14. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

15. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
CBT3126_3	20081209	Product data sheet	-	CBT3126_2
Modifications:	• Section 5 “Pinning information” SOT108-1 pin configuration drawing added. • Section 5 “Pinning information” SOT337-4 number changed to SOT337-1 • Section 9 “Static characteristics” in $C_{io(off)}$ conditions $\overline{OE}$ changed to OE • Section 13 “Package outline” SOT109-1, SOT338-1, SOT403-1and SOT763-1 package outline drawings removed. • Section 13 “Package outline” SOT108-1, SOT337-1and SOT402-1 package outline drawings added.			
CBT3126_2	20081023	Product data sheet	-	CBT3126_1
CBT3126_1	20011212	Product data sheet	-	-

16. Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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18. Contents

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