

HD74HC109

Dual J- \bar{K} Flip-Flops (with Preset and Clear)

REJ03D0561-0200
 (Previous ADE-205-434)
 Rev.2.00
 Oct 11, 2005

Description

Each flip-flop has independent J, \bar{K} , preset, clear and clock inputs and Q and \bar{Q} outputs. This device is edge sensitive to the clock input and changes state on the positive going transition of the clock pulse. Clear and preset are independent of the clock and accomplished by a low logic level on the corresponding input.





Features

- High Speed Operation: t_{pd} (Clock to Q) = 15 ns typ ($C_L = 50$ pF)
- High Output Current: Fanout of 10 LSTTL Loads
- Wide Operating Voltage: $V_{CC} = 2$ to 6 V
- Low Input Current: 1 μ A max
- Low Quiescent Supply Current: I_{CC} (static) = 2 μ A max ($T_a = 25^\circ\text{C}$)
- Ordering Information

Part Name	Package Type	Package Code (Previous Code)	Package Abbreviation	Taping Abbreviation (Quantity)
HD74HC109P	DILP-16 pin	PRDP0016AE-B (DP-16FV)	P	—
HD74HC109FPEL	SOP-16 pin (JEITA)	PRSP0016DH-B (FP-16DAV)	FP	EL (2,000 pcs/reel)
HD74HC109RPEL	SOP-16 pin (JEDEC)	PRSP0016DG-A (FP-16DNV)	RP	EL (2,500 pcs/reel)

Note: Please consult the sales office for the above package availability.

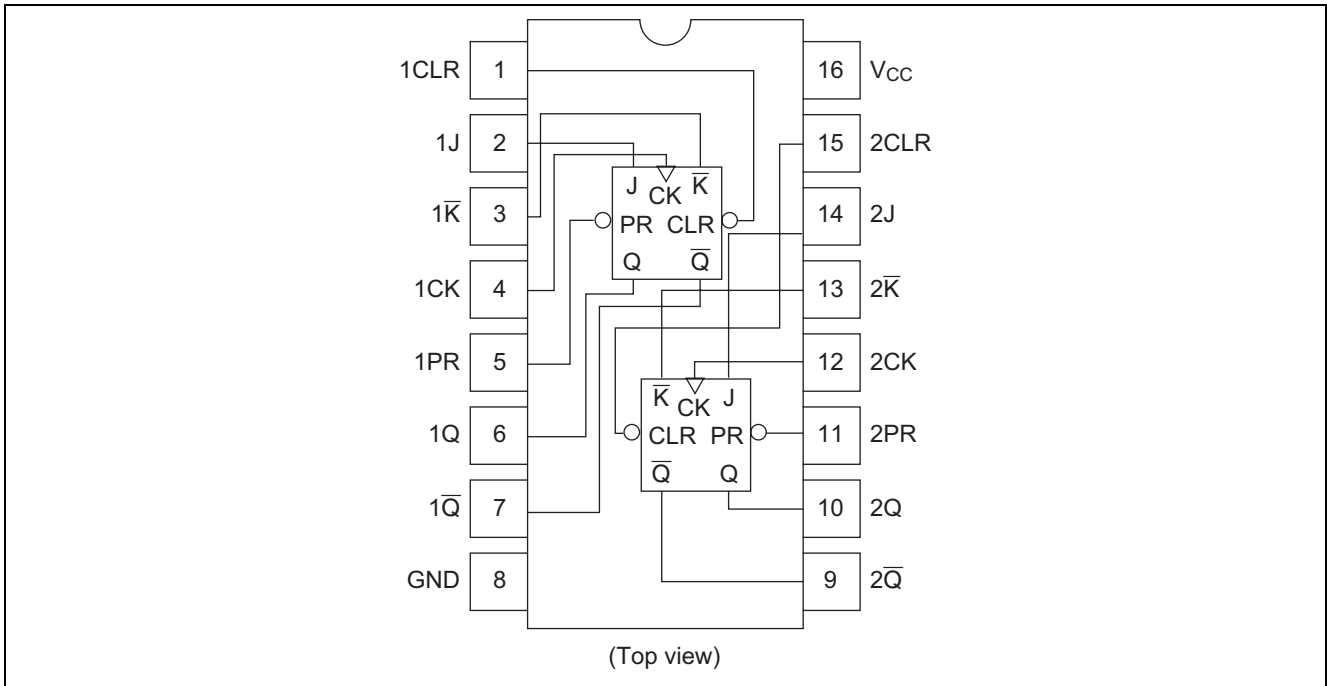
Function Table

Inputs					Outputs	
Preset	Clear	Clock	J	\bar{K}	Q	\bar{Q}
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H^{*1}	H^{*1}
H	H		L	L	L	H
H	H		H	L	Toggle	
H	H		L	H	Q_0	\bar{Q}_0
H	H		H	H	H	L
H	H	L	X	X	Q_0	\bar{Q}_0

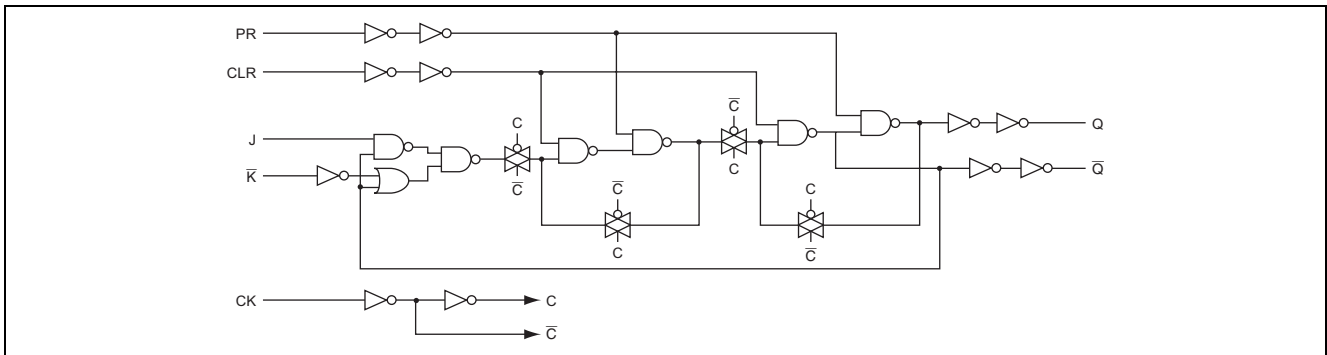
Note: 1. Q and \bar{Q} will remain high as long as preset and clear input are low, but Q and \bar{Q} are unpredictable if preset and clear input go high simultaneously.

H: High level
 L: Low level
 X: Irrelevant

Pin Arrangement



Logic Diagram (1/2)



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage range	V_{CC}	-0.5 to 7.0	V
Input / Output voltage	V_{in}, V_{out}	-0.5 to $V_{CC} + 0.5$	V
Input / Output diode current	I_{IK}, I_{OK}	± 20	mA
Output current	I_O	± 25	mA
V_{CC} , GND current	I_{CC} or I_{GND}	± 50	mA
Power dissipation	P_T	500	mW
Storage temperature	T_{stg}	-65 to +150	$^{\circ}C$

Note: The absolute maximum ratings are values, which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

Recommended Operating Conditions

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	V_{CC}	2 to 6	V	
Input / Output voltage	V_{IN}, V_{OUT}	0 to V_{CC}	V	
Operating temperature	T_a	-40 to 85	°C	
Input rise / fall time ^{*1}	t_r, t_f	0 to 1000	ns	$V_{CC} = 2.0\text{ V}$
		0 to 500		$V_{CC} = 4.5\text{ V}$
		0 to 400		$V_{CC} = 6.0\text{ V}$

Note: 1. This item guarantees maximum limit when one input switches.
 Waveform: Refer to test circuit of switching characteristics.

Electrical Characteristics

Item	Symbol	V_{CC} (V)	$T_a = 25^\circ\text{C}$			$T_a = -40\text{ to }+85^\circ\text{C}$		Unit	Test Conditions	
			Min	Typ	Max	Min	Max			
Input voltage	V_{IH}	2.0	1.5	—	—	1.5	—	V		
		4.5	3.15	—	—	3.15	—			
		6.0	4.2	—	—	4.2	—			
	V_{IL}	2.0	—	—	0.5	—	0.5	V		
		4.5	—	—	1.35	—	1.35			
		6.0	—	—	1.8	—	1.8			
Output voltage	V_{OH}	2.0	1.9	2.0	—	1.9	—	V	$V_{in} = V_{IH}\text{ or }V_{IL}$	$I_{OH} = -20\ \mu\text{A}$
		4.5	4.4	4.5	—	4.4	—			$I_{OH} = -4\ \text{mA}$
		6.0	5.9	6.0	—	5.9	—			$I_{OH} = -5.2\ \text{mA}$
		4.5	4.18	—	—	4.13	—			
		6.0	5.68	—	—	5.63	—			
	V_{OL}	2.0	—	0.0	0.1	—	0.1	V	$V_{in} = V_{IH}\text{ or }V_{IL}$	$I_{OL} = 20\ \mu\text{A}$
		4.5	—	0.0	0.1	—	0.1			
		6.0	—	0.0	0.1	—	0.1			
		4.5	—	—	0.26	—	0.33			$I_{OL} = 4\ \text{mA}$
		6.0	—	—	0.26	—	0.33			$I_{OL} = 5.2\ \text{mA}$
Input current	I_{in}	6.0	—	—	± 0.1	—	± 1.0	μA	$V_{in} = V_{CC}\text{ or GND}$	
Quiescent supply current	I_{CC}	6.0	—	—	2.0	—	20	μA	$V_{in} = V_{CC}\text{ or GND}, I_{out} = 0\ \mu\text{A}$	

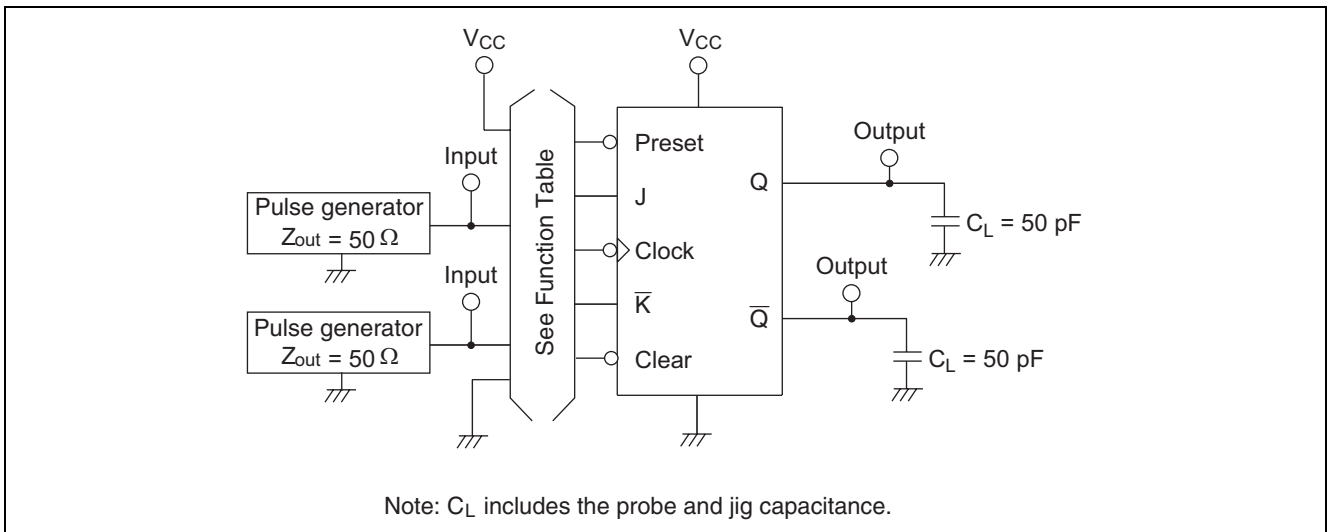
Switching Characteristics ($C_L = 50\ \text{pF}$, Input $t_r = t_f = 6\ \text{ns}$)

Item	Symbol	V_{CC} (V)	$T_a = 25^\circ\text{C}$			$T_a = -40\text{ to }+85^\circ\text{C}$		Unit	Test Conditions	
			Min	Typ	Max	Min	Max			
Maximum clock frequency	f_{max}	2.0	—	—	5	—	4	ns		
		4.5	—	—	27	—	21			
		6.0	—	—	32	—	25			
Propagation delay time	t_{PLH}, t_{PHL}	2.0	—	—	175	—	220	ns	Clock to Q or \bar{Q}	
		4.5	—	15	35	—	44			
		6.0	—	—	30	—	37			
	t_{rem}	2.0	—	—	190	—	240	ns	Preset or Clear to Clock	
		4.5	—	14	38	—	48			
		6.0	—	—	32	—	41			
Removal time	t_{rem}	2.0	25	—	—	32	—	ns		
		4.5	5	1	—	6	—			
		6.0	4	—	—	5	—			

Switching Characteristics ($C_L = 50 \text{ pF}$, Input $t_r = t_f = 6 \text{ ns}$)

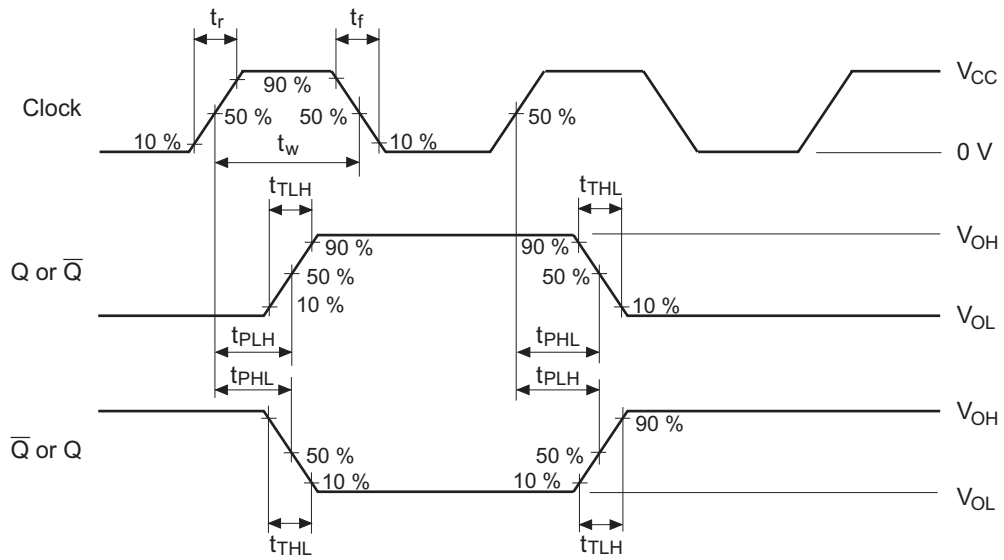
Item	Symbol	V_{CC} (V)	$T_a = 25^\circ\text{C}$			$T_a = -40 \text{ to } +85^\circ\text{C}$		Unit	Test Conditions
			Min	Typ	Max	Min	Max		
Setup time	t_{su}	2.0	100	—	—	125	—	ns	Data to Latch Enable
		4.5	20	4	—	25	—		
		6.0	17	—	—	21	—		
Hold time	t_h	2.0	0	—	—	0	—	ns	Latch Enable to Data
		4.5	0	-4	—	0	—		
		6.0	0	—	—	0	—		
Pulse width	t_w	2.0	80	—	—	100	—	ns	Latch Enable
		4.5	16	5	—	20	—		
		6.0	14	—	—	17	—		
Output rise/fall time	t_{TLH}, t_{THL}	2.0	—	—	75	—	95	ns	
		4.5	—	5	15	—	19		
		6.0	—	—	13	—	16		
Input capacitance	C_{in}	—	—	5	10	—	10	pF	

Test Circuit

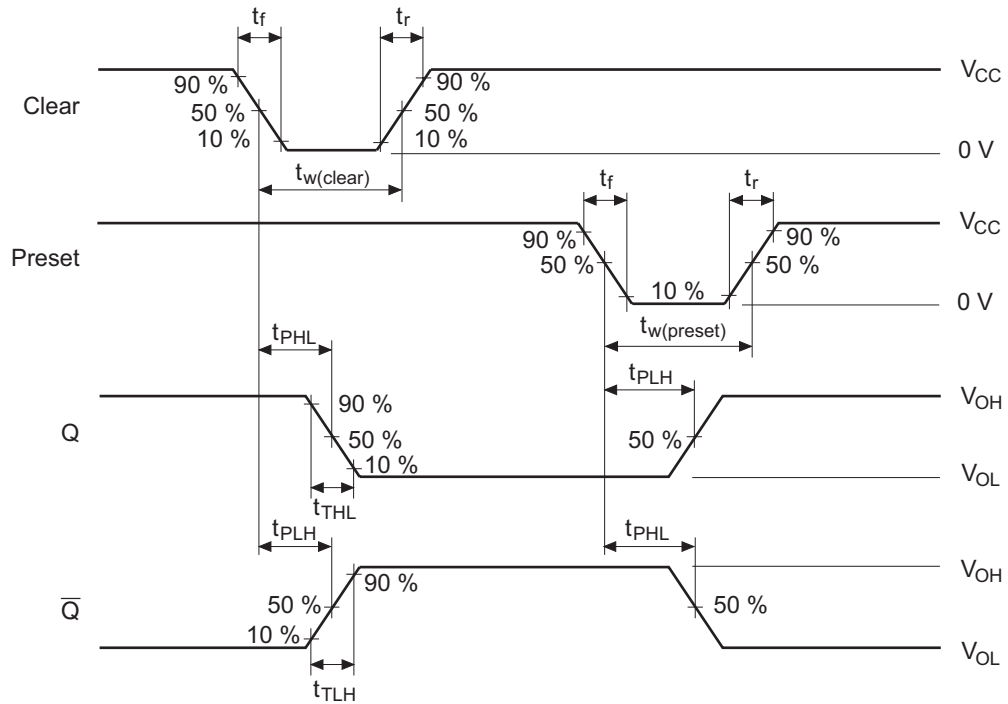


Waveforms

• Waveform – 1

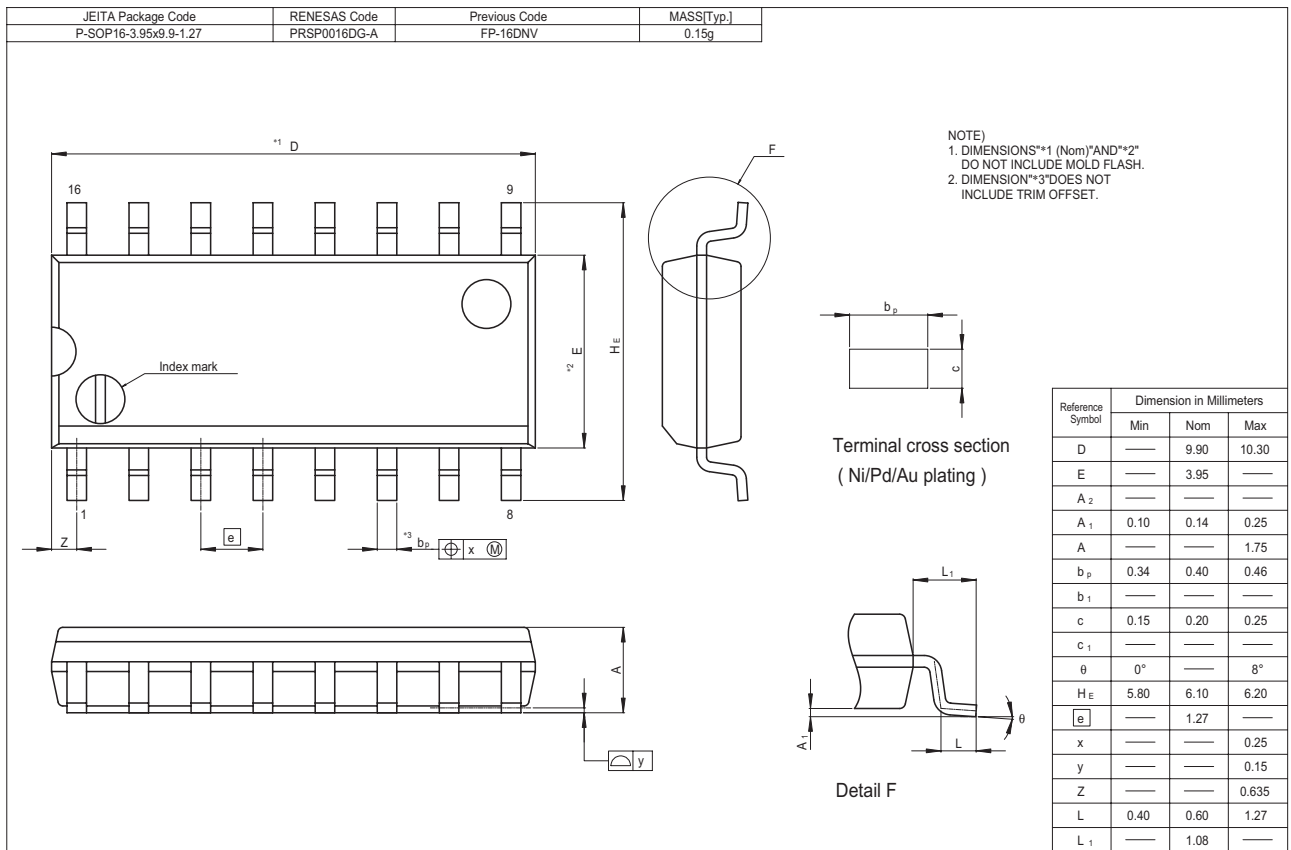
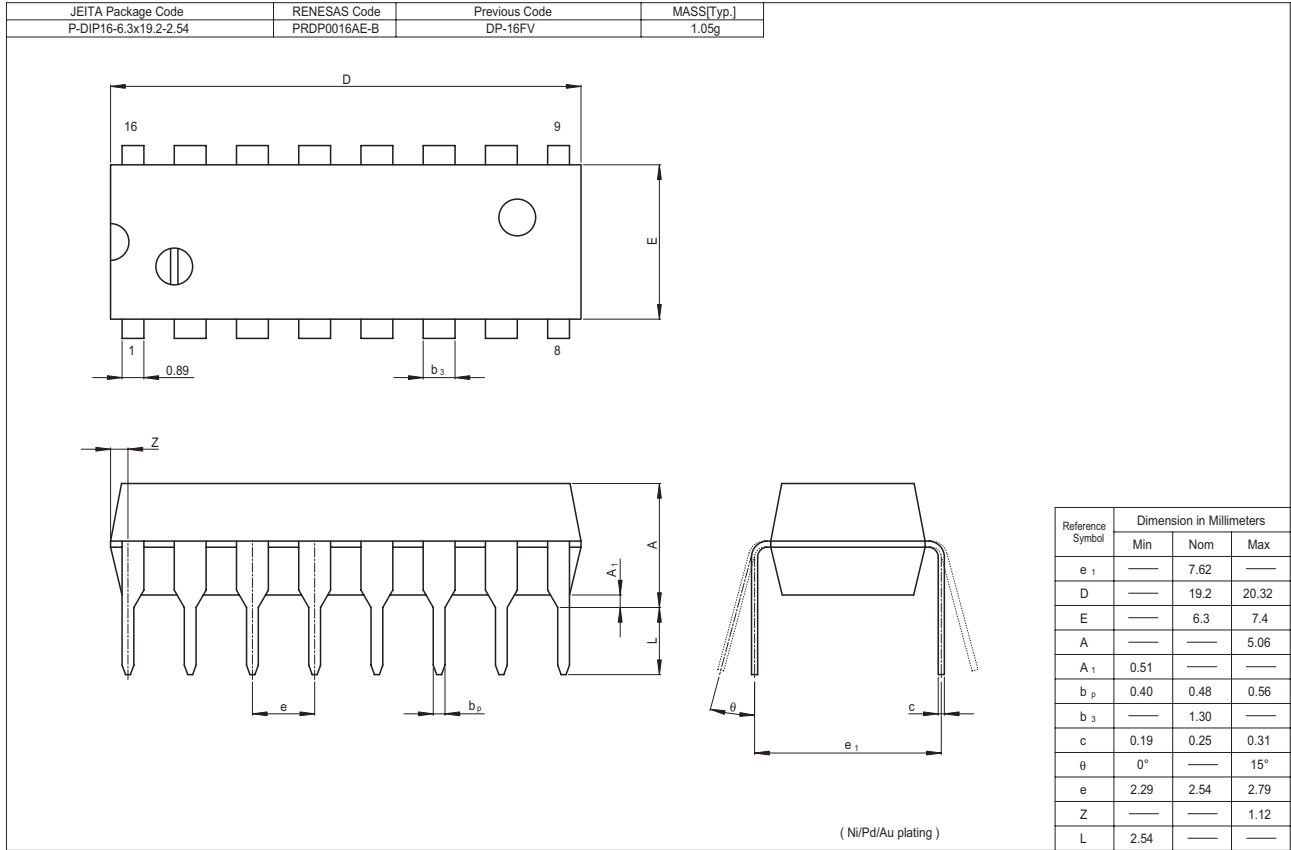


• Waveform – 2

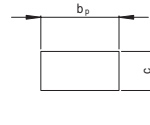
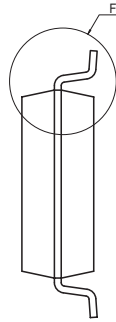
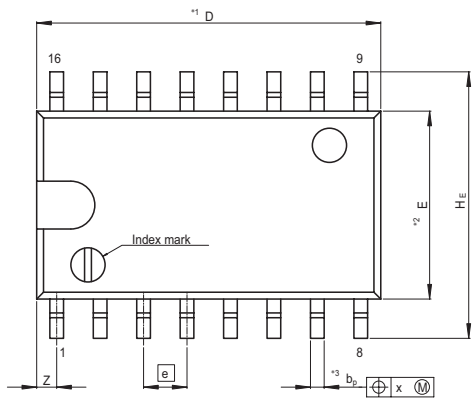


- Notes: 1. Input waveform: $PRR \leq 1 \text{ MHz}$, $Z_o = 50 \Omega$, $t_r \leq 6 \text{ ns}$, $t_f \leq 6 \text{ ns}$
 2. The output are measured one at a time with one transition per measurement.

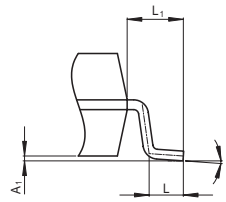
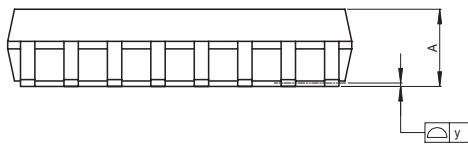
Package Dimensions



JEITA Package Code P-SOP16-5.5x10.06-1.27	RENESAS Code PRSP0016DH-B	Previous Code FP-16DAV	MASS[Typ.] 0.24g
--	------------------------------	---------------------------	---------------------



Terminal cross section
(Ni/Pd/Au plating)



Detail F

NOTE)
1. DIMENSIONS*1 (Nom)*AND*2*
DO NOT INCLUDE MOLD FLASH.
2. DIMENSION*3*DOES NOT
INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	10.06	10.5
E	—	5.50	—
A ₂	—	—	—
A ₁	0.00	0.10	0.20
A	—	—	2.20
b _p	0.34	0.40	0.46
b ₁	—	—	—
c	0.15	0.20	0.25
c ₁	—	—	—
θ	0°	—	8°
H _E	7.50	7.80	8.00
e	—	1.27	—
x	—	—	0.12
y	—	—	0.15
Z	—	—	0.80
L	0.50	0.70	0.90
L ₁	—	1.15	—

Renesas Technology Corp. Sales Strategic Planning Div. Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

Keep safety first in your circuit designs!

1. Renesas Technology Corp. puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage. Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

Notes regarding these materials

1. These materials are intended as a reference to assist our customers in the selection of the Renesas Technology Corp. product best suited to the customer's application; they do not convey any license under any intellectual property rights, or any other rights, belonging to Renesas Technology Corp. or a third party.
 2. Renesas Technology Corp. assumes no responsibility for any damage, or infringement of any third-party's rights, originating in the use of any product data, diagrams, charts, programs, algorithms, or circuit application examples contained in these materials.
 3. All information contained in these materials, including product data, diagrams, charts, programs and algorithms represents information on products at the time of publication of these materials, and are subject to change by Renesas Technology Corp. without notice due to product improvements or other reasons. It is therefore recommended that customers contact Renesas Technology Corp. or an authorized Renesas Technology Corp. product distributor for the latest product information before purchasing a product listed herein.
The information described here may contain technical inaccuracies or typographical errors.
Renesas Technology Corp. assumes no responsibility for any damage, liability, or other loss rising from these inaccuracies or errors.
Please also pay attention to information published by Renesas Technology Corp. by various means, including the Renesas Technology Corp. Semiconductor home page (<http://www.renesas.com>).
 4. When using any or all of the information contained in these materials, including product data, diagrams, charts, programs, and algorithms, please be sure to evaluate all information as a total system before making a final decision on the applicability of the information and products. Renesas Technology Corp. assumes no responsibility for any damage, liability or other loss resulting from the information contained herein.
 5. Renesas Technology Corp. semiconductors are not designed or manufactured for use in a device or system that is used under circumstances in which human life is potentially at stake. Please contact Renesas Technology Corp. or an authorized Renesas Technology Corp. product distributor when considering the use of a product contained herein for any specific purposes, such as apparatus or systems for transportation, vehicular, medical, aerospace, nuclear, or undersea repeater use.
 6. The prior written approval of Renesas Technology Corp. is necessary to reprint or reproduce in whole or in part these materials.
 7. If these products or technologies are subject to the Japanese export control restrictions, they must be exported under a license from the Japanese government and cannot be imported into a country other than the approved destination.
Any diversion or reexport contrary to the export control laws and regulations of Japan and/or the country of destination is prohibited.
 8. Please contact Renesas Technology Corp. for further details on these materials or the products contained therein.
-



RENESAS SALES OFFICES

<http://www.renesas.com>

Refer to "<http://www.renesas.com/en/network>" for the latest and detailed information.

Renesas Technology America, Inc.

450 Holger Way, San Jose, CA 95134-1368, U.S.A
Tel: <1> (408) 382-7500, Fax: <1> (408) 382-7501

Renesas Technology Europe Limited

Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K.
Tel: <44> (1628) 585-100, Fax: <44> (1628) 585-900

Renesas Technology Hong Kong Ltd.

7th Floor, North Tower, World Finance Centre, Harbour City, 1 Canton Road, Tsimshatsui, Kowloon, Hong Kong
Tel: <852> 2265-6688, Fax: <852> 2730-6071

Renesas Technology Taiwan Co., Ltd.

10th Floor, No.99, Fushing North Road, Taipei, Taiwan
Tel: <886> (2) 2715-2888, Fax: <886> (2) 2713-2999

Renesas Technology (Shanghai) Co., Ltd.

Unit2607 Ruijing Building, No.205 Maoming Road (S), Shanghai 200020, China
Tel: <86> (21) 6472-1001, Fax: <86> (21) 6415-2952

Renesas Technology Singapore Pte. Ltd.

1 Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632
Tel: <65> 6213-0200, Fax: <65> 6278-8001

Renesas Technology Korea Co., Ltd.

Kukje Center Bldg. 18th Fl., 191, 2-ka, Hangang-ro, Yongsan-ku, Seoul 140-702, Korea
Tel: <82> 2-796-3115, Fax: <82> 2-796-2145

Renesas Technology Malaysia Sdn. Bhd.

Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No.18, Jalan Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: <603> 7955-9390, Fax: <603> 7955-9510