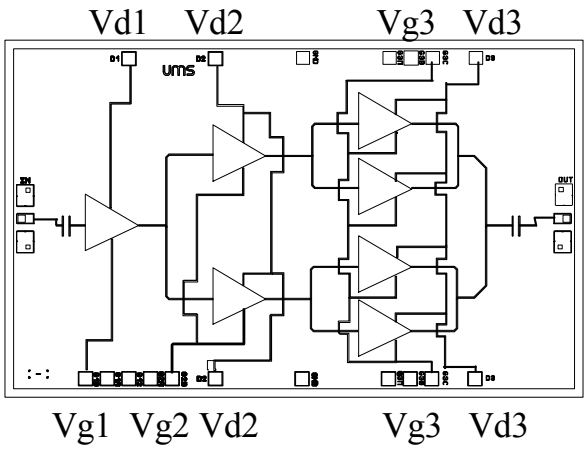
24.5-26.5GHz High Power Amplifier

GaAs Monolithic Microwave IC

Description

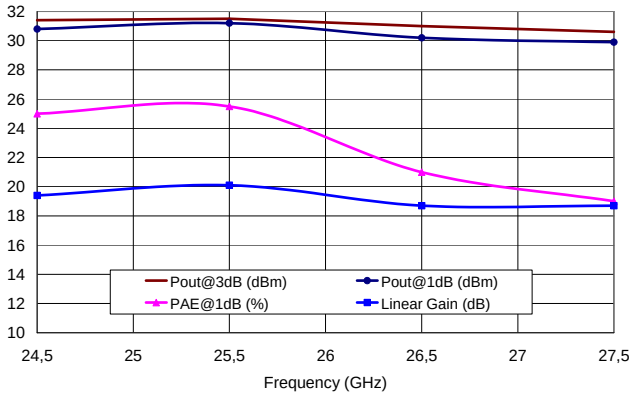
The CHA5295 is a high gain three-stage monolithic high power amplifier. It is designed for a wide range of applications, from military to commercial communication systems. The backside of the chip is both RF and DC grounds. This help simplifies the assembly process.

The circuit is manufactured with a PM-HEMT process, 0.25µm gate length, via holes through the substrate, air bridges and electron beam gate lithography.
It is available in chip form.



Main Features

- Performances : 24.5-26.5GHz
- 31dBm output power @ 1dB comp.
- 18 dB ± 1dB gain
- DC power consumption, 800mA @ 6V
- Chip size : 4.01 x 2.52 x 0.05 mm



Typical on jig Measurements

Main Characteristics

Tamb. = 25°C

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency range	24.5		26.5	GHz
G	Small signal gain	17	18		dB
P1dB	Output power at 1dB gain compression	30	31		dBm
Id	Bias current		800		mA

ESD Protection : Electrostatic discharge sensitive device. Observe handling precautions !

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Electrical Characteristics

Tamb = +25℃, Vd = 6V Id #800mA

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency range (1)	24.5		26.5	GHz
G	Small signal gain (1)	17	18		dB
ΔG	Small signal gain flatness (1)		±1		dB
Is	Reverse isolation		50		dB
P1dB	Pulsed output power at 1dB compression (1)	30	31		dBm
P03	Output power at 3dB gain compression (1)		31.5		dBm
IP3	3rd order intercept point (2) (3)		41		dBm
PAE	Power added efficiency at 1dB comp.		20		%
VSWRin	Input VSWR			3.5:1	
VSWRout	Output VSWR			2:1	
Tj	Junction temperature for 80℃ backside		+155		℃
Id	Bias current @ small signal		800	1000	mA

(1) These values are representative for pulsed on-wafer measurements that are made without bonding wires at the RF ports.
(2) Value representative for CW on jig measurement.
(3) Linearity could be improved with a biasing point around 600mA (see curves on next pages)

Absolute Maximum Ratings

Tamb. = 25℃ (1)

Symbol	Parameter	Values	Unit
Vd	Maximum drain bias voltage with Pin max=12dBm	+6.25	V
Id	Maximum drain bias current	1400	mA
Vg	Gate bias voltage	-2.5 to +0.4	V
Ig	Gate bias current	-5 to +5	mA
Vdg	Maximum drain to gate voltage (Vd - Vg)	+8.0	V
Pin	Maximum input power overdrive (2)	+15	dBm
Tch	Maximum channel temperature	+175	℃
Ta	Operating temperature range	-40 to +80	℃
Tstg	Storage temperature range	-55 to +125	℃

(1) Operation of this device above anyone of these parameters may cause permanent damage.

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(2) Duration < 1s.

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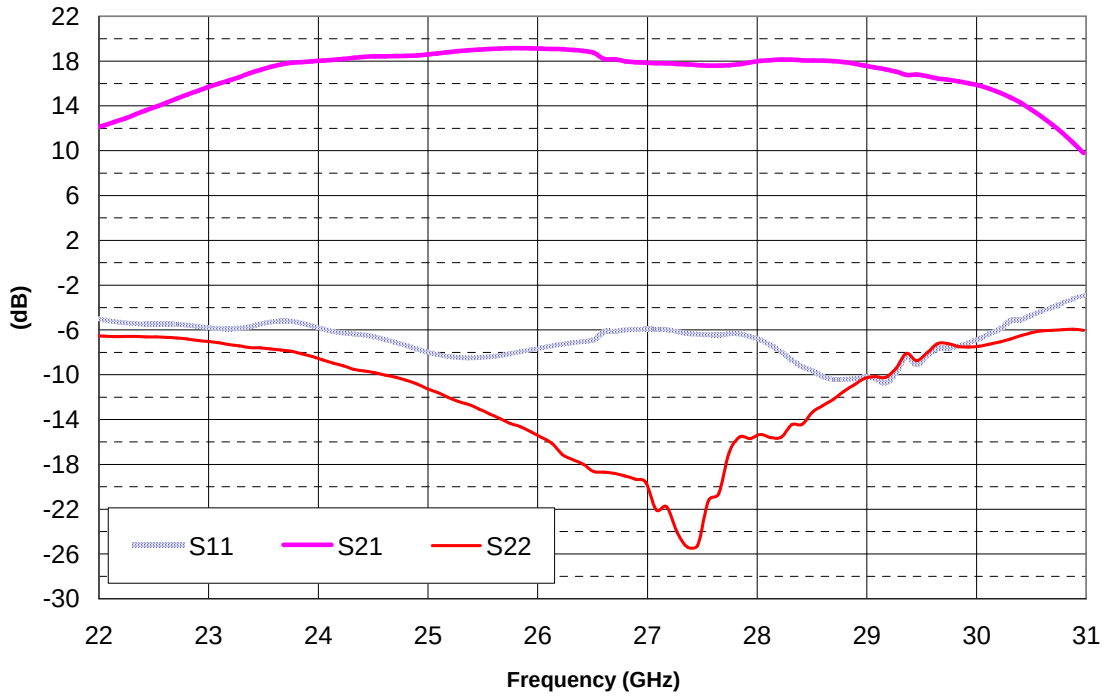
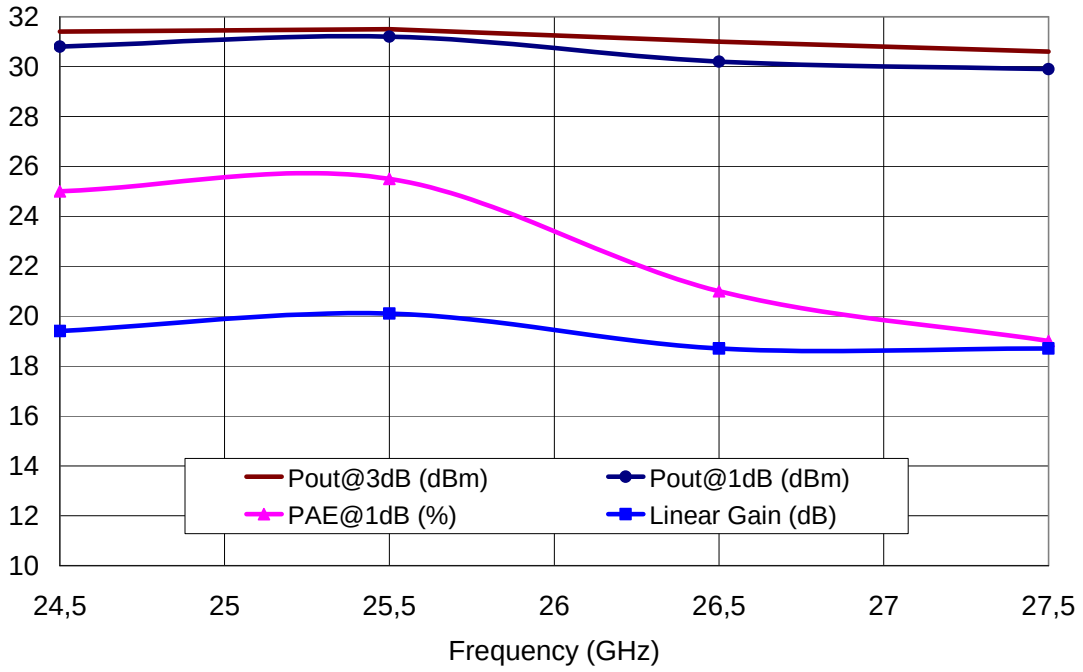
Typical on Jig Measurements

Bias conditions: Vd=6V, Vg tuned for Id #800mA



Linear Gain & Return Losses versus frequency



Linear Gain, Output power @ 1dB & 3dB compression,
PAE @ 1dB compression

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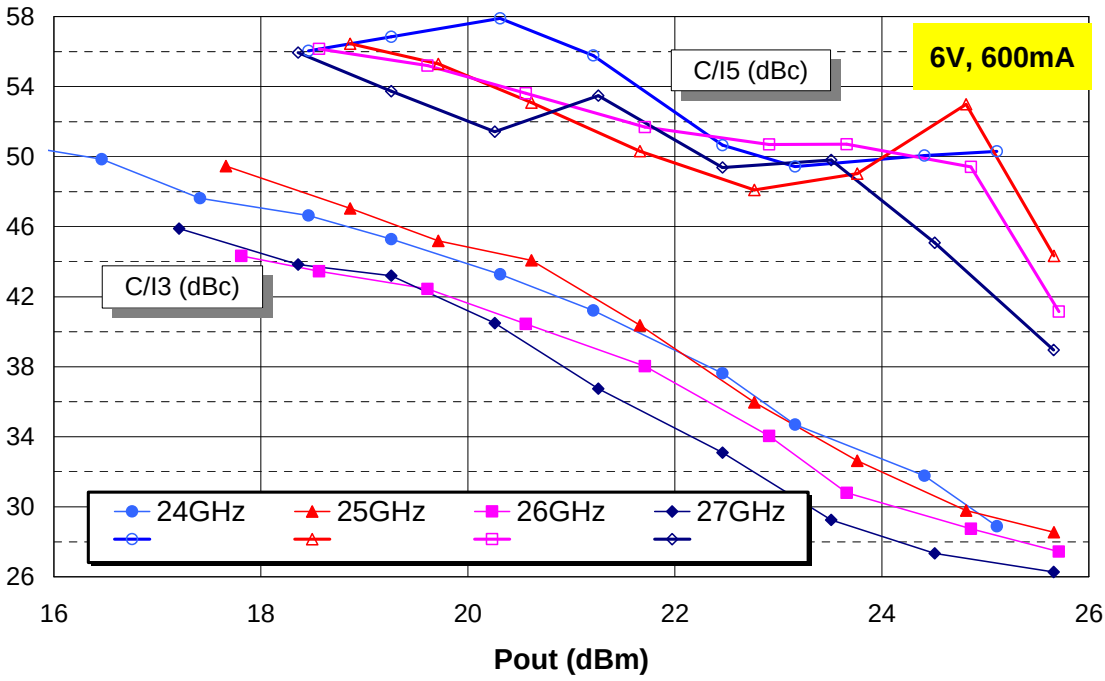
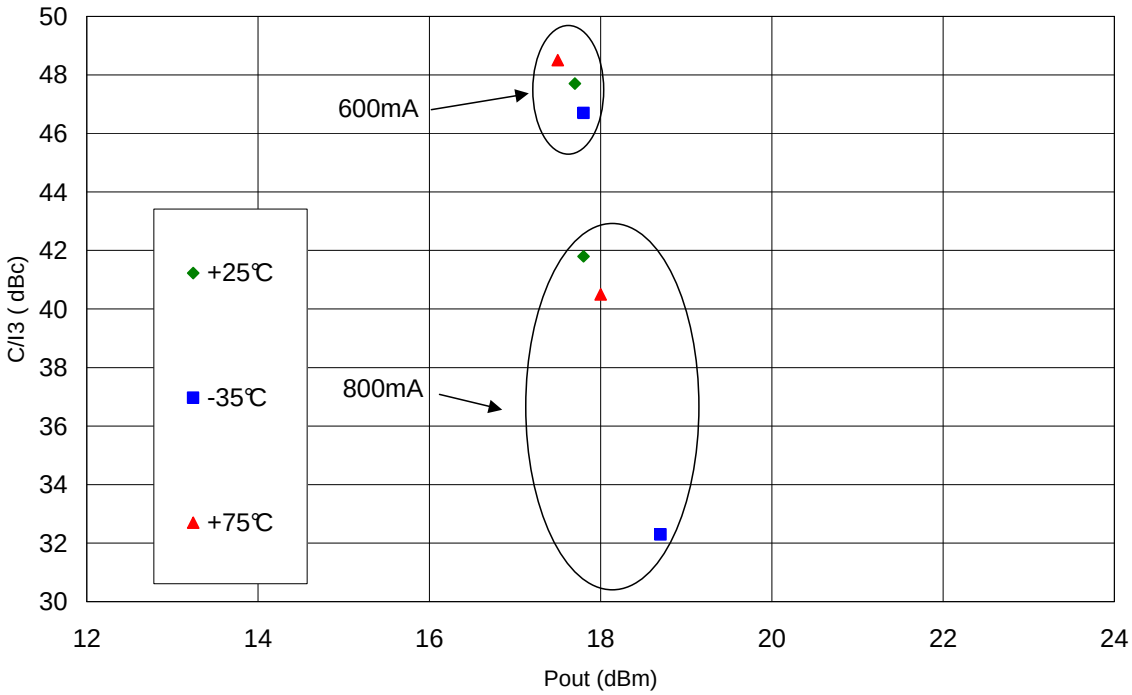


C/I3 & C/I5 versus DCL* Output Power



C/I3 versus drain current & temperature @ 25.5GHz

DCL: Double Carrier Level

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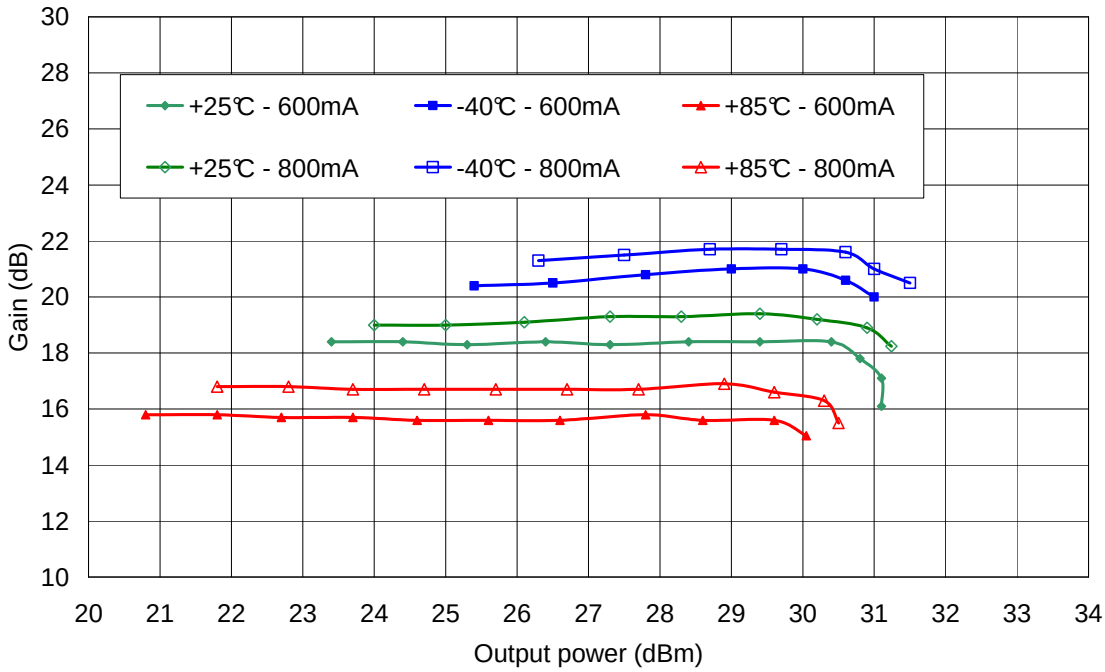

Output power versus temperature & Drain current @ 25.5GHz

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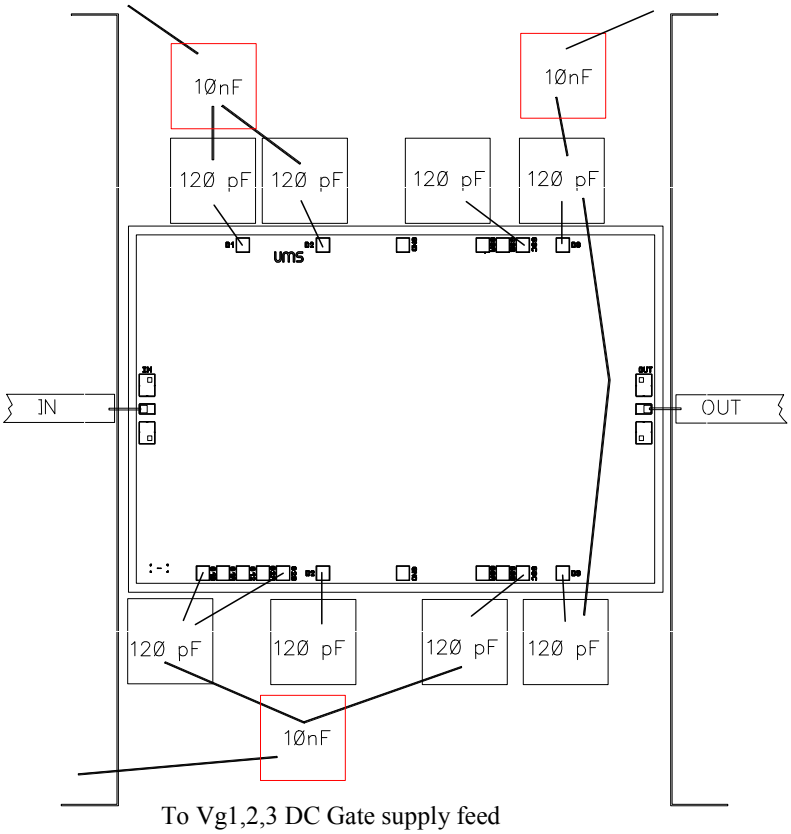
Chip Assembly and Mechanical Data

To Vd1,Vd2 DC Drain supply feed To Vd3 DC Drain supply feed



To Vg1,2,3 DC Gate supply feed

Note : Supply feed should be capacitively by-passed. 25µm diameter gold wire is to be prefered.

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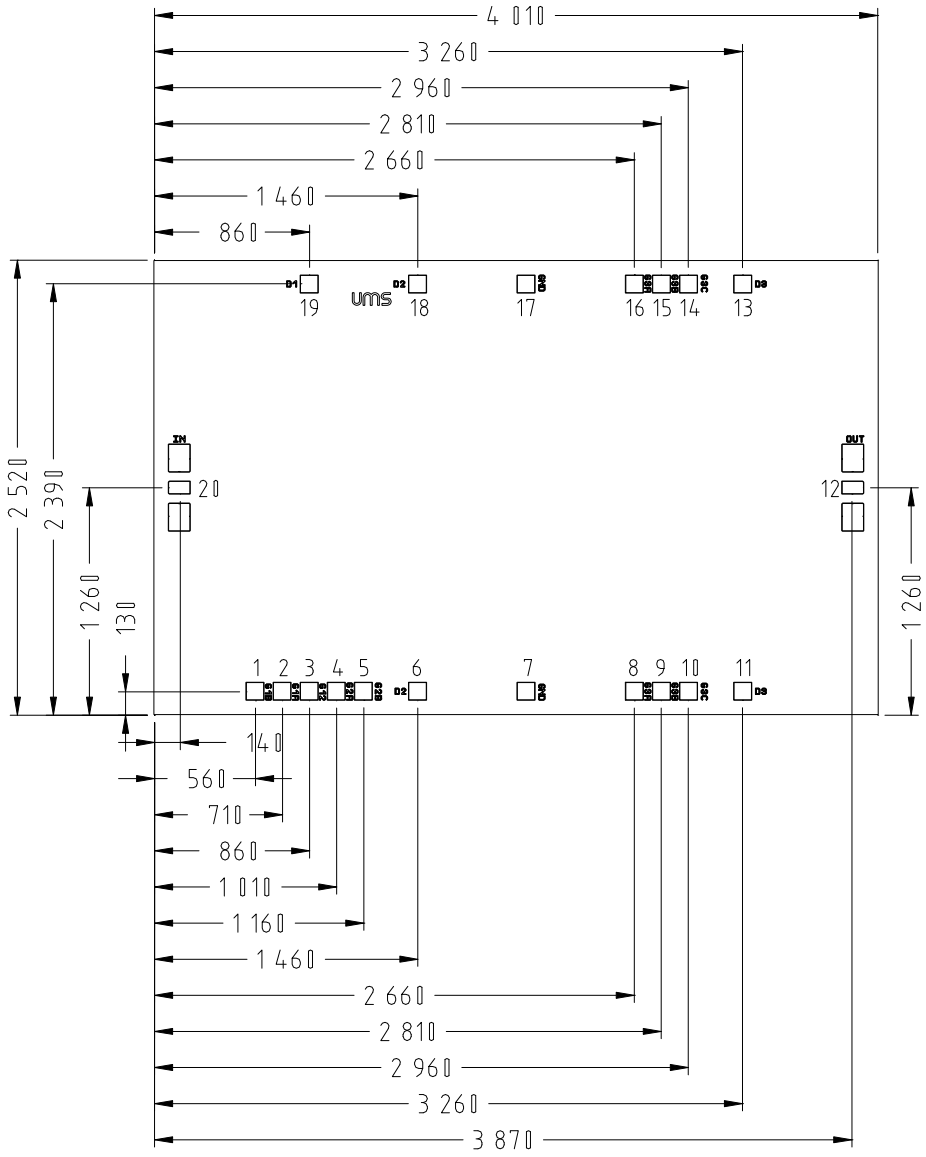

Bonding pad positions.
(Chip thickness : 50µm)

Application note

Due to 50µm thickness, specific care is requested for the handling and assembly.

Bias operation sequence:

ON: Supply Gate voltage
Supply Drain voltage
OFF: Cut off Drain voltage
Cut off Gate voltage

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Ordering Information

Chip form : CHA5295-99F/00

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