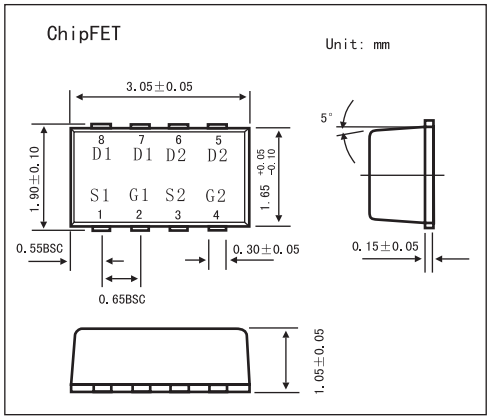
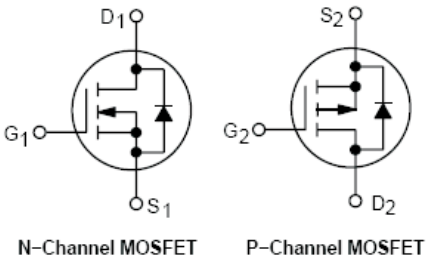
Power MOSFET

KTHC5513



■ Features

- Complementary N-Channel and P-Channel MOSFET
  Leadless SMD Package Featuring Complementary Pair
- Low $R_{DS(on)}$ in a ChipFET Package for High Efficiency Performance
- Low Profile (< 1.10 mm) Allows Placement in Extremely Thin Environments Such as Portable Electronics



N-Channel MOSFET P-Channel MOSFET

■ Absolute Maximum Ratings Ta = 25℃

Parameter	Symbol	N-Channel	P-Channel	Unit
Drain-source voltage	V_{DSS}	20		V
Gate-source voltage	V_{GSS}	±12		V
Drain current Continuous *1 T_A = 25℃	I_D	2.9	-2.2	A
T_A = 85℃		2.1	-1.6	
t≤5		3.9	-3	
Drain current Pulsed t = 10μs *1	I_{DM}	12	-9	A
Total power dissipation	P_D	1.1		W
t≤5		2.1		W
Operating and Storage Temperature Range	T_J, T_{stg}	-55 to 150		℃
Lead Temperature for Soldering Purposes	T_L	260		℃
Junction-to-Ambient *1 Steady State	$R_{\theta JA}$	110		℃/W
t≤5		60		

*1 Surface Mounted on FR4 board using 1 in sq pad size

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■ Electrical Characteristics Ta = 25℃

Parameter	Symbol	Testconditons		Min	Typ	Max	Unit
Drain-source breakdown voltage	$V_{(BR)\ DSS}$	I_D=250μA,V_{GS}=0V	N-Ch	20			V
		I_D=-250μA,V_{GS}=0V	P-Ch	-20			
Zero gate voltage drain current	I_{DSS}	V_{DS}=16V,V_{GS}=0V	N-Ch			1	μA
		V_{DS}=16V,V_{GS}=0V,T_J = 85℃				5	
		V_{DS}=-16V,V_{GS}=0V	P-Ch			-1	
		V_{DS}=-16V,V_{GS}=0V,T_J = 85℃				-5	
Gate?to?Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±12 V	N-Ch			±100	nA
			P-Ch			±100	
Gate threshold voltage *1	$V_{GS\ (th)}$	V_{DS} = V_{GS}, I_D = 250μA	N-Ch	0.6		1.2	V
		V_{DS} = V_{GS}, I_D = -250μA	P-Ch	-0.6		-1.2	
Static drain-source on-state resistance *1	$R_{DS\ (on)}$	I_D=2.9A,V_{GS}=4.5A	N-Ch		0.058	0.08	Ω
		I_D=2.3A,V_{GS}=2.5V			0.077	0.115	
Static drain-source on-state resistance *1	$R_{DS\ (on)}$	I_D=-2.2A,V_{GS}=-4.5V	P-Ch		0.13	0.155	Ω
		I_D=-1.7A,V_{GS}=-2.5V			0.200	0.240	
Forward Transconductance	g_{FS}	I_D=2.9A,V_{DS}=10V	N-Ch		6.0		S
		I_D=-2.2A,V_{DS}=-10V	P-Ch		6.0		
Input capacitance	C_{iss}	N-Channel	N-Ch		180		pF
		V_{DS}=10V,V_{GS}=0V,f=1MHz	P-Ch		185		
Output capacitance	C_{oss}		N-Ch		80		pF
		P-Channel	P-Ch		95		
Reverse transfer capacitance	C_{rss}	V_{DS}=-10V,V_{GS}=0V,f=1MHz	N-Ch		25		pF
			P-Ch		30		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 4.5 V, V_{DS} = 10 V, I_D = 2.9 A	N-Ch		2.6	4.0	nC
		V_{GS} =-4.5 V, V_{DS} = -10 V, I_D =-2.2 A	P-Ch		3.0	6.0	
Gate?to?Source Gate Charge	Q_{GS}	V_{GS} = 4.5 V, V_{DS} = 10 V, I_D = 2.9 A	N-Ch		0.6		
		V_{GS} =-4.5 V, V_{DS} =-10 V, I_D =-2.2 A	P-Ch		0.5		
Gate?to?Drain "Miller" Charge	Q_{GD}	V_{GS} = 4.5 V, V_{DS} = 10 V, I_D = 2.9 A	N-Ch		0.7		
		V_{GS} =-4.5 V, V_{DS} =-10 V, I_D =-2.2 A	P-Ch		0.9		
Turn-on delay time	$t_{d\ (on)}$	I_D=2.9A,V_{DD}=16V	N-Ch		5.0	10	ns
		I_D=-2.2A,V_{DD}=-16V	P-Ch		7.0	12	
Rise time	tr	N-Channel	N-Ch		9	18	ns
		V_{GS}=4.5V,R_G=2.5Ω*2	P-Ch		13	25	
Turn-off delay time *1	$t_{d\ (off)}$		N-Ch		10	20	ns
		P-Channel	P-Ch		33	50	
Fall time *1	tf	V_{GS}=-4.5V,,R_G=2.5Ω *2	N-Ch		3.0	6.0	ns
			P-Ch		27	40	
Forward Voltage *1	V_{SD}	I_S=2.6 A,V_{GS}=0V	N-Ch		0.8	1.15	V
		I_S=-2.1 A,V_{GS}=0 V	P-Ch		-0.8	-1.15	

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Parameter	Symbol	Testconditons		Min	Typ	Max	Unit
Reverse Recovery Time	t_{rr}	N-Channel V_{GS} = 0 V,dI_S/dt = 100 A/μs,Is=1.5 A	N-Ch		12.5		ns
			P-Ch		32		
	t_a		N-Ch		9		
			P-Ch		10		
	t_b	P-Channel V_{GS} = 0 V,dI_S/dt = 100 A/μs,Is=?1.5A	N-Ch		3.5		
			P-Ch		22		
Reverse Recovery Storage Charge	Q_{RR}		N-Ch		6		μC
			P-Ch		15		

*1 Pulse Test: Pulse Width ≤250 μs, Duty Cycle ≤2%.

*2 Switching characteristics are independent of operating junction temperature.