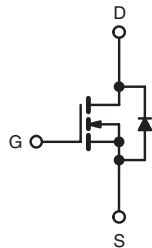
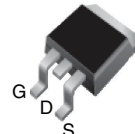
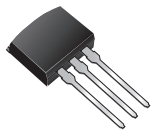




Power MOSFET

PRODUCT SUMMARY	
V_{DS} (V)	600
$R_{DS(on)}$ (Ω)	$V_{GS} = 10\text{ V}$ 2.2
Q_g (Max.) (nC)	23
Q_{gs} (nC)	5.4
Q_{gd} (nC)	11
Configuration	Single

I²PAK (TO-262) D²PAK (TO-263)



N-Channel MOSFET

FEATURES

- Low Gate Charge Q_g Results in Simple Drive Requirement
- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche Voltage and Current
- Effective C_{OSS} Specified
- Lead (Pb)-free Available



RoHS* COMPLIANT

APPLICATIONS

- Switch Mode Power Supply (SMPS)
- Uninterruptible Power Supply
- High Speed Power Switching

TYPICAL SMPS TOPOLOGIES

- Single Transistor Flyback

ORDERING INFORMATION				
Package	D ² PAK (TO-263)	D ² PAK (TO-263)	D ² PAK (TO-263)	I ² PAK (TO-262)
Lead (Pb)-free	IRFBC30ASPbF	IRFBC30ASTRLPbF ^a	IRFBC30ASTRRPbF ^a	IRFBC30ALPbF
	SiHFBC30AS-E3	SiHFBC30ASTL-E3 ^a	SiHFBC30ASTR-E3 ^a	SiHFBC30AL-E3
SnPb	IRFBC30AS	IRFBC30ASTRL ^a	IRFBC30ASTRR ^a	IRFBC30AL
	SiHFBC30AS	SiHFBC30ASTL ^a	SiHFBC30ASTR ^a	SiHFBC30AL

Note

a. See device orientation.

ABSOLUTE MAXIMUM RATINGS $T_C = 25\text{ }^\circ\text{C}$, unless otherwise noted				
PARAMETER	SYMBOL	LIMIT	UNIT	
Drain-Source Voltage	V_{DS}	600	V	
Gate-Source Voltage	V_{GS}	± 30		
Continuous Drain Current	V_{GS} at 10 V	$T_C = 25\text{ }^\circ\text{C}$	A	
		$T_C = 100\text{ }^\circ\text{C}$		
Pulsed Drain Current ^{a, e}	I_{DM}	14		
Linear Derating Factor		0.69	W/ $^\circ\text{C}$	
Single Pulse Avalanche Energy ^b	E_{AS}	290	mJ	
Avalanche Current ^a	I_{AR}	3.6	A	
Repetitive Avalanche Energy ^a	E_{AR}	7.4	mJ	
Maximum Power Dissipation	$T_C = 25\text{ }^\circ\text{C}$	P_D	74	W
Peak Diode Recovery dV/dt ^{c, e}		dV/dt	7.0	V/ns
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to + 150	$^\circ\text{C}$	
Soldering Recommendations (Peak Temperature)	for 10 s	300 ^d		

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).

b. Starting $T_J = 25\text{ }^\circ\text{C}$, $L = 46\text{ mH}$, $R_G = 25\text{ }\Omega$, $I_{AS} = 3.6\text{ A}$ (see fig. 12).

c. $I_{SD} \leq 3.6\text{ A}$, $dI/dt \leq 170\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{DS}$, $T_J \leq 150\text{ }^\circ\text{C}$.

d. 1.6 mm from case.


e. Uses IRFBC30A/SiHFBC30A data and test conditions.

* Pb containing terminations are not RoHS compliant, exemptions may apply

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient (PCB Mounted, steady-state) ^a	R_{thJA}	-	40	°C/W
Maximum Junction-to-Case (Drain)	R_{thJC}	-	1.7	

Note

a. When mounted on 1" square PCB (FR-4 or G-10 material).

SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted							
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Static							
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}$, $I_D = 250\text{ }\mu\text{A}$	600	-	-	V	
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$, $I_D = 1\text{ mA}^d$	-	0.67	-	V/ $^\circ\text{C}$	
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	2.0	-	4.5	V	
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 30\text{ V}$	-	-	± 100	nA	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 600\text{ V}$, $V_{GS} = 0\text{ V}$	-	-	25	μA	
		$V_{DS} = 480\text{ V}$, $V_{GS} = 0\text{ V}$, $T_J = 125\text{ }^\circ\text{C}$	-	-	250		
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$, $I_D = 2.2\text{ A}^b$	-	-	2.2	Ω	
Forward Transconductance	g_{fs}	$V_{DS} = 50\text{ V}$, $I_D = 2.2\text{ A}$	2.1	-	-	S	
Dynamic							
Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}$, $V_{DS} = 25\text{ V}$, $f = 1.0\text{ MHz}$, see fig. 5	-	510	-	pF	
Output Capacitance	C_{oss}		-	70	-		
Reverse Transfer Capacitance	C_{rss}		-	3.5	-		
Output Capacitance	C_{oss}	$V_{GS} = 0\text{ V}$	$V_{DS} = 1.0\text{ V}$, $f = 1.0\text{ MHz}$	-	730	-	
Effective Output Capacitance	$C_{oss\text{ eff.}}$		$V_{DS} = 480\text{ V}$, $f = 1.0\text{ MHz}$	-	19	-	
			$V_{DS} = 0\text{ V to }480\text{ V}^c$	-	31	-	
Total Gate Charge	Q_g	$V_{GS} = 10\text{ V}$	$I_D = 3.6\text{ A}$, $V_{DS} = 480\text{ V}$, see fig. 6 and 13 ^b	-	-	23	nC
Gate-Source Charge	Q_{gs}			-	-	5.4	
Gate-Drain Charge	Q_{gd}			-	-	11	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 300\text{ V}$, $I_D = 3.6\text{ A}$, $R_G = 12\text{ }\Omega$, $R_D = 82\text{ }\Omega$, see fig. 10 ^{b, d}	-	9.8	-	ns	
Rise Time	t_r		-	13	-		
Turn-Off Delay Time	$t_{d(off)}$		-	19	-		
Fall Time	t_f		-	12	-		
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	3.6	A	
Pulsed Diode Forward Current ^a	I_{SM}		-	-	14		
Body Diode Voltage	V_{SD}	$T_J = 25\text{ }^\circ\text{C}$, $I_S = 3.6\text{ A}$, $V_{GS} = 0\text{ V}^b$	-	-	1.6	V	
Body Diode Reverse Recovery Time	t_{rr}	$T_J = 25\text{ }^\circ\text{C}$, $I_F = 3.6\text{ A}$, $dI/dt = 100\text{ A}/\mu\text{s}^b$	-	400	600	ns	
Body Diode Reverse Recovery Charge	Q_{rr}		-	1.1	1.7	μC	
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)					

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$.
- $C_{oss\text{ eff.}}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DS} .
- Uses IRFBC30A/SiHFBC30A data and test conditions.



TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

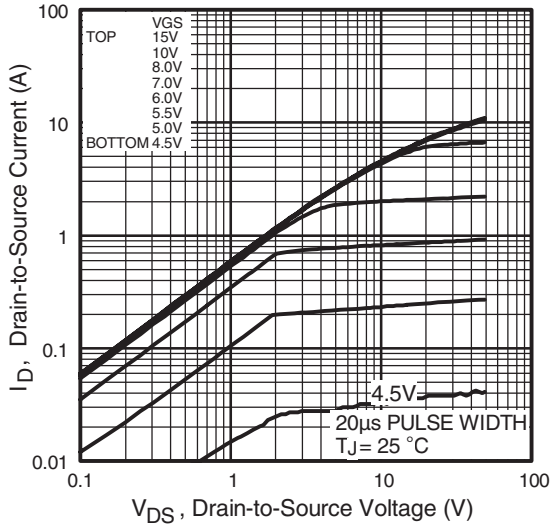


Fig. 1 - Typical Output Characteristics

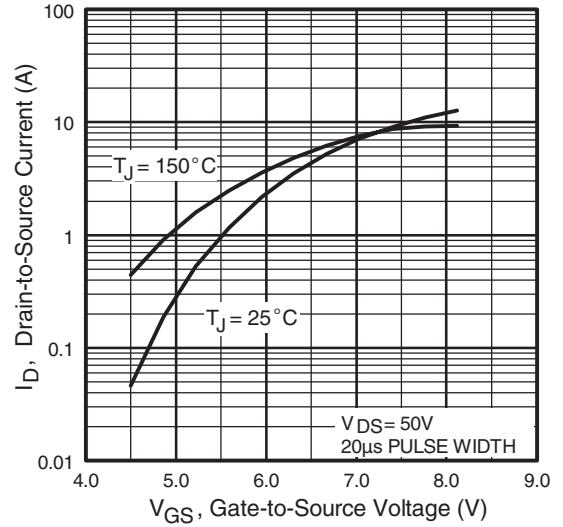


Fig. 3 - Typical Transfer Characteristics

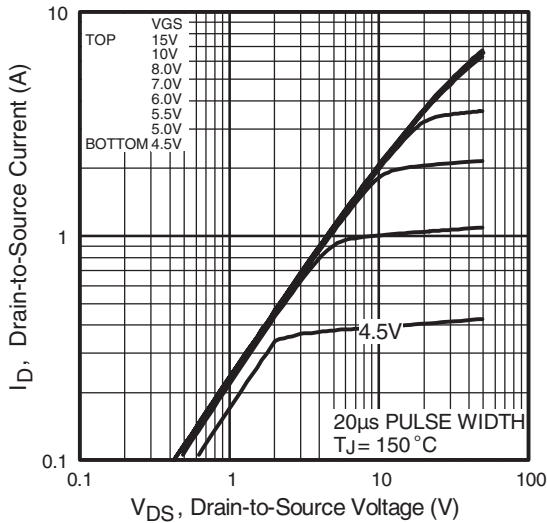


Fig. 2 - Typical Output Characteristics

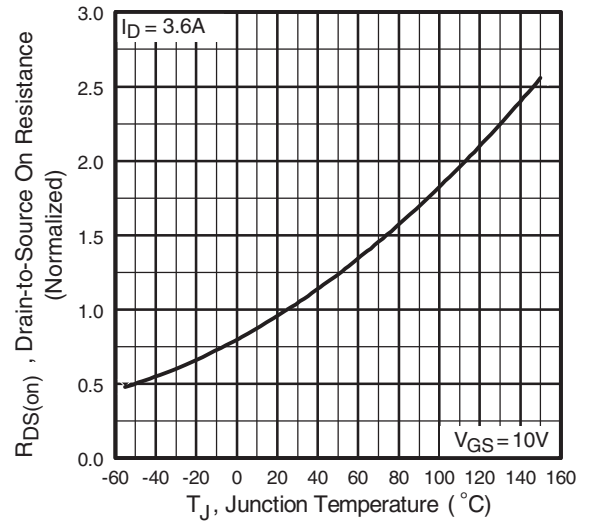


Fig. 4 - Normalized On-Resistance vs. Temperature

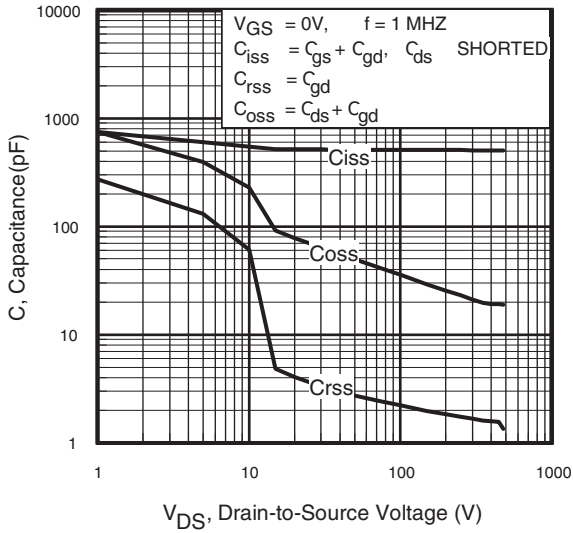


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

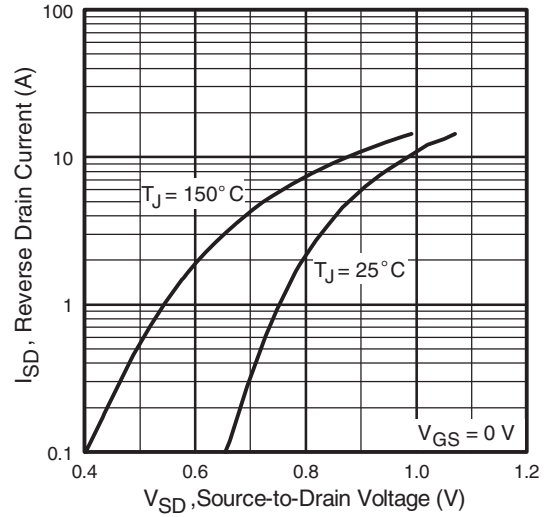


Fig. 7 - Typical Source-Drain Diode Forward Voltage

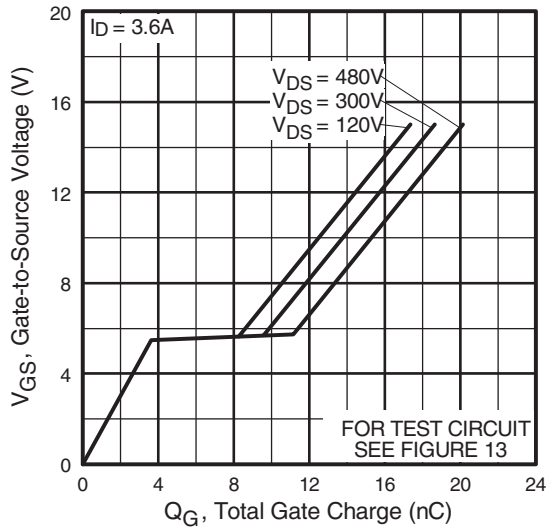


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

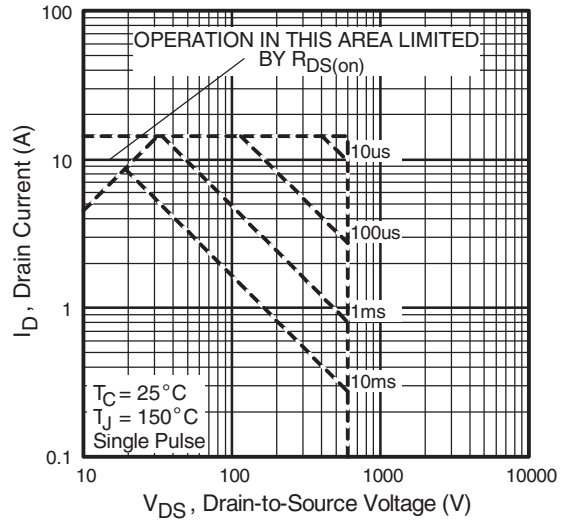


Fig. 8 - Maximum Safe Operating Area

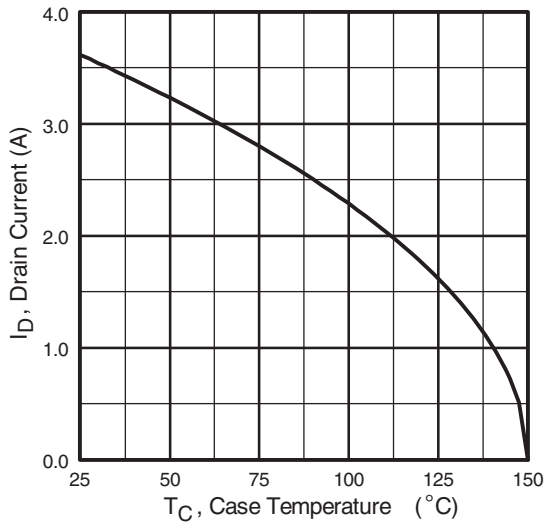


Fig. 9 - Maximum Drain Current vs. Case Temperature

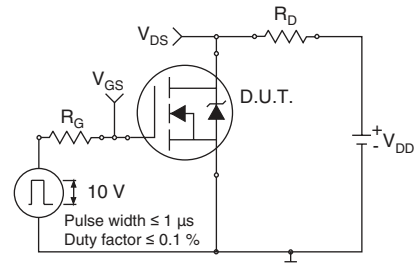


Fig. 10a - Switching Time Test Circuit



Fig. 10b - Switching Time Waveforms

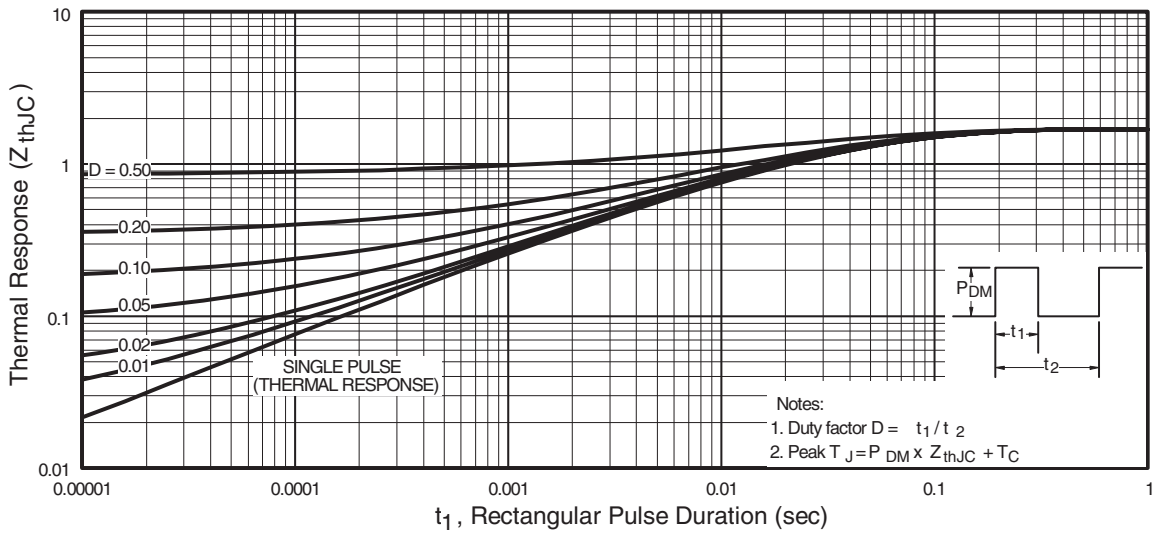


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

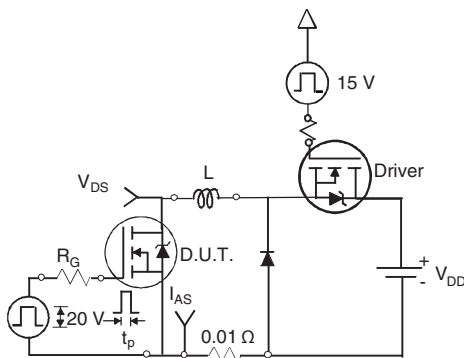


Fig. 12a - Unclamped Inductive Test Circuit

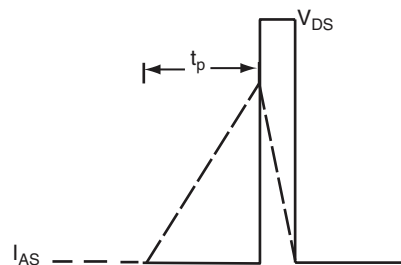


Fig. 12b - Unclamped Inductive Waveforms

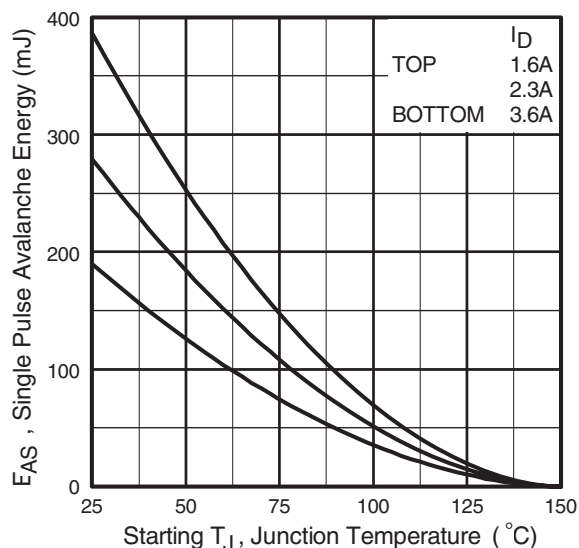


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

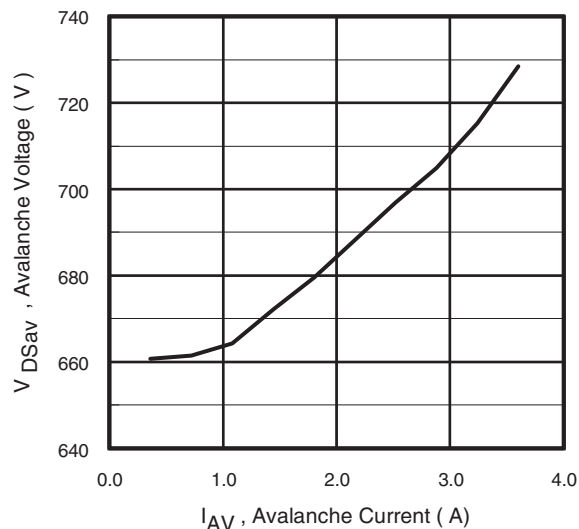


Fig. 12d - Typical Drain-to-Source Voltage vs. Avalanche Current

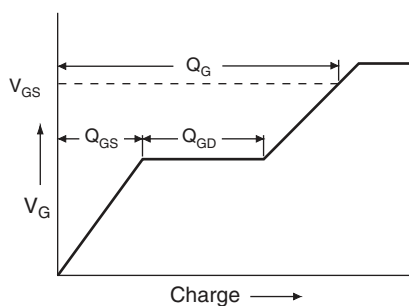


Fig. 13a - Basic Gate Charge Waveform

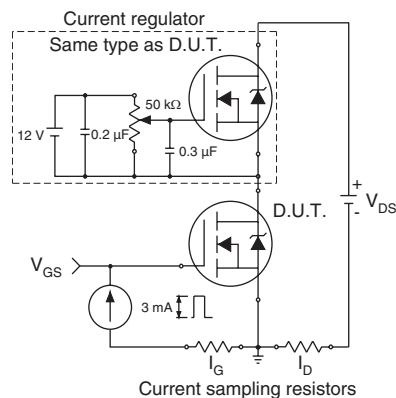


Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit

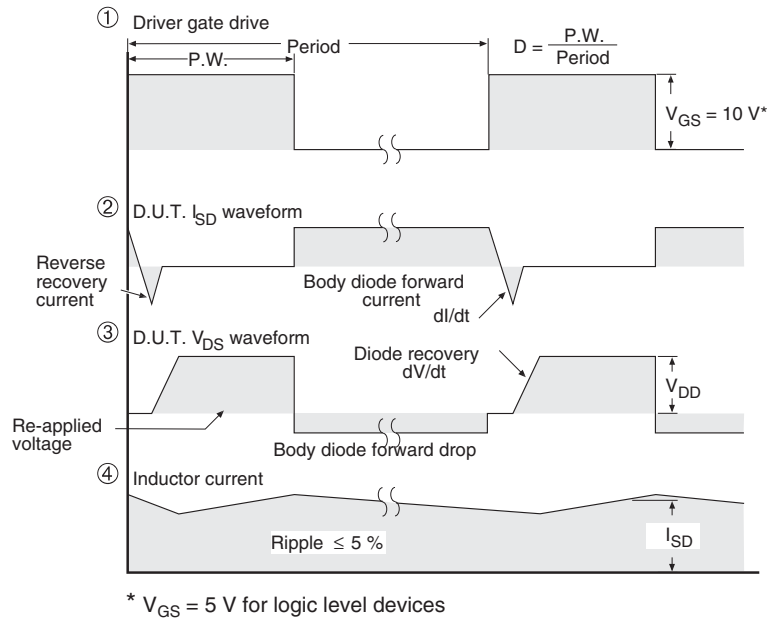
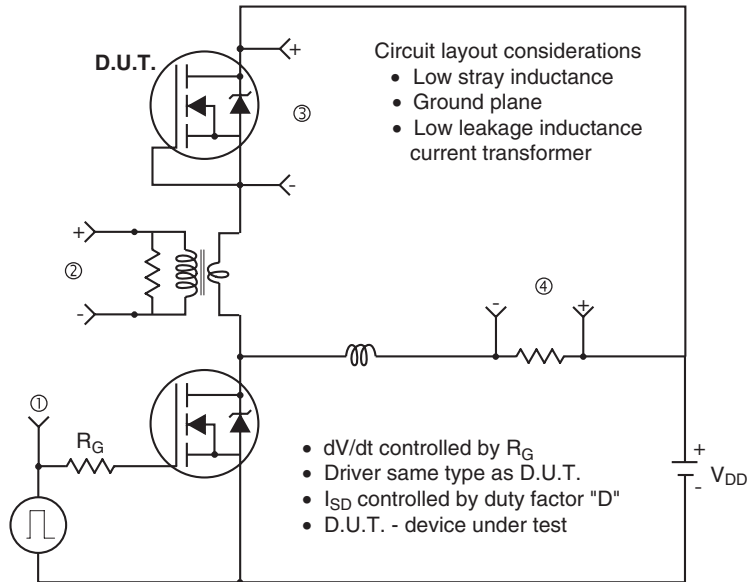


Fig. 14 - For N-Channel

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