

8Kx9 Static RAM

Features

- **High speed**
— $t_{AA} = 25 \text{ ns}$
- **x9 organization is ideal for cache memory applications**
- **CMOS for optimum speed/power**
- **Low active power**
— 770 mW
- **Low standby power**
— 195 mW
- **TTL-compatible inputs and outputs**
- **Automatic power-down when deselected**
- **Easy memory expansion with \overline{CE}_1 , CE_2 , OE options**

Functional Description

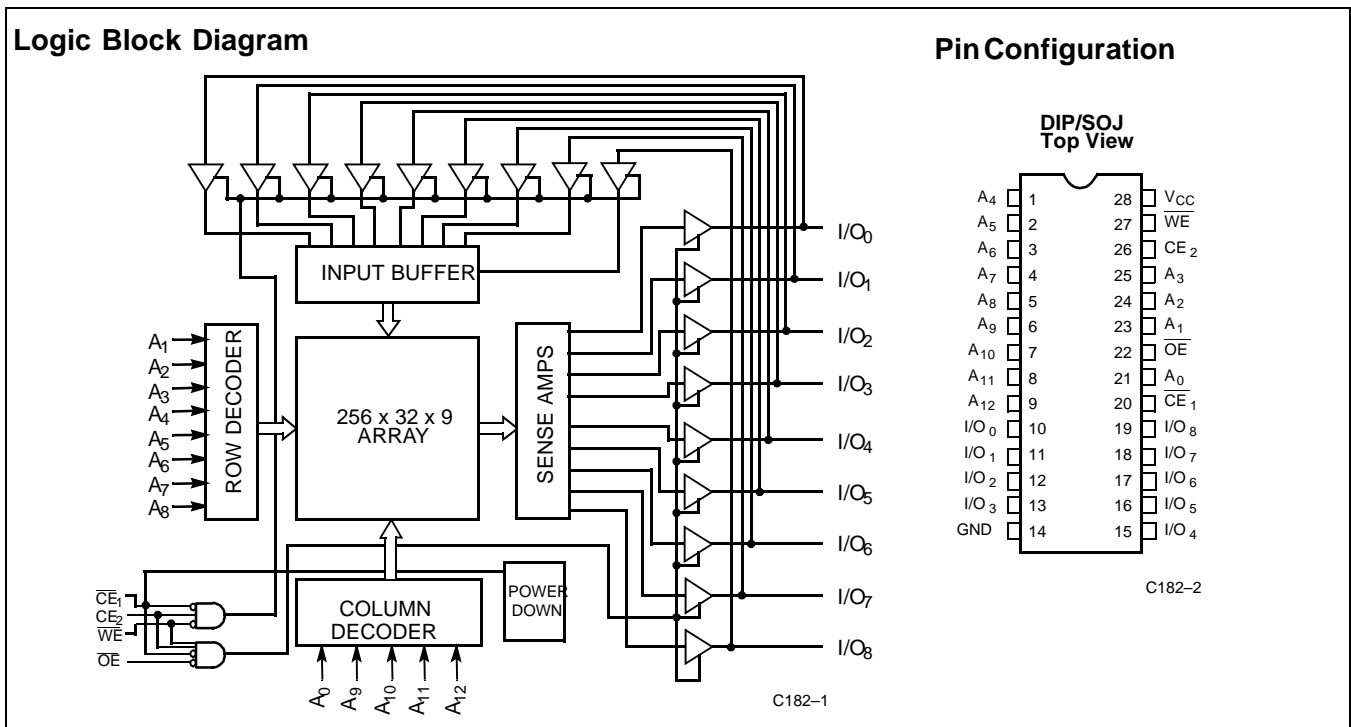
The CY7C182 is a high-speed CMOS static RAM organized as 8,192 by 9 bits and it is manufactured using Cypress's high-performance CMOS technology. Access times as fast as 25 ns are available with maximum power consumption of only 770 mW.

The CY7C182, which is oriented toward cache memory applications, features fully static operation requiring no external clocks or timing strobes. The automatic power-down feature reduces the power consumption by more than 70% when the circuit is deselected. Easy memory expansion is provided by an active-LOW Chip Enable (\overline{CE}_1), an active-HIGH Chip Enable (CE_2), an active-LOW Output Enable (\overline{OE}), and three-state drivers.

An active-LOW Write Enable signal (\overline{WE}) controls the writing/reading operation of the memory. When \overline{CE}_1 and \overline{WE} inputs are both LOW, data on the nine data input/output pins (I/O_0 through I/O_8) is written into the memory location addressed by the address present on the address pins (A_0 through A_{12}). Reading the device is accomplished by selecting the device and enabling the outputs, (\overline{CE}_1 and \overline{OE} active LOW and CE_2 active HIGH), while (\overline{WE}) remains inactive or HIGH. Under these conditions, the contents of the location addressed by the information on address pins is present on the nine data input/output pins.

The input/output pins remain in a high-impedance state unless the chip is selected, outputs are enabled, and write enable (\overline{WE}) is HIGH.

A die coat is used to insure alpha immunity.



Selection Guide

| | 7C182-25 | 7C182-35 | 7C182-45 |
|--------------------------------|----------|----------|----------|
| Maximum Access Time (ns) | 25 | 35 | 45 |
| Maximum Operating Current (mA) | 140 | 140 | 140 |
| Maximum Standby Current (mA) | 35 | 35 | 35 |

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

| | |
|--|-----------------|
| Storage Temperature | -65°C to +150°C |
| Ambient Temperature with Power Applied..... | -55°C to +125°C |
| Supply Voltage to Ground Potential ^[1] | -0.5V to +7.0V |
| DC Voltage Applied to Outputs in High Z State ^[1] | -0.5V to +7.0V |
| DC Input Voltage ^[1] | -0.5V to +7.0V |

| | |
|--|---|
| Output Current into Outputs (LOW)..... | 20 mA |
| Static Discharge Voltage | >2001V (per MIL-STD-883, Method 3015.2) |
| Latch-Up Current..... | >200 mA |

Operating Range

| Range | Ambient Temperature | V _{CC} |
|------------|---------------------|-----------------|
| Commercial | 0°C to +70°C | 5V ± 10% |

Electrical Characteristics Over the Operating Range

| Parameter | Description | Test Conditions | 7C182-25, 35, 45 | | Unit |
|-----------------|---|--|------------------|-----------------|------|
| | | | Min. | Max. | |
| V _{OH} | Output HIGH Voltage | V _{CC} Min., I _{OH} = -4.0 mA. | 2.4 | | V |
| V _{OL} | Output LOW Voltage | V _{CC} Min., I _{OL} = 8.0 mA | | 0.4 | V |
| V _{IH} | Input HIGH Voltage | | 2.2 | V _{CC} | V |
| V _{IL} | Input LOW Voltage ^[1] | | -0.5 | 0.8 | V |
| I _{IX} | Input Load Current | GND ≤ V _{IN} ≤ V _{CC} , GND < V _{OUT} < V _{CC} , Output Disabled | -10 | +10 | μA |
| I _{OZ} | Output Leakage Current | V _{CC} = Max., V _{OUT} = GND | -10 | +10 | μA |
| I _{OS} | Output Short Circuit Current ^[2] | V _{CC} = Max., V _{OUT} = GND | | -300 | mA |
| I _{CC} | V _{CC} Operating Circuit Current | V _{CC} Max., Output Current = 0 mA, f = Max., V _{IN} = V _{CC} or GND | | 140 | mA |
| | Automatic Power-Down Current — TTL Inputs | Max V _{CC} , $\overline{CE}_1 \geq V_{IH}$, CE ₂ ≤ V _{IL} , V _{IN} ≥ V _{IH} or V _{IN} ≤ V _{IL} , f = f _{MAX} | | 35 | mA |
| | Automatic Power-Down Current — CMOS Inputs | Max V _{CC} , $\overline{CE}_1 \geq V_{CC} - 0.3V$, CE ₂ ≤ 0.3V, V _{IN} ≥ V _{CC} - 0.3V or V _{IN} ≤ 0.3V, f = 0 | | 20 | mA |

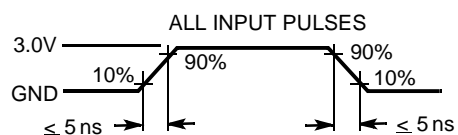
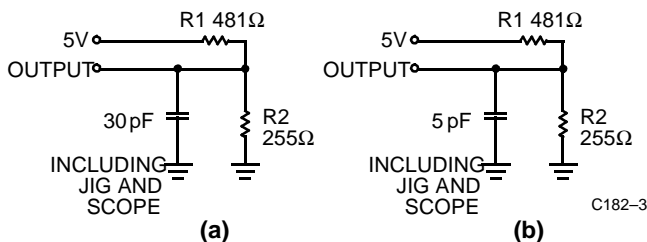
Capacitance^[3]

| Parameter | Description | Test Conditions | Max. | Unit |
|------------------|--------------------|---|------|------|
| C _{OUT} | Output Capacitance | T _A = 25°C, f = 1 MHz, V _{CC} = 5.0V | 10 | pF |
| C _{IN} | Input Capacitance | | 10 | pF |

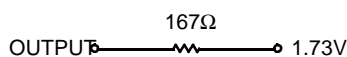
Note:

- V_{IL} (min.) = -3.0V for pulse durations of less than 20 ns.
- Duration of the short circuit should not exceed 30 seconds. Not more than one output should be shorted at one time.
- Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT

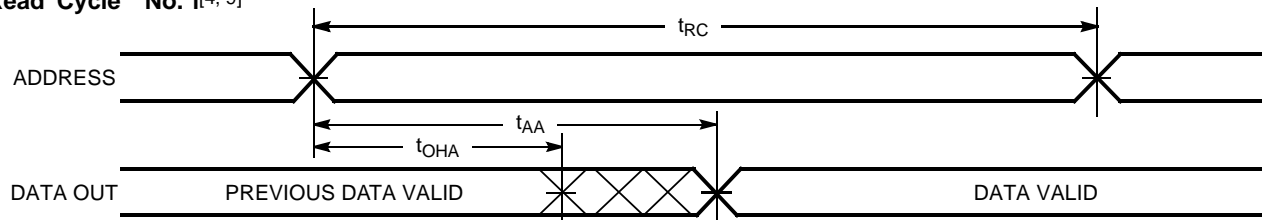


Switching Characteristics Over the Operating Range

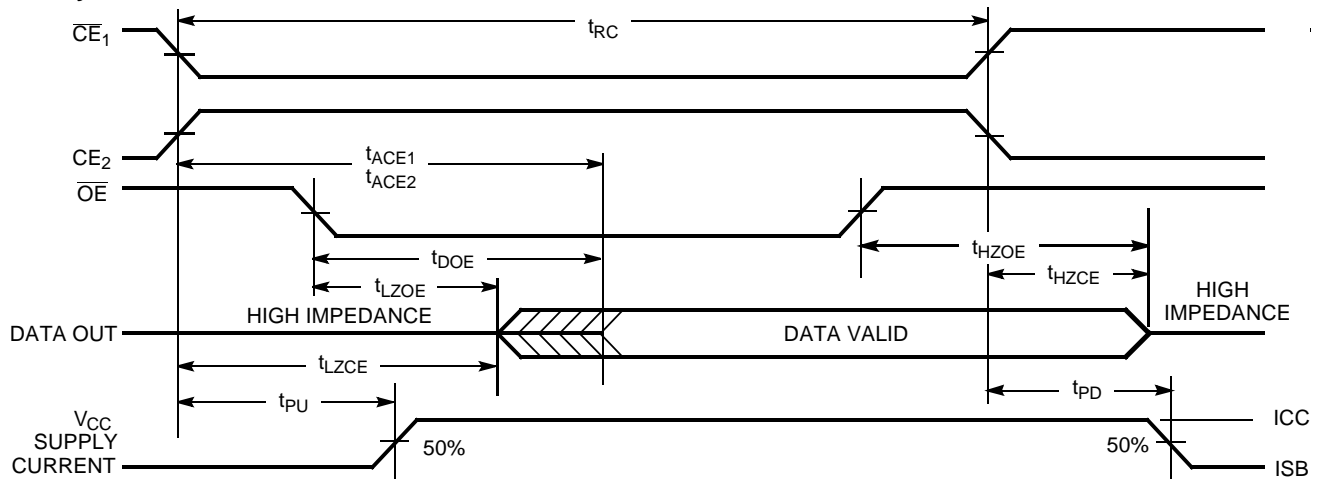
| Parameter | Description | 7C182-25 | | 7C182-35 | | 7C182-45 | | Unit |
|----------------------------------|---|----------|------|----------|------|----------|------|------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| READ CYCLE^[4] | | | | | | | | |
| t _{RC} | Read Cycle Time | 25 | | 35 | | 45 | | ns |
| t _{AA} | Address to Data Valid | | 25 | | 35 | | 45 | ns |
| t _{OHA} | Data Hold from Address Change | 3 | | 3 | | 3 | | ns |
| t _{ACE1} | \overline{CE}_1 Access Time | | 25 | | 35 | | 45 | ns |
| t _{ACE2} | \overline{CE}_2 Access Time | | 25 | | 35 | | 45 | ns |
| t _{LZCE1} | \overline{CE}_1 LOW to Low Z | 5 | | 5 | | 5 | | ns |
| t _{LZCE2} | \overline{CE}_2 HIGH to Low Z | 5 | | 5 | | 5 | | ns |
| t _{HZCE1} | \overline{CE}_1 HIGH to High Z ^[5] | | 18 | | 20 | | 25 | ns |
| t _{HZCE2} | \overline{CE}_2 LOW to High Z ^[5] | | 18 | | 20 | | 25 | ns |
| t _{PU} | \overline{CE}_1 LOW to Power-Up | 0 | | 0 | | 0 | | ns |
| t _{PD} | \overline{CE}_1 HIGH to Power-Down | | 20 | | 20 | | 25 | ns |
| t _{DOE} | \overline{OE} Access Time | | 18 | | 20 | | 20 | ns |
| t _{LZOE} | \overline{OE} LOW to Low Z | 3 | | 3 | | 3 | | ns |
| t _{HZOE} | \overline{OE} HIGH to High Z ^[5] | | 18 | | 20 | | 25 | ns |
| WRITE CYCLE^[6] | | | | | | | | |
| t _{WC} | Write Cycle Time | 25 | | 35 | | 45 | | ns |
| t _{SA} | Address Set-Up Time | 0 | | 0 | | 0 | | ns |
| t _{AW} | Address Valid to End of Write | 20 | | 30 | | 40 | | ns |
| t _{SD} | Data Set-Up Time | 15 | | 20 | | 25 | | ns |
| t _{SCE1} | \overline{CE}_1 LOW to Write End | 20 | | 30 | | 40 | | ns |
| t _{SCE2} | \overline{CE}_2 HIGH to Write End | 20 | | 30 | | 40 | | ns |
| t _{PWE} | \overline{WE} Pulse Width | 20 | | 25 | | 30 | | ns |
| t _{HA} | Address Hold from End of Write | 0 | | 0 | | 0 | | ns |
| t _{HD} | Data Hold Time | 0 | | 0 | | 0 | | ns |
| t _{LZWE} | Write HIGH to Low Z ^[7] | 3 | | 3 | | 3 | | ns |
| t _{HZWE} | Write LOW to High Z ^[5, 7, 8] | | 13 | | 15 | | 20 | ns |

Notes:

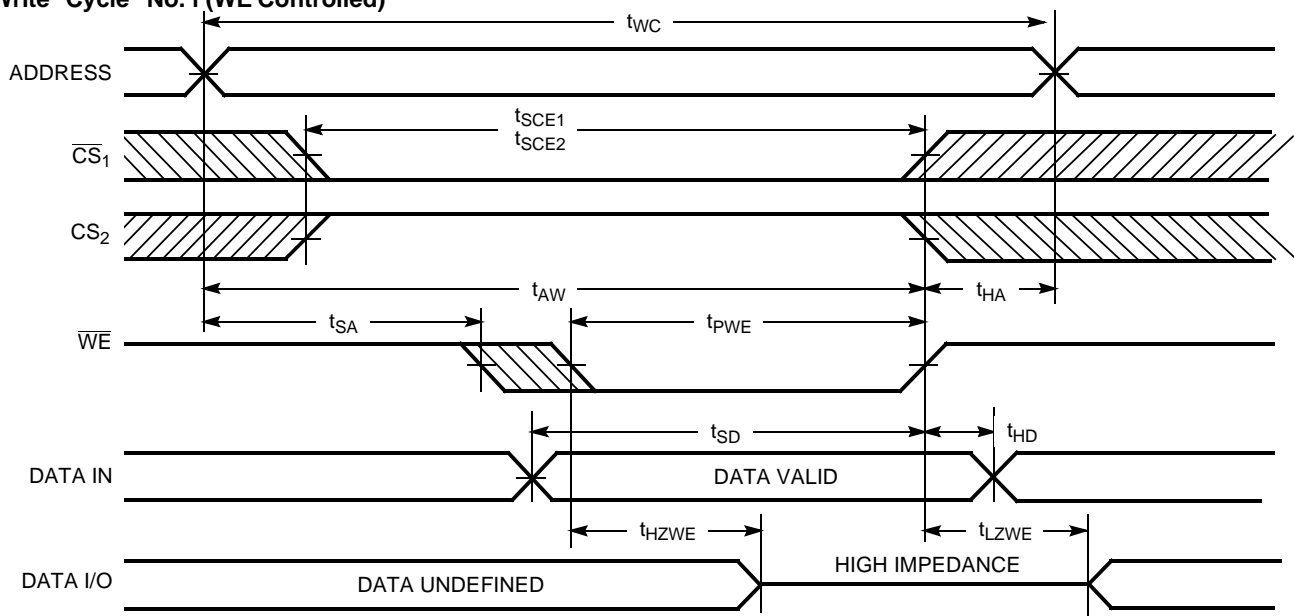
4. \overline{WE} is HIGH for read cycle.
5. t_{HZCE} and t_{HZWE} are specified with C_L = 5 pF. Transition is measured ± 500 mV from steady-state voltage.
6. The internal write time of the memory is defined by the overlap of \overline{CE}_1 LOW, \overline{CE}_2 HIGH, and \overline{WE} LOW. All three signals must be asserted to initiate a write and any signal can terminate a write by being deasserted. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
7. At any given temperature and voltage condition, t_{LZWE} is less than t_{HZWE} for any given device. These parameters are sampled and not 100% tested.
8. Address valid prior to or coincident with \overline{CE} transition LOW and \overline{CE}_2 transition HIGH.

Switching Waveforms
Read Cycle No. 1^[4, 9]


C182-5

Read Cycle No. 2^[4, 10]


C182-6

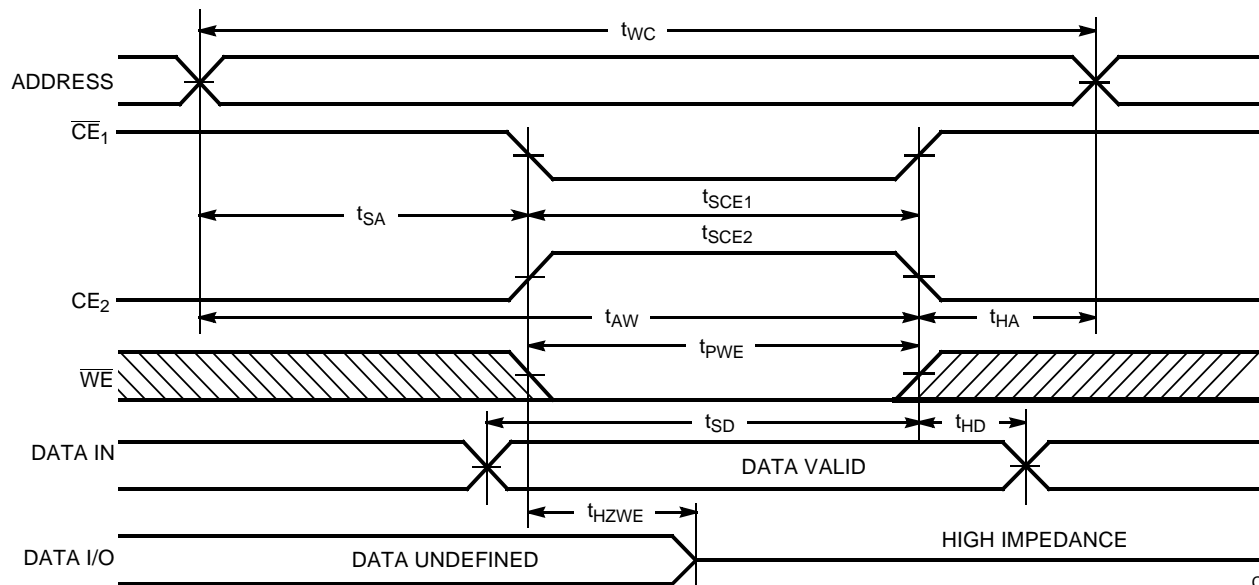
Write Cycle No. 1 (WE Controlled)^[6]


C182-7

Notes:

9. Device is continuously selected. \overline{OE} , $\overline{CE}_1 = V_{IL}$. $CE_2 = V_{IH}$.
10. If \overline{CE}_1 goes HIGH and CE_2 goes LOW simultaneously with WE HIGH, the output remains in a high-impedance state.

Switching Waveforms (continued)

Write Cycle No.2 (\overline{CE} Controlled) ^[6, 10]


C182-8

Truth Table

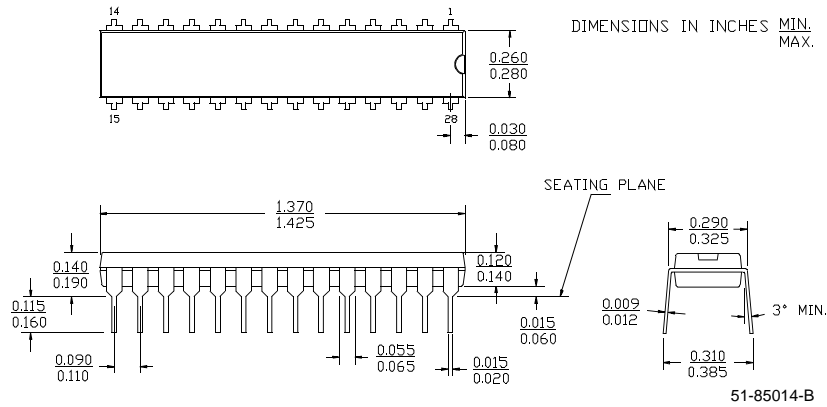
| CE ₁ | CE ₂ | OE | WE | Data In | Data Out | Mode |
|-----------------|-----------------|----|----|---------|----------|---------------------|
| H | X | X | X | Z | Z | Deselect/Power-Down |
| L | H | L | H | Z | Valid | Read |
| L | H | X | L | Valid | Z | Write |
| L | H | H | H | Z | Z | Output Disable |
| X | L | X | X | Z | Z | Deselect |

Ordering Information

| Speed (ns) | Ordering Code | Package Name | Package Type | Operating Range |
|------------|---------------|--------------|------------------------------|-----------------|
| 25 | CY7C182-25PC | P21 | 28-Lead (300-Mil) Molded DIP | Commercial |
| | CY7C182-25VC | V21 | 28-Lead Molded SOJ | |
| 35 | CY7C182-35PC | P21 | 28-Lead (300-Mil) Molded DIP | Commercial |
| | CY7C182-35VC | V21 | 28-Lead Molded SOJ | |
| 45 | CY7C182-45PC | P21 | 28-Lead (300-Mil) Molded DIP | Commercial |
| | CY7C182-45VC | V21 | 28-Lead Molded SOJ | |

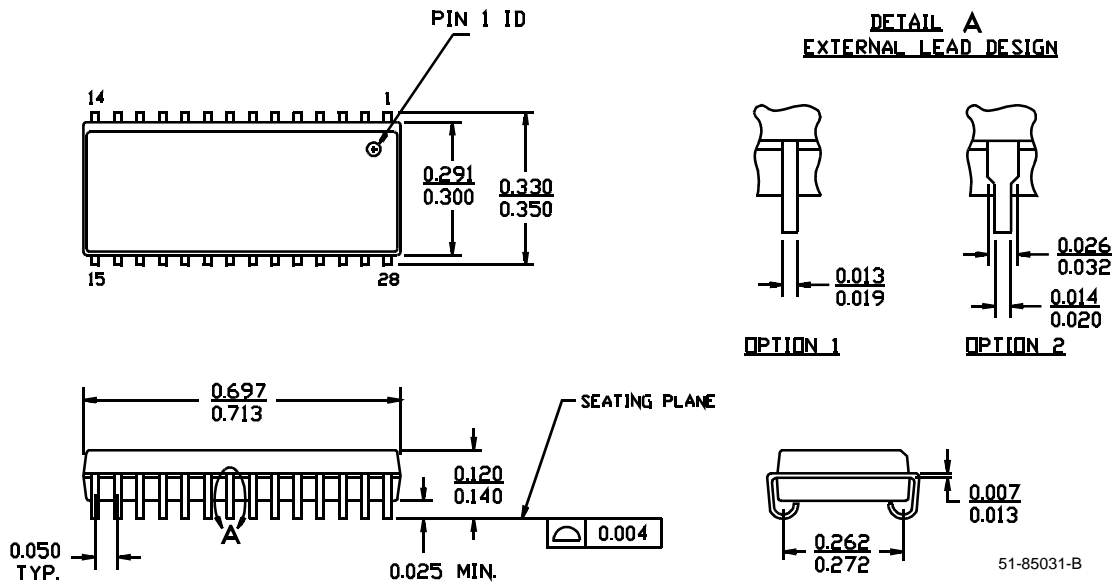
Package Diagrams

28-Lead (300-Mil) Molded DIP P21



28-Lead (300-Mil) Molded SOJ V21

DIMENSIONS IN INCHES MIN. MAX.



| Document Title: CY7C182 8K x 9 Static RAM Document Number: 38-05031 | | | | |
|--|---------|------------|-----------------|---|
| REV. | ECN NO. | Issue Date | Orig. of Change | Description of Change |
| ** | 106825 | 09/15/01 | SZV | Change from Spec number: 38-00110 to 38-05031 |