AvnetCore: Datasheet

Double Data Rate SDRAM Controller

Block Diagram

Intended Use:

— Supports All Standard DDR SDRAM Memory Types
— High-Speed Networking
— Embedded Computing
— Digital Video

Features:

— DDR SDRAM dynamic burst length support for burst lengths of 2, 4, or 8 per access
— Supports DRAM data path widths of 16, 32, 64, and 72 bits
— Supports multiple bank interleaving with read and write commands, and all read and write commands are issued at the earliest possible time with maximum efficiency
— CAS latency 2.0 support
— Support for the following commands: NOP, LOAD_MODE, READ, READ w/ AUTO_PRECHARGE, WRITE, WRITE w/ AUTO_PRECHARGE, and AUTO_REFRESH
— Data mask support for write operations
— Support for 4 internal banks
— Controller provides automatic management of all four SDRAM memory banks simultaneously

Targeted Devices:

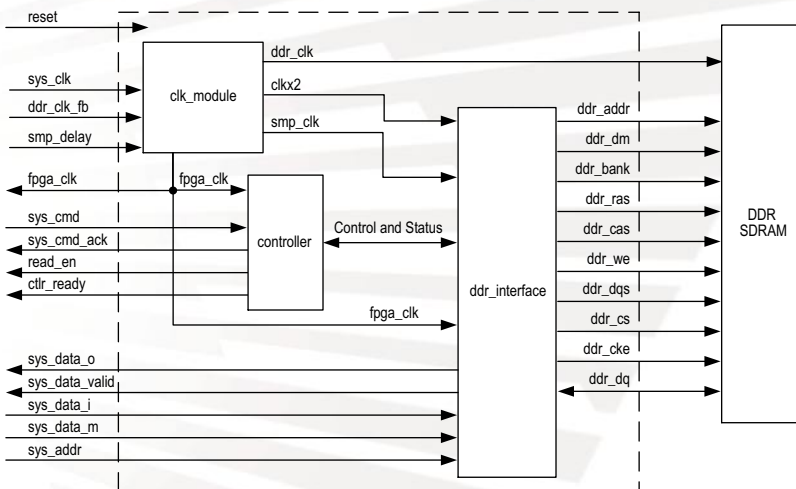— Axcelerator® Family
— ProASIC®3 Family

Core Deliverables:

— Netlist Version
  > Netlist compatible with the Actel Designer place and route tool
— RTL Version
  > VHDL Source Code
  > Test Bench
— All
  > User Guide

Synthesis and Simulation Support:

— Synthesis: Synplicity®
— Simulation: Model*Sim*®
— Other tools supported upon request

Verification:

— Test Bench
— Test Vectors

This core conforms to the appropriate standard(s). In general, standards do not define the internal user interface, only the external interfaces and protocols. Therefore, Avnet Memec has created a simple FIFO interface to this core for easy user connectivity. Please consult the appropriate standards document for all external signaling. The Double Data Rate (DDR) Synchronous Dynamic Random Access Memory (SDRAM) controller pro-vides the user with a simplified interface to industry standard memory devices. The controller has been targeted to the Actel Axcelerator® and ProASIC®3 families of platform FPGAs and can be reconfigured to provide a solution customized to the user's needs based on system and memory-specific require-ments. The DDR SDRAM controller offers full support for SDRAM bank and row management, supports four bank interleaving between commands, and executes all commands with maximum efficiency. The extensive feature list makes this an extremely flexible and efficient core to use.

Functional Description

The DDR SDRAM Controller core is partitioned into modules as shown in the block diagram and as described below.

CONTROLLER

The Controller module contains the main state machine, which controls the SDRAM accesses. The Controller is responsible for SDRAM bus arbitration, command interpreting, bank-interleaving, and timing issues. The Controller instructs the ddr_interface module when to perform writes and reads from the DDR data bus.

DDR INTERFACE

The DDR Interface (ddr_interface) module is responsible for maintaining the bi-directional ddr_data bus, and for asserting all address and command signals to the SDRAM. For a write operation, this module reads from the larger sys_data bus and, using the 2x clock and muxes, constructs the DDR data bus, writing out a new value on every rising edge of the 2x clock which is strobed into the DDR SDRAM with ddr_dqs. For read operations, the opposite must occur. The Data Path reads in the DDR data using sys_clk_fb rising edge as the time reference, and de-muxes the data into two separate 1x clock pipelines. These two 1x clock pipelines are then concatenated to form the larger sys_data bus, which is provided to the user.

CLOCK MODULE

The Clock module (clk_module) instantiates all of the PLLs and global clocks required for the DDR Core. One PLL creates a 1x de-skewed clock that is fed to most of the logic in the core, plus it also creates a 2x clock which generates the 2X DDR related clocks used for write-related operations. The other PLL generates a delayed clock that is used in the read-related operations.
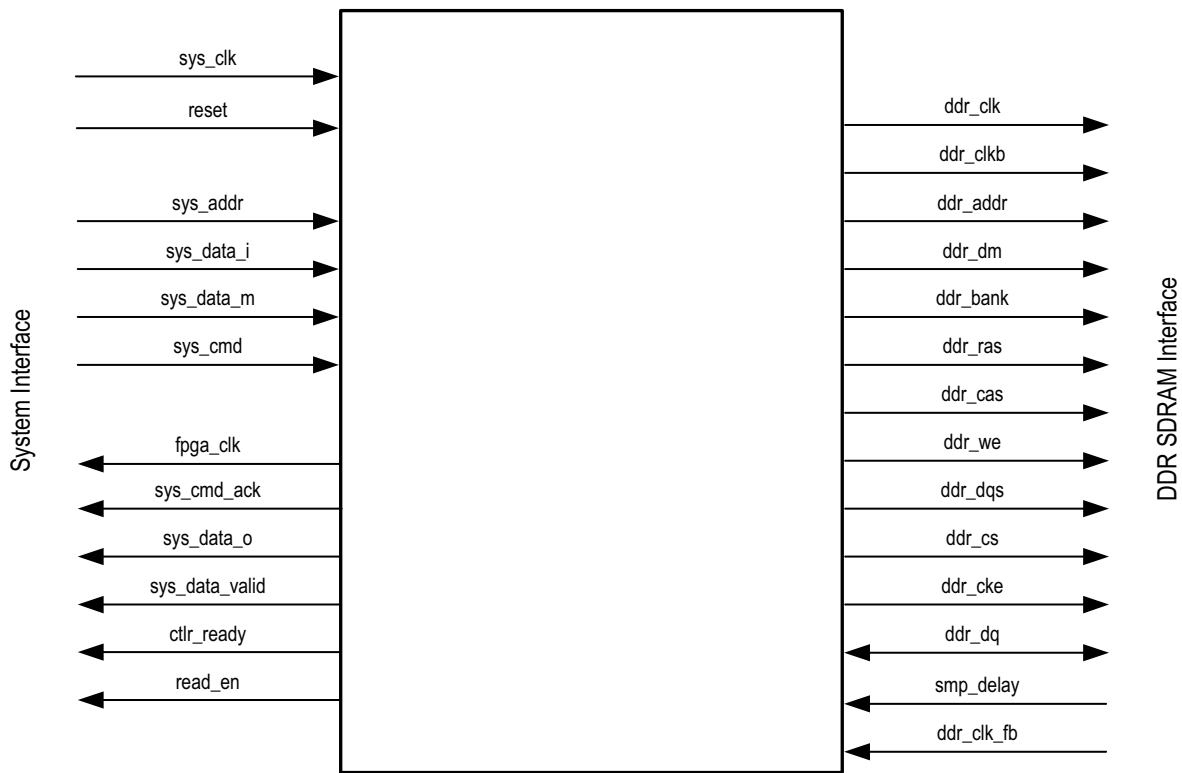

Figure 1: MC-ACT-SDRAMDDR Logic Symbol

Family	Device	Utilization			Performance
		COMB	SEQ	Total	
Axcelerator	AX250-2	20%	40%	27%	100 MHz

Table 1: Device Utilization and Performance

Verification and Compliance
Functional and timing simulation has been performed on the DDR SDRAM Controller using VHDL Test Benches. Simulation vectors used for verification are provided with the core.

Signal Descriptions
The following signal descriptions define the IO signals.

	Signal	Direction	Width	Description
Global Signals	SYS_CLK	Input	1	System clock
	DDR_CLK_FB	Input	1	ddr_clk from DDR SDRAM
	FPGA_CLK	Output	1	primary H-CLOCK clock used by core and available for host interface
	RESET	Input	1	Active high system reset
Interface to System	SYS_DATA_I	Input	SYS_DATA_BITS	System write data
	SYS_DATA_M	Input	SYS_MASK_BITS	System write data mask
	SYS_ADDR	Input	SYS_ADDR_BITS	System address
	SYS_CMD	Input	7	DDR command bus
	SYS_DATA_O	Output	SYS_DATA_BITS	System read data
	SYS_DATA_VALID	Output	1	High when sys_data_o is valid
	SYS_CMD_ACK	Output	1	High when command is accepted
	CTLR_READY	Output	1	High when controller can accept a cmd
	READ_EN	Output	1	When high, controller needs new data in 2 clocks
Interface to DDR SDRAM	DDR_ADDR	Output	DDR_ADDR_BITS	DDR SDRAM address bus
	DDR_DQ	Output	DDR_DATA_BITS	DDR SDRAM data bus
	DDR_DQS	Input/Output	8	DDR SDRAM data strobe
	DDR_RAS	Input/Output	1	DDR SDRAM row address strobe
	DDR_CAS	Output	1	DDR SDRAM column address strobe
	DDR_WE	Output	1	DDR SDRAM write enable
	DDR_BANK	Output	DDR_BANK_BITS	DDR SDRAM bank bus
	DDR_CLK	Output	1	DDR SDRAM clock
	DDR_CLKB	Output	1	DDR SDRAM inverted clock
	DDR_CS	Output	1	DDR SDRAM chip select
	DDR_CKE	Output	1	DDR SDRAM clock enable
	DDR_DM	Output	DDR_MASK_BITS	DDR SDRAM data mask bus

Table 2: Core I/O Signals

Timing

All timing diagrams assume that all banks were previously closed, and that BURST-4 accesses were issued. All timing is based on a 100 MHz sys_clk.
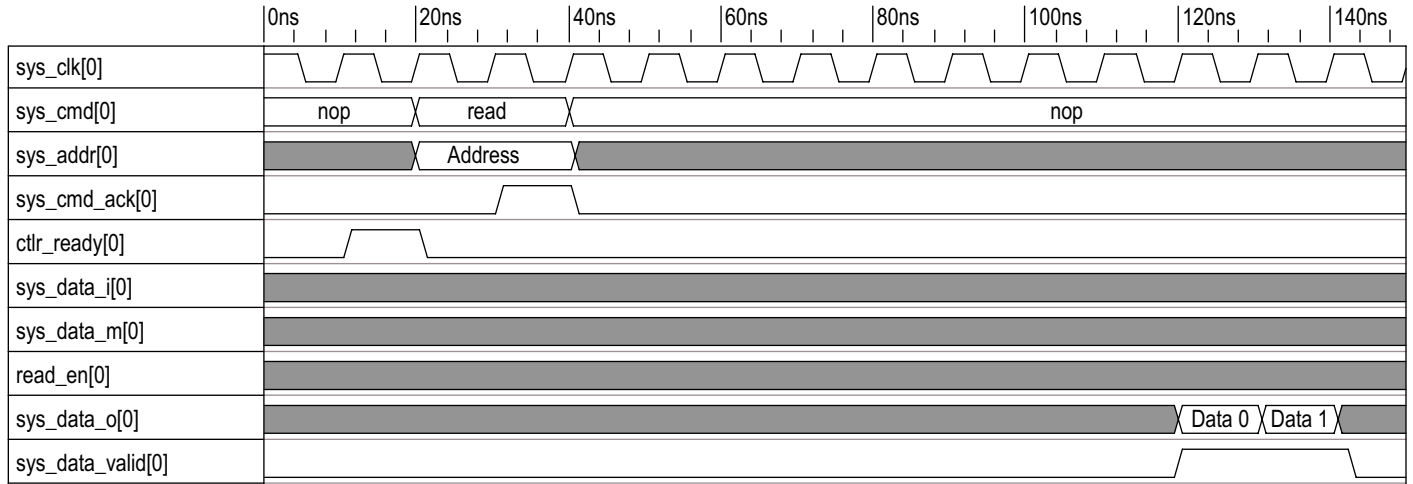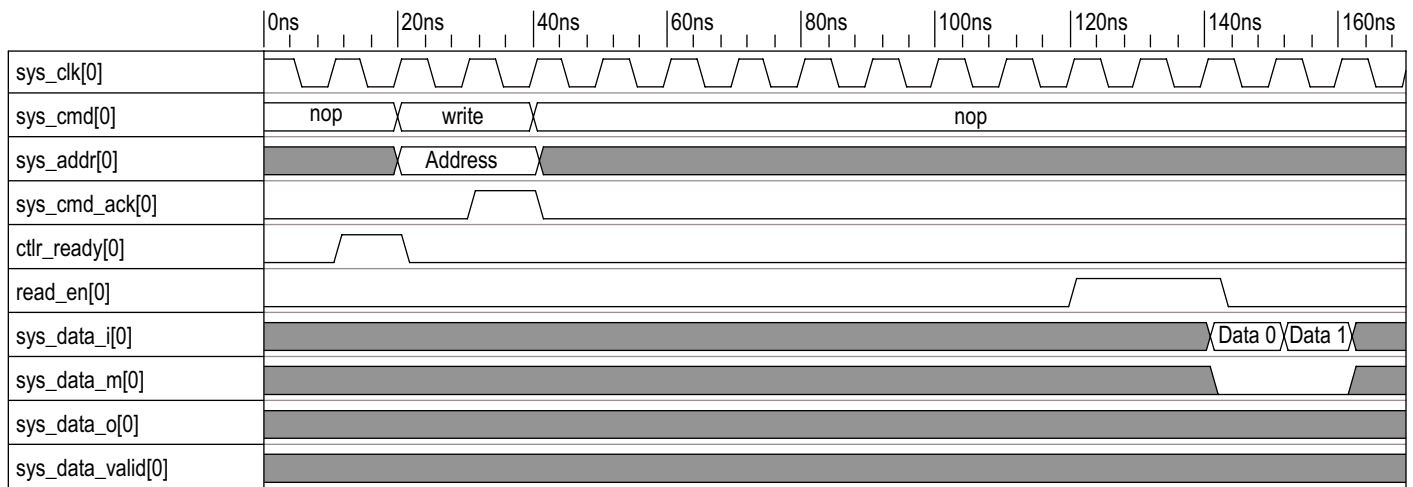
Figure 3: Read Command

Figure 4: Write Command

Recommended Design Experience

For the source version, users should be familiar with HDL entry and Actel design flows. Users should be familiar with Actel Libero Integrated Design Environment (IDE) and preferably with Synplify and Model*Sim*. Users should also have experience with microprocessor systems and asynchronous communication controllers.

Ordering Information

The CORE is provided under license from Avnet Memec for use in Actel programmable logic devices. Please contact Avnet Memec for pricing and more information.

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Ordering Information:

Part Number	Hardware	Resale
MC-ACT-SDRAMDDR-NET	Actel DDR SDRAM Controller Netlist	Contact for pricing
MC-ACT-SDRAMDDR-VHDL	Actel DDR SDRAM Controller VHDL	Contact for pricing

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