HA17902 Series

Quad Operational Amplifier

REJ03D0685-0100
(Previous: ADE-204-045)
Rev.1.00
Jun 15, 2005

Description

The HA17902 is an internal phase compensation quad operational amplifier that operates on a single-voltage power supply and is appropriate for use in a wide range of general-purpose control equipment.

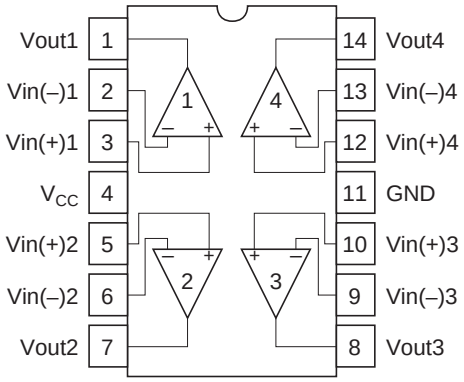
Features

- Wide usable power-supply voltage range and single-voltage supply operation
- Internal phase compensation
- Wide common-mode voltage range and operation for inputs close to the 0 level

Ordering Information

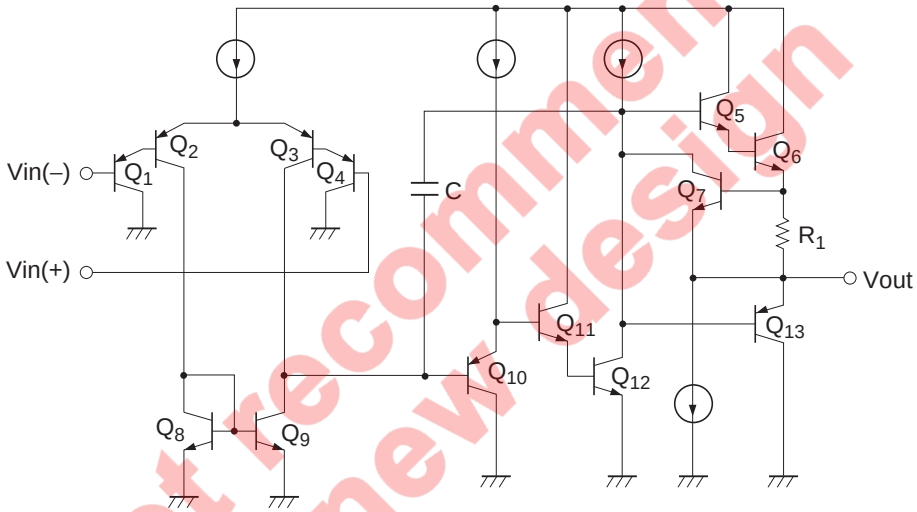
Type No.	Application	Package Code (Previous Code)
HA17902PJ	Car use	PRDP0014AB-A (DP-14)
HA17902FPJ		PRSP0014DF-B (FP-14DAV)
HA17902FPK		PRSP0014DF-B (FP-14DAV)

Pin Arrangement



(Top view)

Circuit Structure (1/4)



Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	HA17902PJ	HA17902 FPJ	HA17902FPK	Unit
Power supply voltage	V_{CC}	28	28	28	V
Sink current	Io sink	50	50	25	mA
Allowable power dissipation	P_T	625*[1]	625*[2]	625*[2]	mW
Common-mode input voltage	V_{CM}	–0.3 to V_{CC}	–0.3 to V_{CC}	–0.3 to V_{CC}	V
Differential-mode input voltage	Vin(diff)	±V_{CC}	±V_{CC}	±V_{CC}	V
Operating temperature	Topr	–40 to +85	–40 to +85	–40 to +125	°C
Storage temperature	Tstg	–55 to +125	–55 to +125	–55 to +150	°C

Notes: 1. These are the allowable values up to Ta = 50°C. Derate by 8.3mW/°C above that temperature.
2. See notes on SOP Package Usage in Reliability section.

Electrical Characteristics 1

(V_{CC} = + 15V, Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Input offset voltage	V_{IO}	—	3	8	mV	V_{CM} = 7.5V, R_S = 50Ω, Rf = 5kΩ
Input offset current	I_{IO}	—	5	50	nA	I_{IO} = | I_I^- – I_I^+ |, V_{CM} = 7.5V
Input bias current	I_{IB}	—	30	500	nA	V_{CM} = 7.5V
Power-supply rejection ratio	PSRR	—	93	—	dB	f = 100Hz, R_S = 1kΩ, Rf = 100kΩ
Voltage gain	A_{VD}	75	90	—	dB	R_S = 1kΩ, Rf = 100kΩ, RL = ∞
Common-mode rejection ratio	CMR	—	80	—	dB	R_S = 50Ω, Rf = 5kΩ
Common-mode input voltage range	V_{CM}	–0.3	—	13.5	V	R_S = 1kΩ, Rf = 100kΩ, f = 100Hz
Maximum output voltage amplitude	V_{OP-P}	—	13.6	—	V	f = 100Hz, R_S = 1kΩ, Rf = 100kΩ, R_L = 20kΩ
Output voltage	V_{OH1}	13.2	13.6	—	V	I_{OH} = –1mA
	V_{OH2}	12	13.3	—	V	I_{OH} = –10mA
	V_{OL1}	—	0.8	1	V	I_{OL} = 1mA
	V_{OL2}	—	1.1	1.8	V	I_{OL} = 10mA
Output source current	Io source	15	—	—	mA	V_{OH} = 10V
Output sink current	Io sink	3	9	—	mA	V_{OL} = 1V
Supply current	I_{CC}	—	0.8	2	mA	Vin = GND, R_L = ∞
Slew rate	SR	—	0.19	—	V/µs	f = 1.5kHz, V_{CM} = 7.5V, R_L = ∞
Channel separation	CS	—	120	—	dB	f = 1kHz

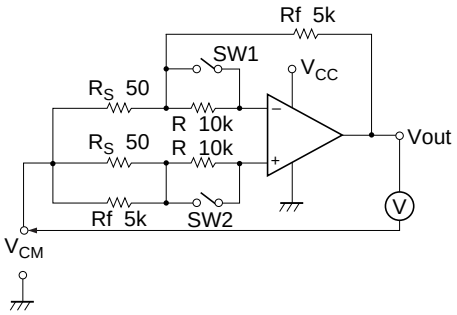
Electrical Characteristics 2

(V_{CC} = + 15V, Ta = – 40 to 125°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Input offset voltage	V_{IO}	—	—	8	mV	V_{CM} = 7.5V, R_S = 50Ω, Rf = 5kΩ
Input offset current	I_{IO}	—	—	200	nA	V_{CM} = 7.5V , I_{IO} = | I_I^- – I_I^+ |
Input bias current	I_{IB}	—	—	500	nA	V_{CM} = 7.5V
Common-mode input voltage range	V_{CM}	0	—	13.0	V	R_S = 1kΩ, Rf = 100kΩ, f = 100Hz
Output voltage	V_{OH}	13.0	—	—	V	I_{OH} = –1mA
	V_{OL}	—	—	1.3	V	I_{OL} = 1mA
Supply current	I_{CC}	—	—	4	mA	Vin = GND, R_L = ∞

Test Circuits

1. Input offset voltage (V_{IO}), input offset current (I_{IO}), and Input bias current (I_{IB}) test circuit



SW1	SW2	V_O
On	On	V_{O1}
Off	Off	V_{O2}
On	Off	V_{O3}
Off	On	V_{O4}

$$V_{CM} = \frac{1}{2} V_{CC}$$

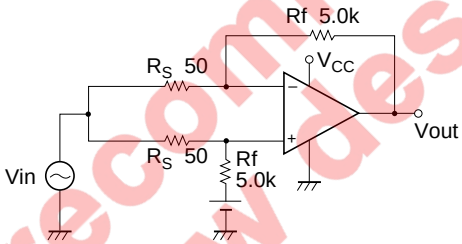
$$V_{IO} = \frac{V_{O1}}{1 + Rf / R_S} \quad (mV)$$

$$I_{IO} = \frac{V_{O2} - V_{O1}}{R(1 + Rf / R_S)} \quad (nA)$$

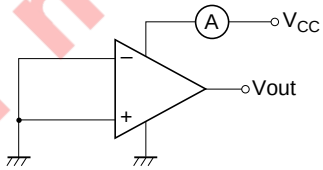
$$I_{IB} = \frac{| V_{O4} - V_{O3} |}{2 \cdot R(1 + Rf / R_S)} \quad (nA)$$

2. Common-mode rejection ratio (CMR) test circuit

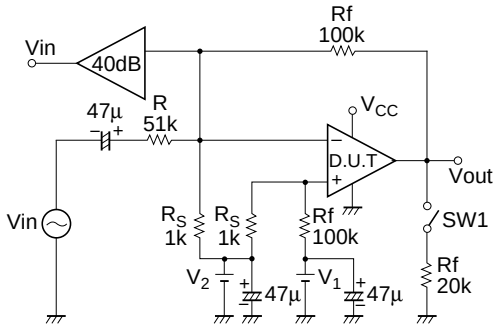
$$CMR = 20 \log \frac{V_{IN} \cdot Rf}{V_O \cdot R_S} \quad (dB)$$



3. Supply current (I_{CC}) test circuit



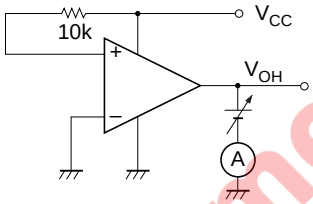
4. Voltage gain (A_{VD}), slew rate (SR), common-mode input voltage range (V_{CM}), and maximum output voltage amplitude (V_{OP-P}) test circuit.



(1) A_{VD}: R_S = 1kΩ, Rf = 100kΩ, R_L = ∞, V_1 = V_2 = 1/2 V_{CC}

$$A_{VD} = 20 \log \frac{V_O}{V_{IN}} + 40 \quad \text{(dB)}$$

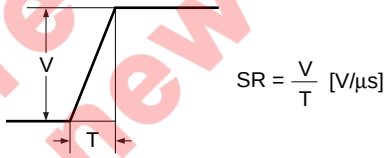
(2) SR: f = 1.5kHz, R_L = ∞, V_1 = V_2 = 1/2 V_{CC}



(3) V_{CM}: R_S = 1kΩ, Rf = 100kΩ, f = 100Hz, V_1 = 1/2 V_{CC}, R_L = ∞,
and the value of V_2 just slightly prior to the point where the output waveform changes.

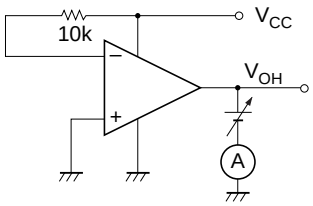
(4) V_{OP-P}:R_S = 1kΩ, Rf = 100kΩ, R_L: 20kΩ, f = 100Hz, V_{OP-P} = V_{OH} ↔ V_{OL} [V_{P-P}]

5. Output source current (Iosource) test circuit
Io source: V_{OH} = 10V



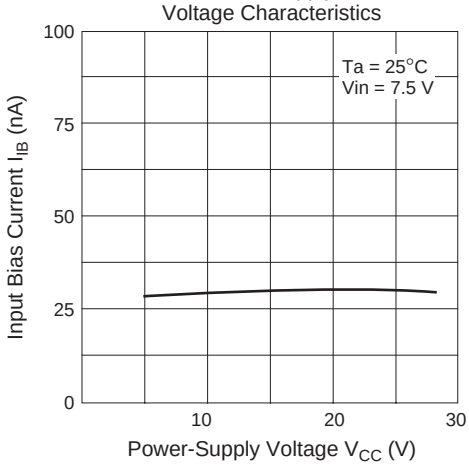
$$SR = \frac{V}{T} \text{ [V/µs]}$$

6. Output sink current (Iosink) test circuit
Io sink: V_{OL} = 1V

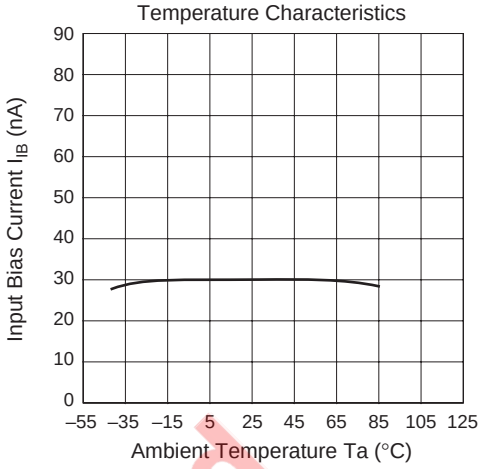


Characteristics Curve

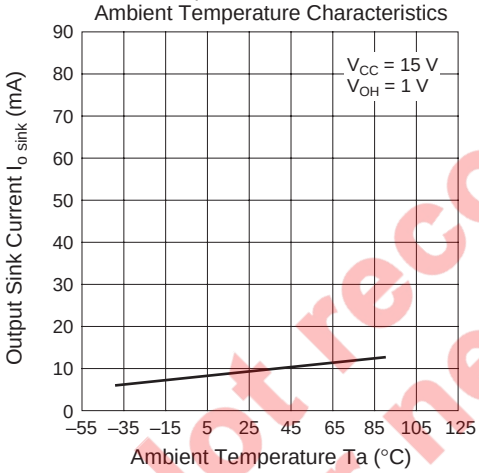
Input Bias Current vs. Power-Supply Voltage Characteristics



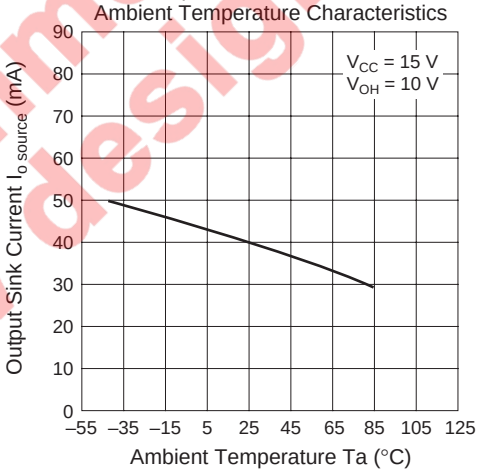
Input Bias Current vs. Ambient Temperature Characteristics



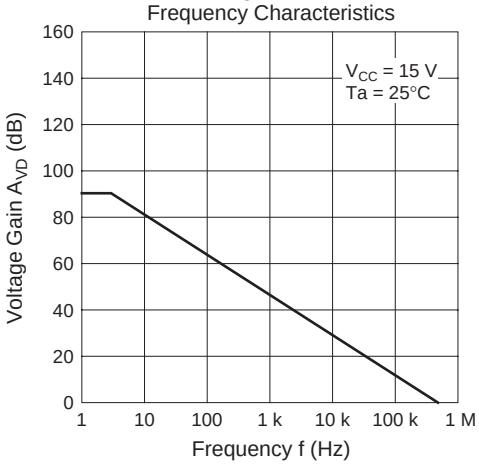
Output Sink Current vs. Ambient Temperature Characteristics



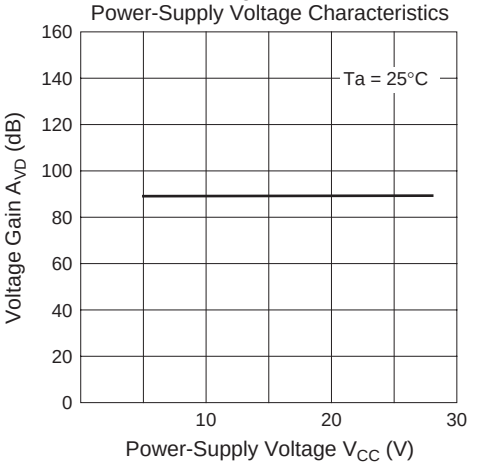
Output Source Current vs. Ambient Temperature Characteristics



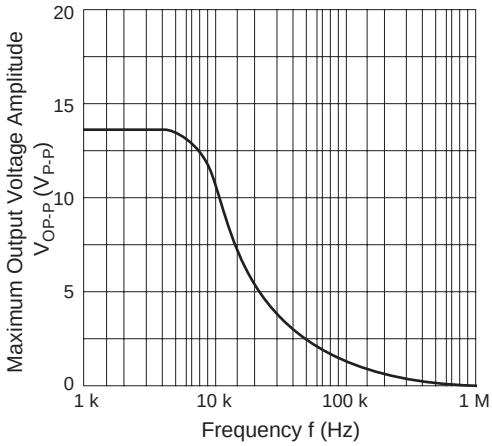
Voltage Gain vs. Frequency Characteristics



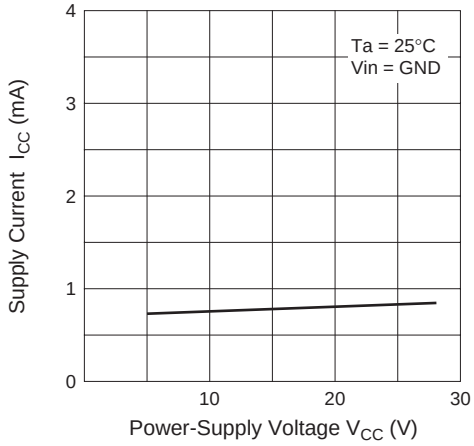
Voltage Gain vs. Power-Supply Voltage Characteristics



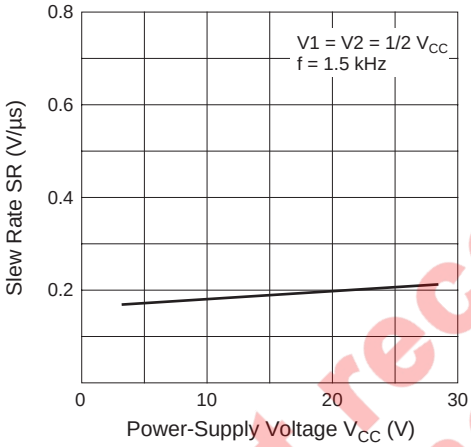
Maximum Output Voltage Amplitude vs. Frequency Characteristics



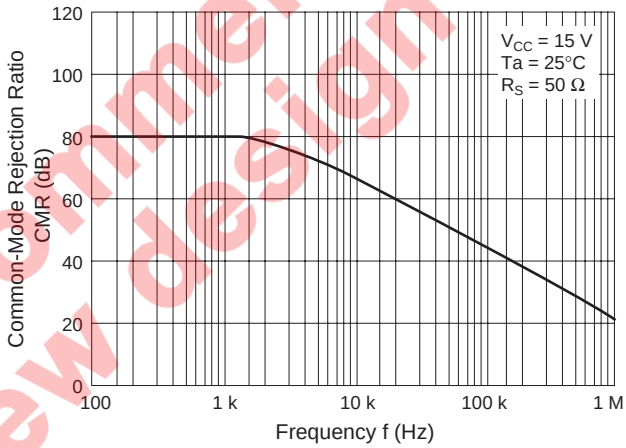
Supply Current vs. Power-Supply Voltage Characteristics



Slew Rate vs. Power-Supply Voltage Characteristics



Common-Mode Rejection Ratio vs. Frequency Characteristics



HA17902 Application Examples

The HA17902 is a quad operational amplifier, and consists of four operational amplifier circuits and one bias current circuit. It features single-voltage power supply operation, internal phase compensation, a wide zero-cross bandwidth, a low input bias current, and a high open-loop gain. Thus the HA17902 can be used in a wide range of applications. This section describes several applications using the HA17902.

1. Noninverting Amplifier

   Figure 1 shows the circuit diagram for a noninverting amplifier. The voltage gain of this amplifier is given by the following formula.

$$\frac{Vout}{Vin} = 1 + \frac{R2}{R1}$$

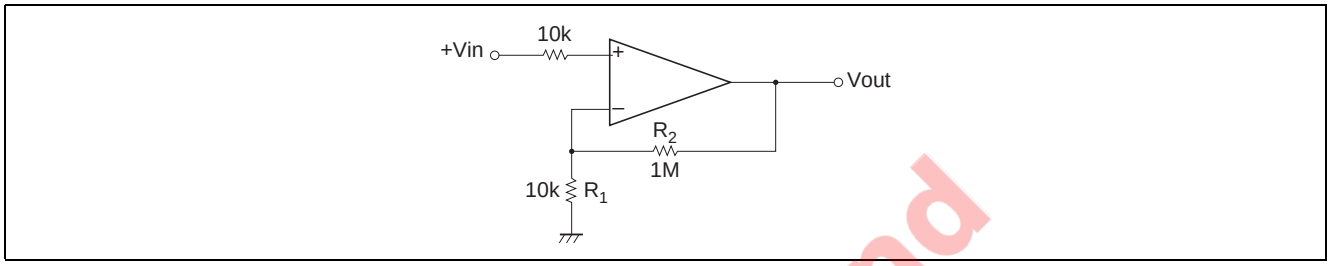


Figure 1 Noninverting Amplifier

2. Summing Amplifier

   Since the circuit shown in figure 2 applies $+V_1$ and $+V_2$ to the noninverting input and $+V_3$ and $+V_4$ to the inverting input, the total output will be $Vout = V_1 + V_2 - V_3 - V_4$.

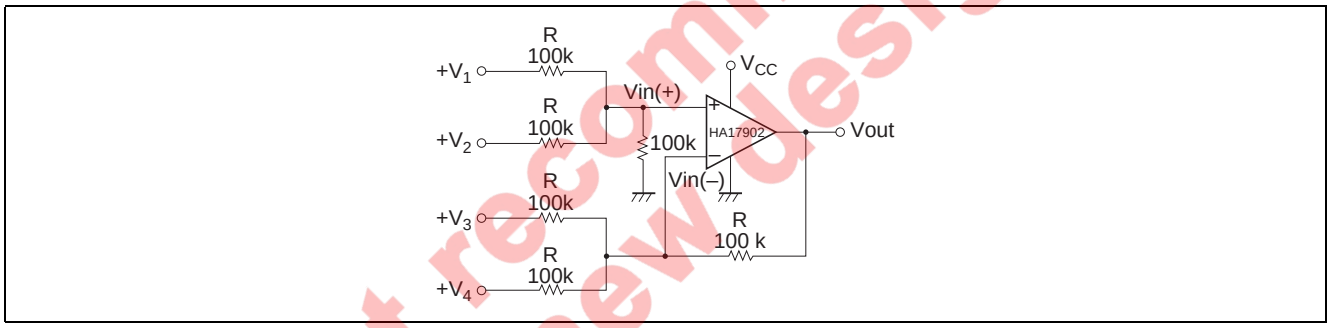


Figure 2 Summing Amplifier

3. High Input Impedance DC Differential Amplifier

The circuit shown in figure 3 is a high input impedance DC differential amplifier. This circuit's common-mode rejection ratio (CMR) depends on the matching between the R_1/R_2 and R_4/R_3 resistance ratios. This amplifier's output is given by the following formula.

$$Vout = \left(1 + \frac{R_4}{R_3}\right)(V_2 - V_1)$$

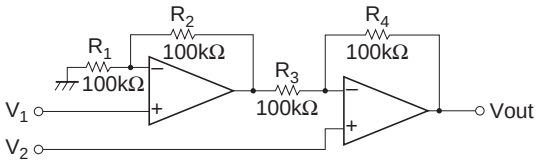


Figure 3 High Input Impedance DC Differential Amplifier

4. Voltage Controlled Oscillator

Figure 4 shows an oscillator circuit in which the amplifier A_1 is an integrator, the amplifier A_2 is a comparator, and transistor Q_1 operates as a switch that controls the oscillator frequency. If the output Vout1 is at the low level, this will cut off transistor Q1 and cause the A_1 inverting input to go to a higher potential than the noninverting input. Therefore, A_1 will integrate this negative input state and its output level will decrease. When the A_1 integrator output becomes lower than the A_2 comparator noninverting input level ($V_{CC}/2$) the comparator output goes high. This turns on transistor Q_1 causing the integrator to integrate a positive input state and for its output to increase. This operation generates a square wave on Vout1 and a triangular wave on Vout2.

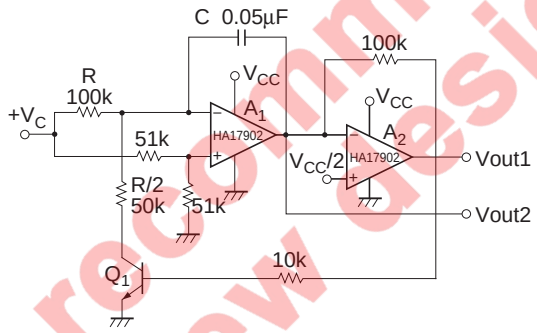
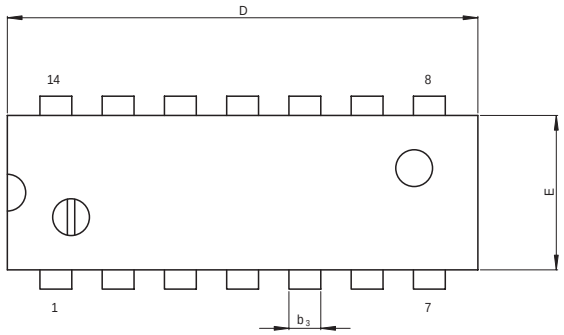
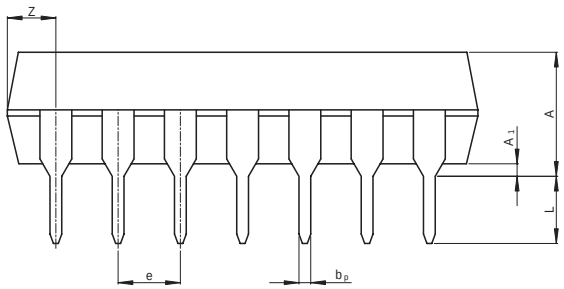


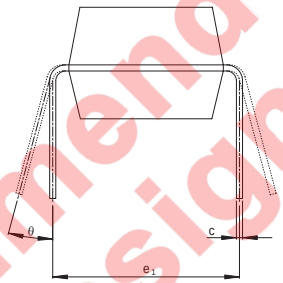
Figure 4 Voltage Controlled Oscillator

Package Dimensions

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-DIP14-6.3x19.2-2.54	PRDP0014AB-A	DP-14	0.97g

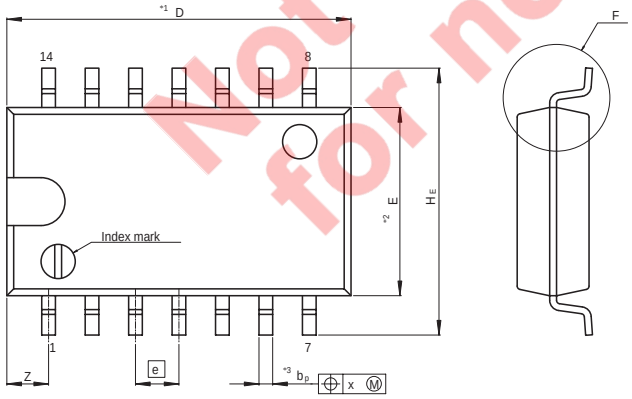


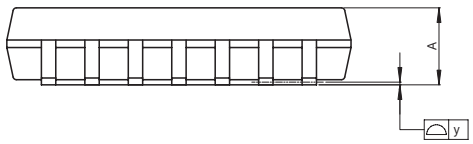




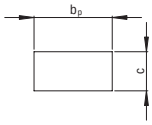
Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
e_1	—	7.62	—
D	—	19.2	20.32
E	—	6.3	7.4
A	—	—	5.06
A_1	0.51	—	—
b_p	0.38	0.48	0.58
b_3	—	1.3	—
c	0.20	0.25	0.35
θ	0°	—	15°
e	2.29	2.54	2.79
Z	—	—	2.79
L	2.54	—	—

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-SOP14-5.5x10.06-1.27	PRSP0014DF-B	FP-14DAV	0.23g

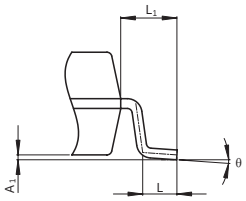




NOTE)
1. DIMENSIONS"*1 (Nom)"AND"*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION"*3"DOES NOT INCLUDE TRIM OFFSET.



Terminal cross section
(Ni/Pd/Au plating)



Detail F

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	10.06	10.5
E	—	5.50	—
A_2	—	—	—
A_1	0.00	0.10	0.20
A	—	—	2.20
b_p	0.34	0.40	0.46
b_1	—	—	—
c	0.15	0.20	0.25
c_1	—	—	—
θ	0°	—	8°
H_E	7.50	7.80	8.00
e	—	1.27	—
x	—	—	0.12
y	—	—	0.15
Z	—	—	1.42
L	0.50	0.70	0.90
L_1	—	1.15	—

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Colophon 2.0