STV270N4F3

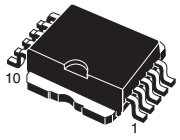
N-channel 40 V, 1.25 mΩ, 270 A, PowerSO-10 STripFET™ Power MOSFET

Features

Type	V_{DSS}	$R_{DS(on)}$ max	I_D (1)
STV270N4F3	40 V	< 1.5 mΩ	270 A

1. Current limited by package

- Conduction losses reduced
- Low profile, very low parasitic inductance



PowerSO-10

Applications

- Switching application

Description

This n-channel enhancement mode Power MOSFET is the latest refinement of STMicroelectronics' unique “single feature size“ strip-based process, which has decreased the critical alignment steps, offering remarkable manufacturing reproducibility. The outcome is a transistor with extremely high packing density for low on resistance, rugged avalanche characteristics and low gate charge.

Figure 1. Internal schematic diagram and connection diagram (top view)

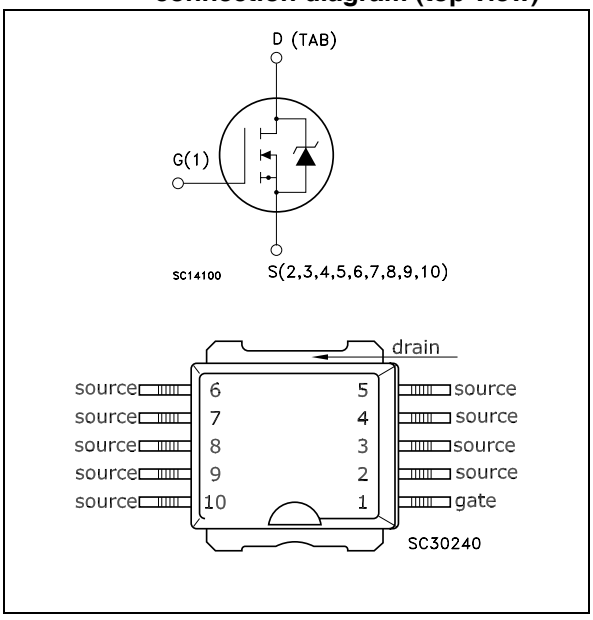


Table 1. Device summary

Order code	Marking	Package	Packaging
STV270N4F3	270N4F3	PowerSO-10	Tape and reel

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage (v_{gs} = 0)	40	V
V_{GS}	Gate-source voltage	± 20	V
I_D (1)	Drain current (continuous) at T_C = 25 °C	270	A
I_D	Drain current (continuous) at T_C = 100 °C	220	A
I_{DM} (1)	Drain current (pulsed)	1080	A
P_{TOT} (2)	Total dissipation at T_C = 25 °C	300	W
	Derating factor	2	W/°C
E_{AS} (3)	Single pulse avalanche energy	1000	mJ
T_{stg}	Storage temperature	-55 to 175	°C
T_j	Operating junction temperature		

1. Current limited by package
2. This value is rated according to Rthj-c
3. Starting Tj = 25 °C, I_D = 80 A, V_{DD} = 32 V

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case max	0.5	°C/W
$R_{thj\text{-}pcb}$ (1)	Thermal resistance junction-pcb max	50	°C/W

1. When mounted on 1 inch2 FR-4 2 oz Cu.

2 Electrical characteristics

(Tcase =25°C unless otherwise specified)

Table 4. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 250 µA, V_{GS}= 0	40			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max rating, V_{DS} = Max rating, T_c=125 °C			10 100	µA µA
I_{GSS}	Gate body leakage current (V_{DS} = 0)	V_{DS} = ± 20 V			±200	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS}= V_{GS}, I_D = 250 µA	2		4	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS}= 10 V, I_D= 80 A		1.25	1.5	mΩ

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward transconductance	V_{DS} = 10 V, I_D= 100 A		200		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} =0		7500 1900 50		pF pF pF
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD}= 20 V, I_D= 160 A, V_{GS}= 10 V *(see Figure 14)*		110 30 25	150	nC nC nC

1. Pulsed: Pulse duration = 300 µs, duty cycle 1.5%

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$t_{d(on)}$ t_r	Turn-on delay time Rise time	V_{DD} = 20 V, I_D = 80 A R_G= 4.7 Ω, V_{GS}= 10 V *(see Figure 13)*		25 180		ns ns
$t_{d(off)}$ t_f	Turn-off delay time Fall time	V_{DD} = 20 V, I_D = 80 A R_G= 4.7 Ω, V_{GS}= 10 V, *(see Figure 13)*		110 45		ns ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SD} (1)	Source-drain current Source-drain current (pulsed)				270 1080	A A
V_{SD} (2)	Forward on voltage	I_{SD} = 80 A, V_{GS} = 0			1.3	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 160 A,di/dt = 100 A/µs V_{DD} = 32 V, T_j = 150 °C *(see Figure 15)*		70 225 3.2		ns nC A

1. Pulse width limited by safe operating area
2. Pulsed: Pulse duration = 300 µs, duty cycle 1.5%

2.1 Electrical characteristics

Figure 2. Safe operating area

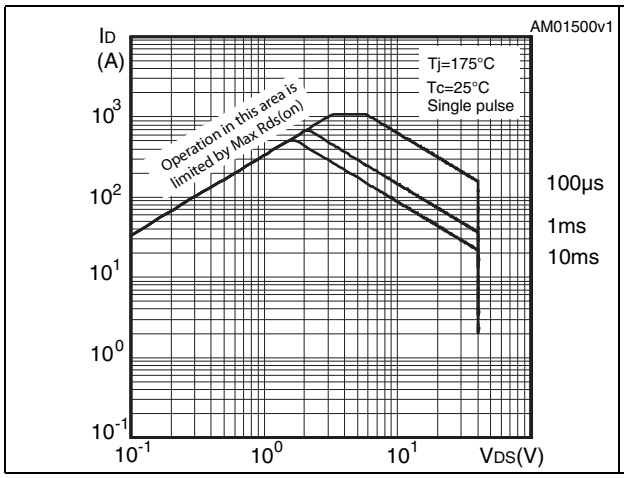


Figure 3. Thermal impedance

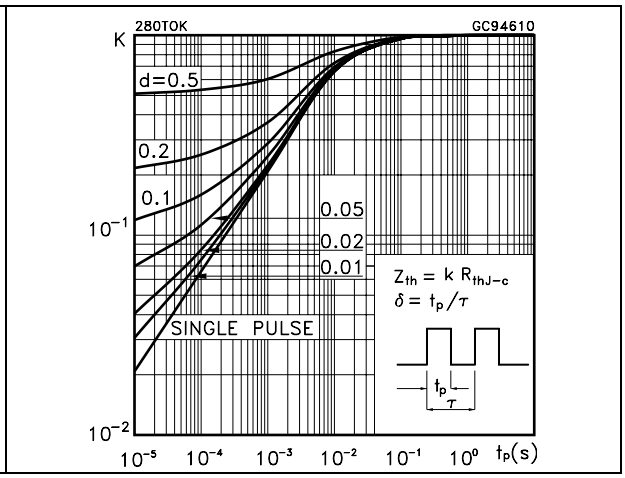


Figure 4. Output characteristics

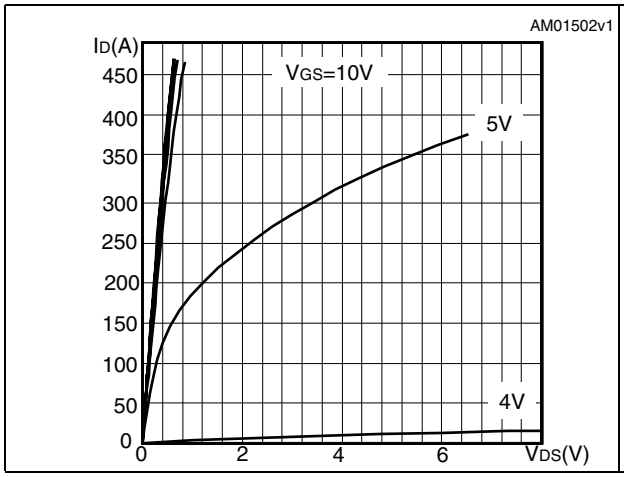


Figure 5. Transfer characteristics

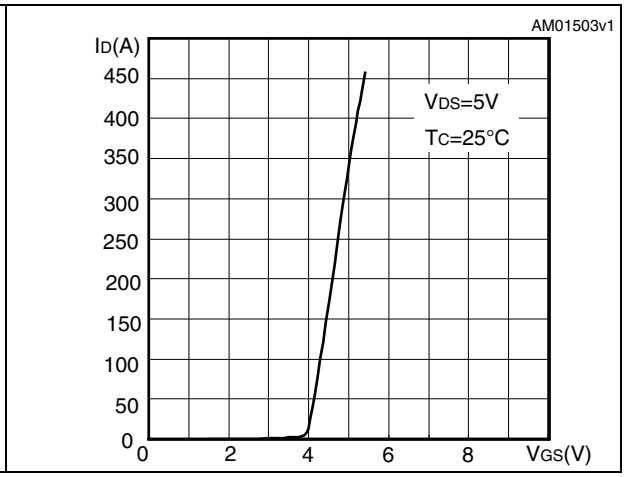


Figure 6. Static drain-source on resistance

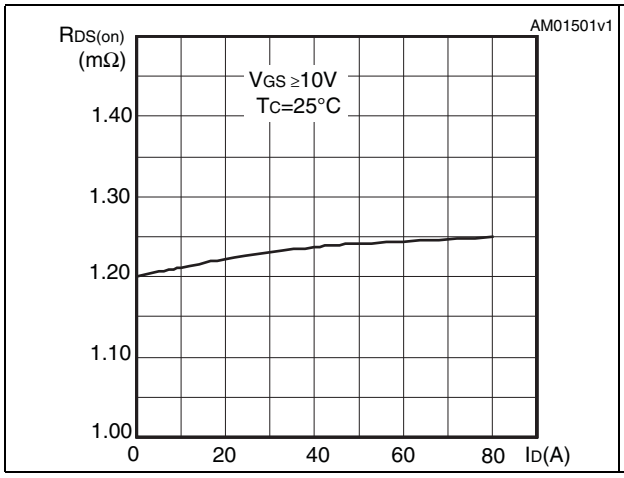


Figure 7. Normalized B_{VDSS} vs temperature

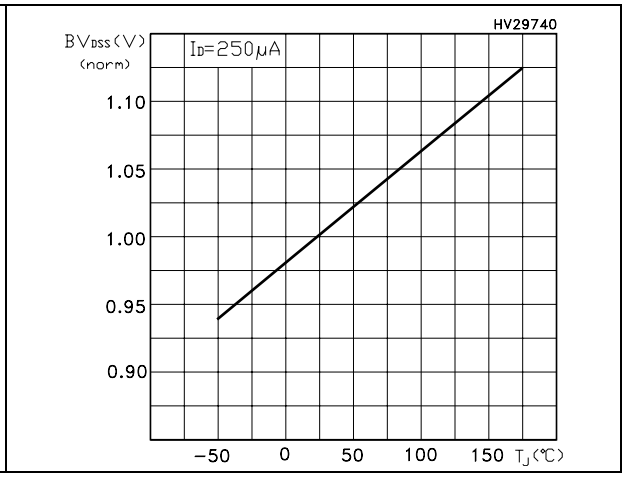


Figure 8. Gate charge vs gate-source voltage

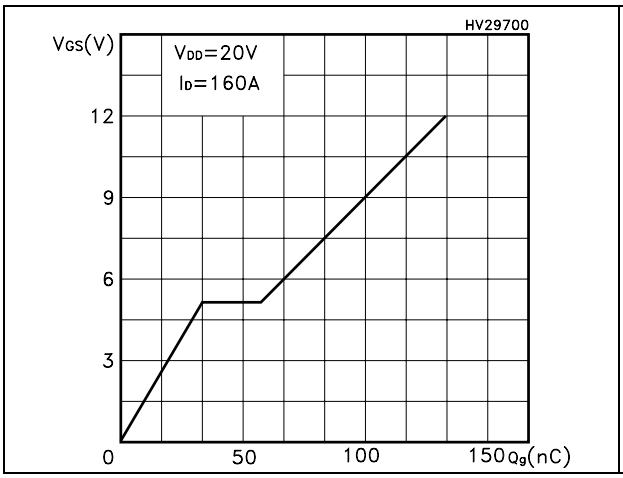


Figure 9. Capacitance variations

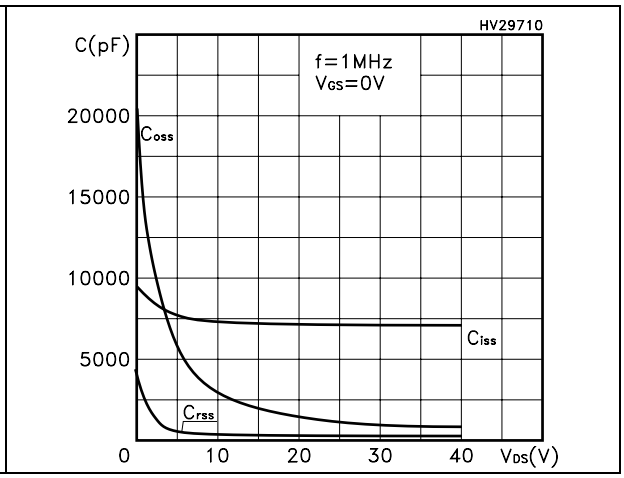


Figure 10. Normalized gate threshold voltage vs temperature

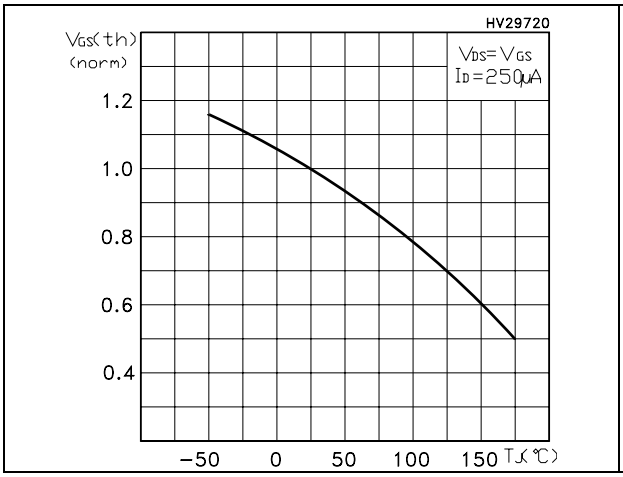


Figure 11. Normalized on resistance vs temperature

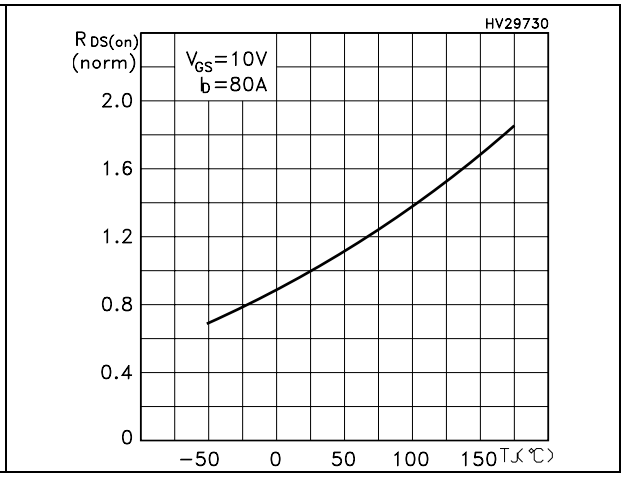
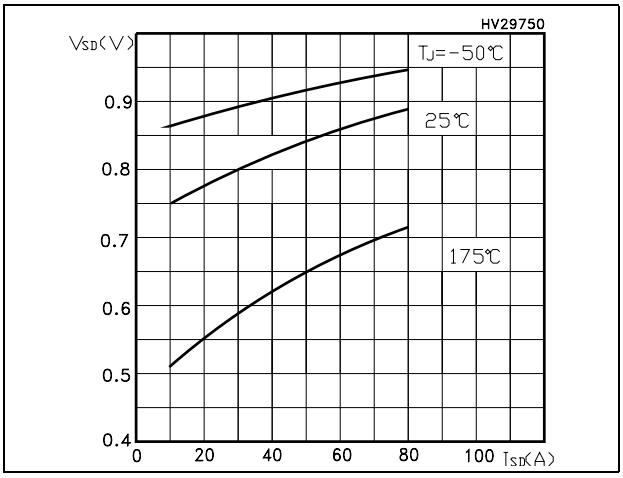


Figure 12. Source-drain diode forward characteristics



3 Test circuits

Figure 13. Switching times test circuit for resistive load

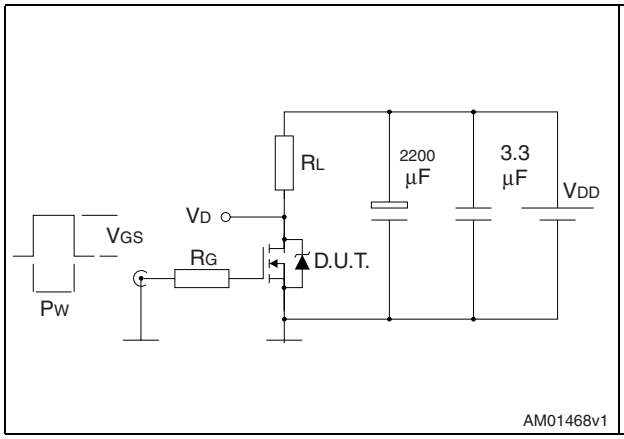


Figure 14. Gate charge test circuit

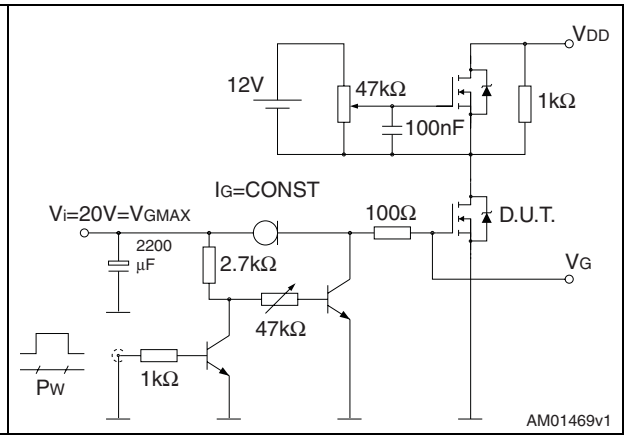


Figure 15. Test circuit for inductive load switching and diode recovery times

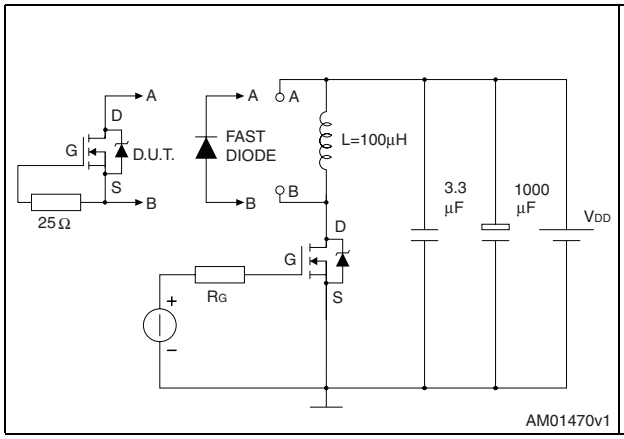


Figure 16. Unclamped inductive load test circuit

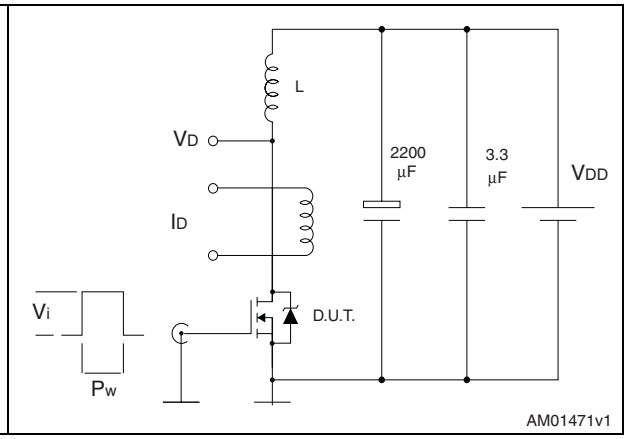


Figure 17. Unclamped inductive waveform

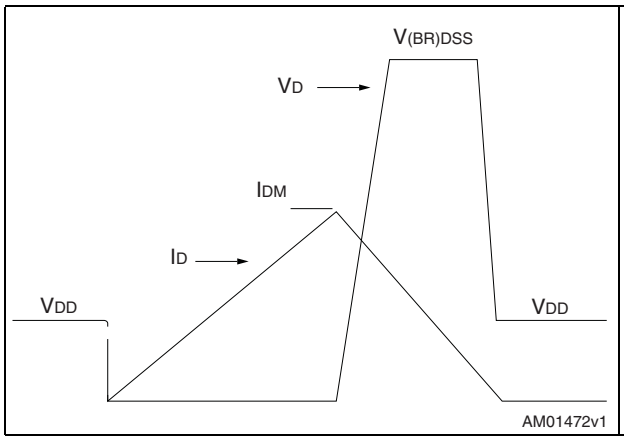
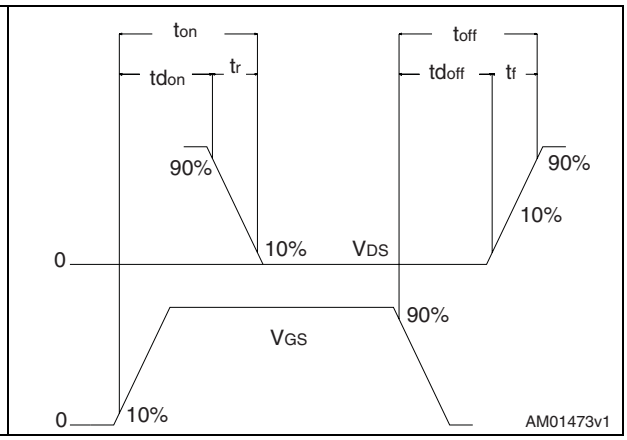


Figure 18. Switching time waveform

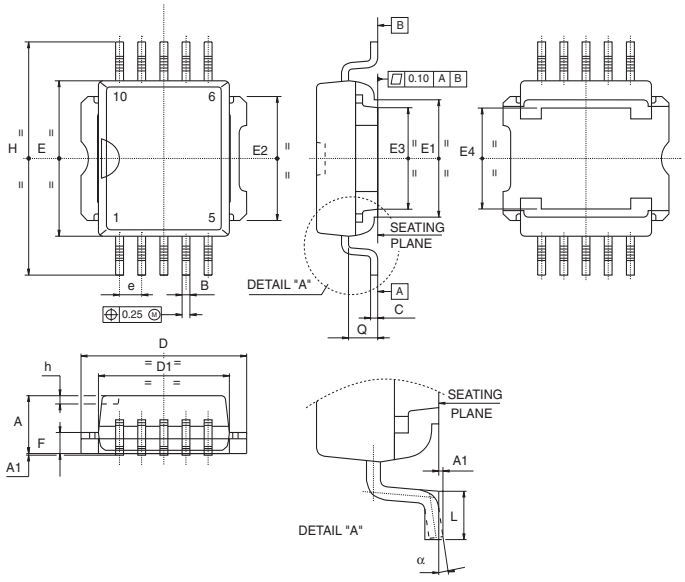


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: *www.st.com*

PowerSO-10 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	3.35		3.65	0.132		0.144
A1	0.00		0.10	0.000		0.004
B	0.40		0.60	0.016		0.024
C	0.35		0.55	0.013		0.022
D	9.40		9.60	0.370		0.378
D1	7.40		7.60	0.291		0.300
e		1.27			0.050	
E	9.30		9.50	0.366		0.374
E1	7.20		7.40	0.283		0.291
E2	7.20		7.60	0.283		0.300
E3	6.10		6.35	0.240		0.250
E4	5.90		6.10	0.232		0.240
F	1.25		1.35	0.049		0.053
h		0.50			0.002	
H	13.80		14.40	0.543		0.567
L	1.20		1.80	0.047		0.071
q		1.70			0.067	
α	0°		8°			



0068039-C

5 Revision history

Table 8. Document revision history

Date	Revision	Changes
25-Oct-2007	1	initial release
03-Apr-2008	2	I_D value has been updated.
01-Oct-2008	3	Document status promoted from preliminary data to datasheet

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