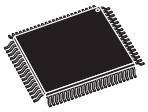
M58BW16F
M58BW32F

16 or 32 Mbit (x 32, boot block, burst) 3.3 V supply Flash memories

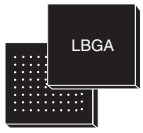
Preliminary Data

Features

- Supply voltage
  - V_{DD} = 2.7 V to 3.6 V (45 ns) or V_{DD} = 2.5 V to 3.3 V (55 ns)
  - V_{DDQ} = V_{DDQIN} = 2.4 V to 3.6 V for I/O buffers
- High performance
  - Access times: 45 and 55 ns
  - Synchronous burst reads
  - 75 MHz effective zero wait-state burst read
  - Asynchronous page reads
- M58BW32F memory organization:
  - Eight 64 Kbit small parameter blocks
  - Four 128 Kbit large parameter blocks
  - Sixty-two 512 Kbit main blocks
- M58BW16F memory organization:
  - Eight 64 Kbit parameter blocks
  - Thirty-one 512 Kbit main blocks
- Hardware block protection
  - $\overline{WP}$ pin to protect any block combination from Program and Erase operations
  - PEN signal for Program/Erase Enable
- Irreversible modify protection (OTP like) on 128 Kbits:
  - Block 1 (bottom device) or block 72 (top device) in the M58BW32F
  - Blocks 2 and 3 (bottom device) or blocks 36 and 35 (top device) in the M58BW16F
- Security
  - 64-bit unique device identifier (UID)
- Fast programming
  - Write to buffer and program capability
- Optimized for FDI drivers
  - Common Flash interface (CFI)
  - Fast Program/Erase Suspend feature in each block
- Low power consumption



PQFP80 (T)



LBGA80 (ZA)
10 x 8 ball array

  - 100 µA typical Standby current
- Electronic signature
  - Manufacturer code: 0020h
  - Top device codes:
    M58BW32FT: 8838h
    M58BW16FT: 883Ah
  - Bottom device codes:
    M58BW32FB: 8837h
    M58BW16FB: 8839h
- Automotive device grade 3:
  - Temperature: –40 to 125 °C
  - Automotive grade certified

Contents

1 Description 7

1.1 Block protection 13

2 Signal descriptions 20

2.1 Address inputs (A0-Amax) 20

2.2 Data inputs/outputs (DQ0-DQ31) 20

2.3 Chip Enable ($\overline{E}$) 20

2.4 Output Enable ($\overline{G}$) 20

2.5 Output Disable ($\overline{GD}$) 21

2.6 Write Enable ($\overline{W}$) 21

2.7 Reset/Power-down ($\overline{RP}$) 21

2.8 Program/Erase Enable (PEN) 21

2.9 Latch Enable ($\overline{L}$) 22

2.10 Burst Clock (K) 22

2.11 Burst Address Advance ($\overline{B}$) 22

2.12 Valid Data Ready (R) 22

2.13 Write Protect ($\overline{WP}$) 22

2.14 Supply voltage ($V_{DD)}$ 23

2.15 Output supply voltage (V_{DDQ}) 23

2.16 Input supply voltage (V_{DDQIN}) 23

2.17 Ground (V_{SS} and V_{SSQ}) 23

2.18 Don't use (DU) 23

2.19 Not connected (NC) 23

3 Bus operations 24

3.1 Asynchronous Bus operations 24

3.1.1 Asynchronous Bus Read 24

3.1.2 Asynchronous Latch Controlled Bus Read 24

3.1.3 Asynchronous Page Read 25

3.1.4 Asynchronous Bus Write 25

3.1.5 Asynchronous Latch Controlled Bus Write 25

3.1.6 Output Disable 25

3.1.7 Standby . . . 26
3.1.8 Reset/Power-down . . . 26
3.2 Synchronous Bus operations . . . 27
3.2.1 Synchronous Burst Read . . . 27
3.2.2 Synchronous Burst Read Suspend . . . 28
3.3 Burst Configuration Register . . . 28
3.3.1 Read Select bit (M15) . . . 28
3.3.2 Standby Disable bit (M14) . . . 28
3.3.3 X-Latency bits (M13-M11) . . . 29
3.3.4 Y-Latency bit (M9) . . . 29
3.3.5 Valid Data Ready bit (M8) . . . 29
3.3.6 Wrap Burst bit (M3) . . . 29
3.3.7 Burst Length bit (M2-M0) . . . 29

4 Command interface . . . 33
4.1 Read Memory Array command . . . 33
4.2 Read Electronic Signature command . . . 33
4.3 Read Query command . . . 33
4.4 Read Status Register command . . . 34
4.5 Clear Status Register command . . . 34
4.6 Block Erase command . . . 34
4.7 Erase All Main Blocks command . . . 35
4.8 Program command . . . 35
4.9 Write to Buffer and Program command . . . 36
4.10 Program/Erase Suspend command . . . 37
4.11 Program/Erase Resume command . . . 37
4.12 Set Burst Configuration Register command . . . 38
4.13 Set Block Protection Configuration Register command . . . 38
4.14 Clear Block Protection Configuration Register command . . . 38

5 Status Register . . . 41
5.1 Program/Erase Controller Status (bit 7) . . . 41
5.2 Erase Suspend Status (bit 6) . . . 41
5.3 Erase Status (bit 5) . . . 42
5.4 Program/Write to Buffer and Program Status (bit 4) . . . 42

5.5 PEN Status (bit 3) 42
5.6 Program Suspend Status (bit 2) 43
5.7 Block Protection Status (bit 1) 43
5.8 Bit 0 43

6 Maximum rating 45

7 DC and AC parameters 46

8 Package mechanical 64

9 Ordering information 67

Appendix A Flowcharts 68

Appendix B Common Flash interface (CFI) 78

Appendix C Block protection. 85

10 Revision history 86

List of tables

Table 1. Signal names . . . 10
Table 2. M58BW32F top boot block addresses . . . 14
Table 3. M58BW32F bottom boot block addresses . . . 16
Table 4. M58BW16F top boot block addresses . . . 18
Table 5. M58BW16F bottom boot block addresses . . . 19
Table 6. Asynchronous Bus operations . . . 26
Table 7. Synchronous Burst Read Bus operations . . . 28
Table 8. Burst Configuration Register . . . 30
Table 9. Burst type definition . . . 32
Table 10. Commands . . . 39
Table 11. Read electronic signature . . . 40
Table 12. Program, Erase times and endurance cycles . . . 40
Table 13. Status Register bits . . . 44
Table 14. Absolute maximum ratings . . . 45
Table 15. Data retention . . . 45
Table 16. Operating and AC measurement conditions . . . 46
Table 17. Device capacitance . . . 47
Table 18. DC characteristics . . . 47
Table 19. Asynchronous Bus Read AC characteristics . . . 50
Table 20. Asynchronous Page Read AC characteristics . . . 51
Table 21. Asynchronous Write and Latch controlled Write AC characteristics . . . 54
Table 22. Synchronous Burst Read AC characteristics . . . 60
Table 23. Power supply AC and DC characteristics . . . 61
Table 24. Reset, Power-down and Power-up AC characteristics . . . 63
Table 25. LBGA80 10 × 12 mm - 8 × 10 active ball array, 1 mm pitch, package mechanical data . . . 65
Table 26. PQFP80 - 80 lead plastic quad flat pack, package mechanical data . . . 66
Table 27. Ordering information scheme . . . 67
Table 28. Query structure overview . . . 78
Table 29. CFI - Query address and data output . . . 79
Table 30. CFI - device voltage and timing specification . . . 79
Table 31. M58BW16F device geometry definition . . . 80
Table 32. M58BW16F extended query information . . . 81
Table 33. M58BW32F device geometry definition . . . 82
Table 34. M58BW32F extended query information . . . 83
Table 35. Protection register information . . . 84
Table 36. Document revision history . . . 86

List of figures

Figure 1. Logic diagram . . . 9
Figure 2. LBGA connections (top view through package) . . . 11
Figure 3. PQFP connections (top view through package) . . . 12
Figure 4. Example burst configuration X-1-1-1 . . . 32
Figure 5. AC measurement input/output waveform . . . 46
Figure 6. AC measurement load circuit . . . 46
Figure 7. Asynchronous Bus Read AC waveforms . . . 48
Figure 8. Asynchronous Latch Controlled Bus Read AC waveforms . . . 48
Figure 9. Asynchronous Chip Enable Controlled Bus Read AC waveforms . . . 49
Figure 10. Asynchronous Address Controlled Bus Read AC waveforms . . . 49
Figure 11. Asynchronous Page Read AC waveforms . . . 51
Figure 12. Asynchronous Write AC waveforms . . . 52
Figure 13. Asynchronous Latch controlled Write AC waveforms . . . 53
Figure 14. Synchronous Burst Read, Latch Enable controlled (data valid from 'n' clock rising edge) . 55
Figure 15. Synchronous Burst Read, Chip Enable controlled (data valid from 'n' clock rising edge) . 56
Figure 16. Synchronous Burst Read, Valid Address transition controlled (data valid from 'n' clock rising edge) . . . 57
Figure 17. Synchronous Burst Read (data valid from 'n' clock rising edge) . . . 58
Figure 18. Synchronous Burst Read - valid data ready output . . . 58
Figure 19. Synchronous Burst Read - Burst Address Advance . . . 59
Figure 20. Clock input AC waveform . . . 59
Figure 21. Power supply slope specification . . . 61
Figure 22. Reset, Power-down and Power-up AC waveforms - Control pins Low . . . 62
Figure 23. Reset, Power-down and Power-up AC waveforms - Control pins toggling . . . 62
Figure 24. LBGA80 10 × 12 mm - 8 × 10 ball array, 1 mm pitch, bottom view package outline . . . 64
Figure 25. PQFP80 - 80 lead plastic quad flat pack, package outline . . . 66
Figure 26. Program flowchart and pseudocode . . . 68
Figure 27. Program Suspend & Resume flowchart and pseudocode . . . 69
Figure 28. Block Erase flowchart and pseudocode . . . 70
Figure 29. Erase Suspend & Resume flowchart and pseudocode . . . 71
Figure 30. Power-up sequence followed by Synchronous Burst Read . . . 72
Figure 31. Command interface and Program/Erase controller flowchart (a) . . . 73
Figure 32. Command interface and Program/Erase controller flowchart (b) . . . 74
Figure 33. Command interface and Program/Erase controller flowchart (c) . . . 75
Figure 34. Command interface and Program/Erase controller flowchart (d) . . . 76
Figure 35. Command interface and Program/Erase controller flowchart (e) . . . 77

1 Description

The M58BW16F and M58BW32F are 16 and 32 Mbit non-volatile Flash memories, respectively. They can be erased electrically at block level and programmed in-system on a double-word basis using a 2.7 V to 3.6 V or 2.5 V to 3.3 V V_{DD} supply for the circuit and a 2.4 V to 3.6 V V_{DDQ} supply voltage for the input and output buffers.

In the rest of the document the M58BW16F and M58BW32F will be referred to as M58BWxxF unless otherwise specified.

The devices support Asynchronous (Latch Controlled and Page Read) and Synchronous Bus operations. The Synchronous Burst Read interface allows a high data transfer rate controlled by the Burst Clock signal, K. It is capable of bursting fixed or unlimited lengths of data. The burst type, latency and length are configurable and can be easily adapted to a large variety of system clock frequencies and microprocessors. All write operations are asynchronous. On power-up the memory defaults to Read mode with an Asynchronous Bus.

The device features an asymmetrical block architecture:

- The M58BW32F has an array of 62 main blocks of 512 Kbits each, plus 4 large parameter blocks of 128 Kbits each and 8 small parameter blocks of 64 Kbits each. The large and small parameter blocks are located either at the top (M58BW32FT) or at the bottom (M58BW32FB) of the address space. The first large parameter block is referred to as boot block and can be used either to store a boot code or parameters. The memory array organization is detailed in *Table 2: M58BW32F top boot block addresses* and *Table 3: M58BW32F bottom boot block addresses*.
- The M58BW16F has an array of 8 parameter blocks of 64 Kbits each and 31 main blocks of 512 Kbits each. In the M58BW16FT the parameter blocks are located at the top of the address space whereas in the M58BW16FB, they are located at the bottom. The memory array organization is detailed in *Table 4: M58BW16F top boot block addresses* and *Table 5: M58BW16F bottom boot block addresses*.

Program and Erase commands are written to the command interface of the memory. An on-chip Program/Erase controller simplifies the process of programming or erasing the memory by taking care of all of the special operations that are required to update the memory contents. The end of a Program or Erase operation can be detected and any error conditions identified in the Status Register. The command set required to control the memory is consistent with JEDEC standards.

Erase can be suspended in order to perform either Read or Program in any other block, and then resumed. Program can be suspended to Read data in any other block, and then resumed. Each block can be programmed and erased over 100,000 cycles.

All blocks are protected during power-up. The M58BWxxF features five different levels of hardware and software block protection to avoid unwanted Program/Erase operations:

- Write/Protect Enable input, $\overline{WP}$, hardware protects a combination of blocks from Program and Erase operations. The blocks to be protected are configured individually by issuing a Set Block Protection Configuration Register or a Clear Block Protection Configuration Register command.
- All Program or Erase operations are blocked when Reset, $\overline{RP}$, is held Low.
- A Program/Erase Enable input, PEN, is used to protect all blocks, preventing Program and Erase operations from affecting their data.
- A permanent user-enabled protection against Modify operations is available:
  - on one specific 128-Kbit parameter block in the M58BW32F – block 1 for bottom devices or block 72 for top devices
  - on two specific 64-Kbit parameter blocks in the M58BW16F – blocks 2 and 3 for bottom devices or blocks 36 and 35 for top devices.

A Reset/Power-down mode is entered when the $\overline{RP}$ input is Low. In this mode the power consumption is reduced to the standby level, the device is write protected and both the Status and Burst Configuration Registers are cleared. A recovery time is required when the $\overline{RP}$ input goes High.

A manufacturer code and a device code are available. They can be read from the memory allowing programming equipment or applications to automatically match their interface to the characteristics of the memory.

Finally, the M58BWxxF features a 64-bit unique device identifier (UID) which is programmed by Numonyx on the production line. It is unique for each die and can be used to implement cryptographic algorithms to improve security. Information is available in the CFI area (see *Table 32: M58BW16F extended query information*).

The memory is offered in PQFP80 (14 x 20 mm) and LBGA80 (1.0 mm pitch) packages and it is supplied with all the bits erased (set to '1').

Figure 1. Logic diagram

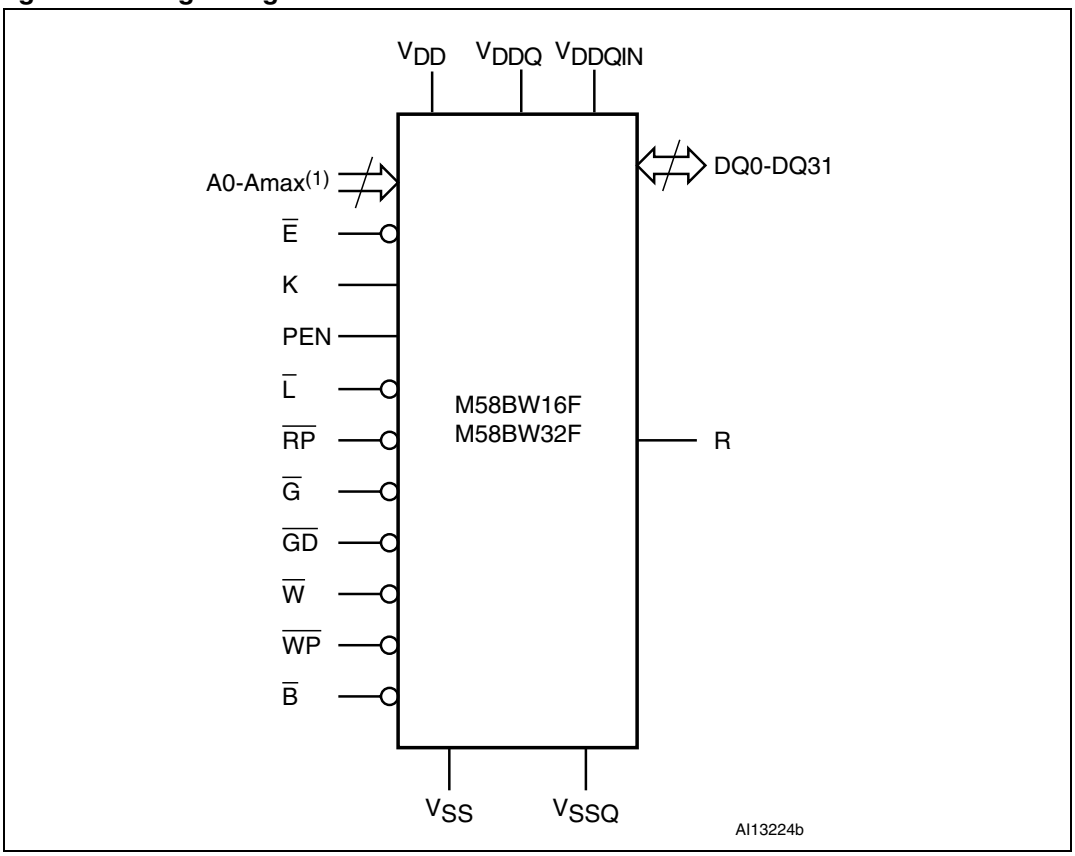
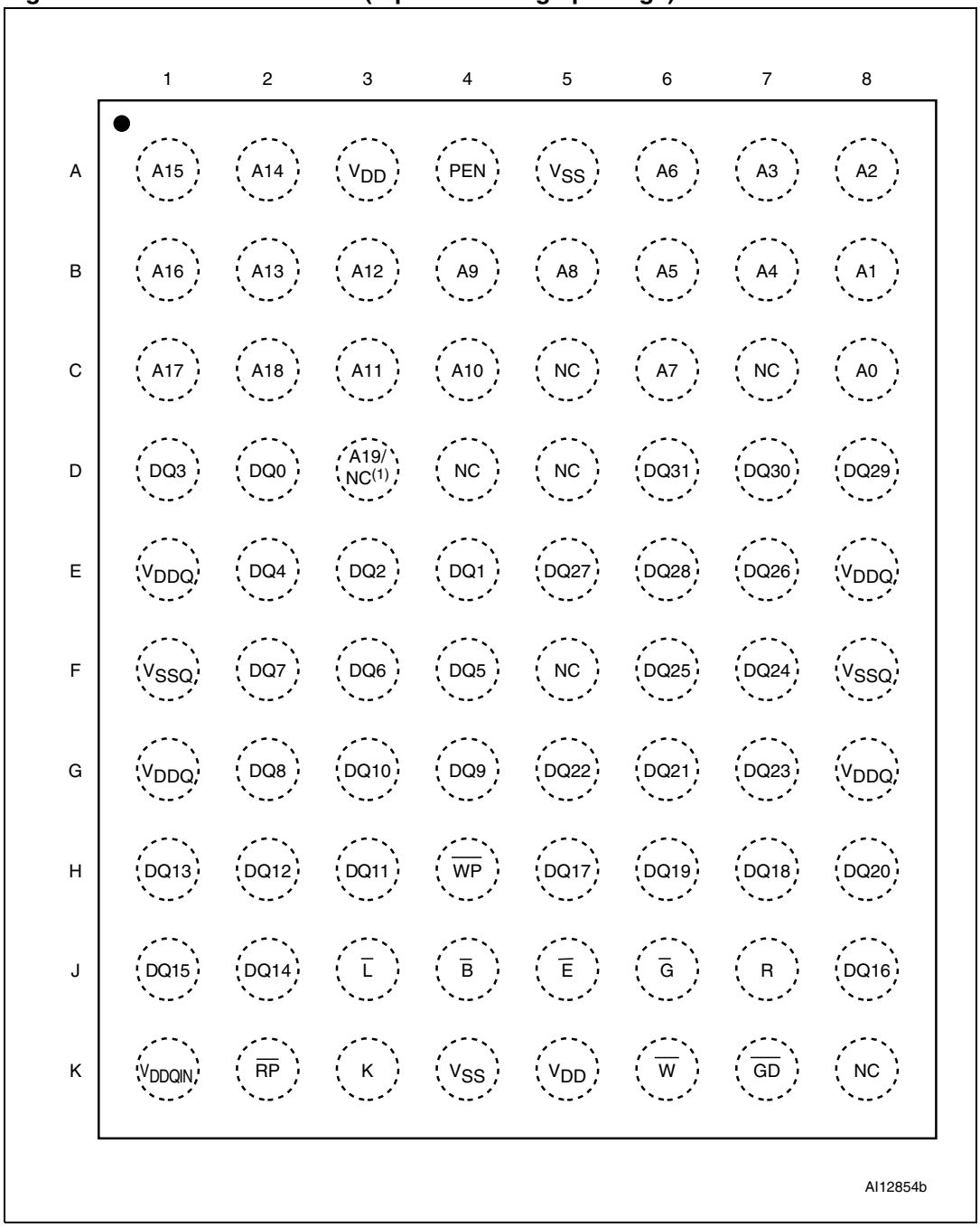


Table 1. Signal names

Signal name	Function	Direction
A0-Amax(1)	Address inputs	Inputs
DQ0-DQ7	Data input/output, command input	I/O
DQ8-DQ15	Data input/output, Burst Configuration Register	I/O
DQ16-DQ31	Data input/output	I/O
$\overline{B}$	Burst Address Advance input	Input
$\overline{E}$	Chip Enable input	Input
$\overline{G}$	Output Enable input	Input
K	Burst Clock input	Input
$\overline{L}$	Latch Enable input	Input
R	Valid Data Ready output	Output
$\overline{RP}$	Reset/Power-down input	Input
$\overline{W}$	Write Enable input	Input
$\overline{GD}$	Output Disable input	Input
$\overline{WP}$	Write Protect input	Input
V_{DD}	Supply voltage	
V_{DDQ}	Power supply for output buffers	
V_{DDQIN}	Power supply for input buffers only	
PEN	Program/Erase Enable	Input
V_{SS}	Ground	
V_{SSQ}	Input/output ground	
NC	Not connected internally	
DU	Don't use as internally connected	

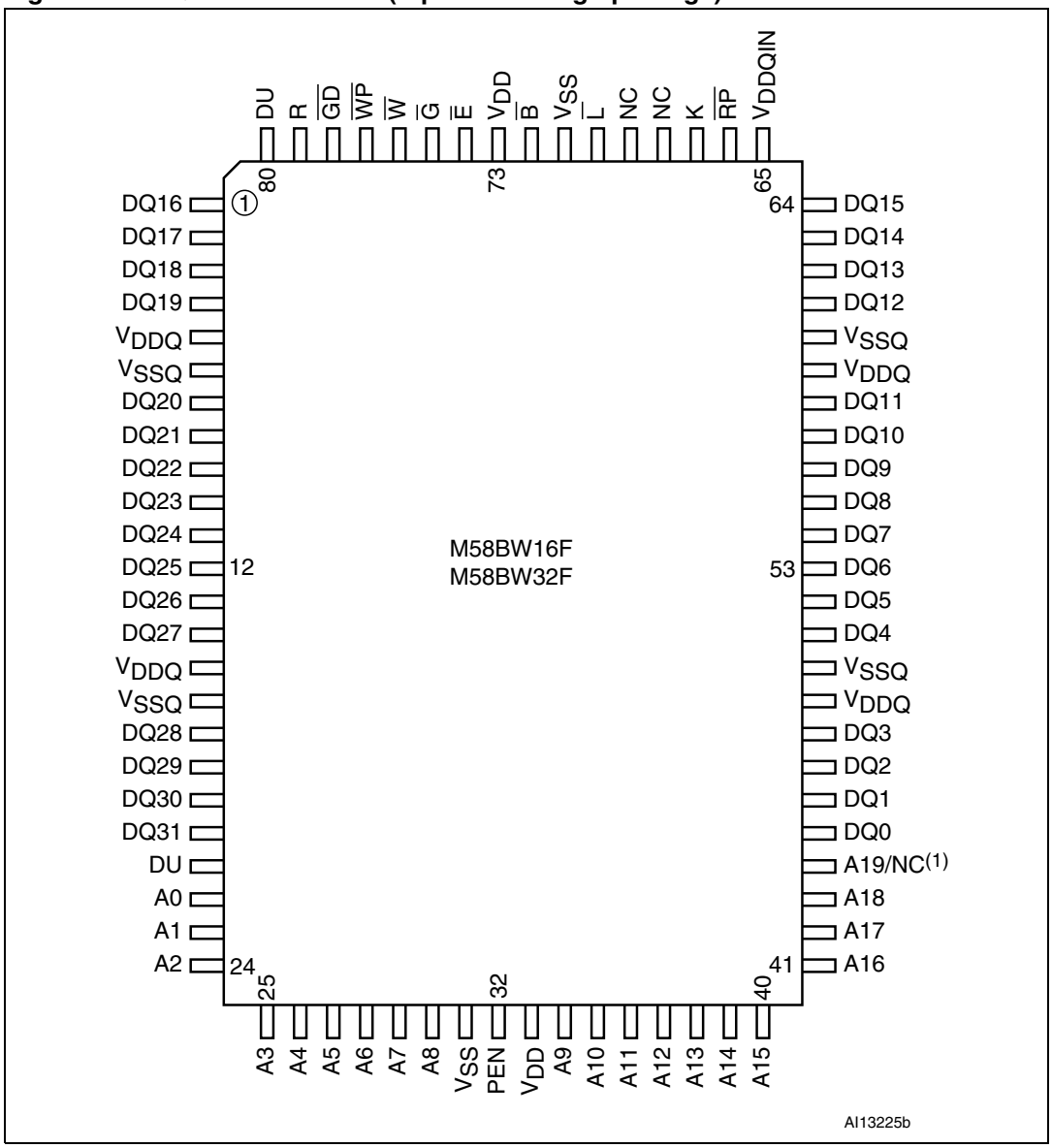
1. Amax is equal to A18 in the M58BW16F, and to A19 in the M58BW32F.

Figure 2. LBGA connections (top view through package)



1. Ball D3 is NC in the M58BW16F and A19 in the M58BW32F.

Figure 3. PQFP connections (top view through package)



1.1 Block protection

The M58BWxxF features four different levels of block protection.

- **Write Protect pin, $\overline{WP}$, -** When $\overline{WP}$ is Low, V_{IL}, the protection status that has been configured in the Block Protection Configuration Register is activated. The Block Protection Configuration Register is volatile. Any combination of blocks is possible. Any attempt to program or erase a protected block will return an error in the Status Register (see *Table 13: Status Register bits*).
- **Reset/Power-down pin, $\overline{RP}$, -** If the device is held in reset mode ($\overline{RP}$ at V_{IL}), no Program or Erase operation can be performed on any block.
- **Program/Erase Enable, PEN, -** The Program/Erase Enable input, PEN, protects all blocks by preventing Program and Erase operations from modifying the data.
  Prior to issuing a Program or Erase command, the Program/Erase Enable must be set to High (V_{IH}). If it is Low (V_{IL}), the Program or Erase operation is not accepted and an error is generated in the Status Register.
- **Permanent protection against modify operations -** specific OTP-like blocks can be permanently protected against modify operations (Program/Erase):
  - in the M58BW32F, a unique 128-Kbit parameter block – block 1 (01000h-01FFFh) for bottom devices or block 72 (FE000h-FEFFFh) for top devices
  - in the M58BW16F, two 64-Kbit parameter blocks – blocks 2 and 3 (01000h-01FFFh) for bottom devices or blocks 36 and 35 (7E000h-7EFFFh) for top devices

  This protection is user-enabled. Details of how this protection is activated are provided in a dedicated application note.

After a device reset the first two kinds of block protection ($\overline{WP}$, $\overline{RP}$) can be combined to give a flexible block protection. All blocks are protected at power-up.

Table 2. M58BW32F top boot block addresses

#	Size (Kbit)	Address range[1]
73	128	FF000h-FFFFFh
72	128	FE000h-FEFFFh[2]
71	128	FD000h-FDFFFh
70	128	FC000h-FCFFFh
69	64	FB800h-FBFFFh
68	64	FB000h-FB7FFh
67	64	FA800h-FAFFFh
66	64	FA000h-FA7FFh
65	64	F9800h-F9FFFh
64	64	F9000h-F97FFh
63	64	F8800h-F8FFFh
62	64	F8000h-F87FFh
61	512	F4000h-F7FFFh
60	512	F0000h-F3FFFh
59	512	EC000h-EFFFFh
58	512	E8000h-EBFFFh
57	512	E4000h-E7FFFh
56	512	E0000h-E3FFFh
55	512	DC000h-DFFFFh
54	512	D8000h-DBFFFh
53	512	D4000h-D7FFFh
52	512	D0000h-D3FFFh
51	512	CC000h-CFFFFh
50	512	C8000h-CBFFFh
49	512	C4000h-C7FFFh
48	512	C0000h-C3FFFh
47	512	BC000h-BFFFFh
46	512	B8000h-BBFFFh
45	512	B4000h-B7FFFh
44	512	B0000h-B3FFFh
43	512	AC000h-AFFFFh
42	512	A8000h-ABFFFh
41	512	A4000h-A7FFFh
40	512	A0000h-A3FFFh
39	512	9C000h-9FFFFh
38	512	98000h-9BFFFh
37	512	94000h-97FFFh
36	512	90000h-93FFFh

Table 2. M58BW32F top boot block addresses (continued)

#	Size (Kbit)	Address range(1)
35	512	8C000h-8FFFFh
34	512	88000h-8BFFFh
33	512	84000h-87FFFh
32	512	80000h-83FFFh
31	512	7C000h-7FFFFh
30	512	78000h-7BFFFh
29	512	74000h-77FFFh
28	512	70000h-73FFFh
27	512	6C000h-6FFFFh
26	512	68000h-6BFFFh
25	512	64000h-67FFFh
24	512	60000h-63FFFh
23	512	5C000h-5FFFFh
22	512	58000h-5BFFFh
21	512	54000h-57FFFh
20	512	50000h-53FFFh
19	512	4C000h-4FFFFh
18	512	48000h-4BFFFh
17	512	44000h-47FFFh
16	512	40000h-43FFFh
15	512	3C000h-3FFFFh
14	512	38000h-3BFFFh
13	512	34000h-37FFFh
12	512	30000h-33FFFh
11	512	2C000h-2FFFFh
10	512	28000h-2BFFFh
9	512	24000h-27FFFh
8	512	20000h-23FFFh
7	512	1C000h-1FFFFh
6	512	18000h-1BFFFh
5	512	14000h-17FFFh
4	512	10000h-13FFFh
3	512	0C000h-0FFFFh
2	512	08000h-0BFFFh
1	512	04000h-07FFFh
0	512	00000h-03FFFh

1. Addresses are indicated in 32-bit addressing.
2. OTP block.

Table 3. M58BW32F bottom boot block addresses

#	Size (Kbit)	Address range(1)
73	512	FC000h-FFFFFh
72	512	F8000h-FBFFFh
71	512	F4000h-F7FFFh
70	512	F0000h-F3FFFh
69	512	EC000h-EFFFFh
68	512	E8000h-EBFFFh
67	512	E4000h-E7FFFh
66	512	E0000h-E3FFFh
65	512	DC000h-DFFFFh
64	512	D8000h-DBFFFh
63	512	D4000h-D7FFFh
62	512	D0000h-D3FFFh
61	512	CC000h-CFFFFh
60	512	C8000h-CBFFFh
59	512	C4000h-C7FFFh
58	512	C0000h-C3FFFh
57	512	BC000h-BFFFFh
56	512	B8000h-BBFFFh
55	512	B4000h-B7FFFh
54	512	B0000h-B3FFFh
53	512	AC000h-AFFFFh
52	512	A8000h-ABFFFh
51	512	A4000h-A7FFFh
50	512	A0000h-A3FFFh
49	512	9C000h-9FFFFh
48	512	98000h-9BFFFh
47	512	94000h-97FFFh
46	512	90000h-93FFFh
45	512	8C000h-8FFFFh
44	512	88000h-8BFFFh
43	512	84000h-87FFFh
42	512	80000h-83FFFh
41	512	7C000h-7FFFFh
40	512	78000h-7BFFFh
39	512	74000h-77FFFh
38	512	70000h-73FFFh
37	512	6C000h-6FFFFh
36	512	68000h-6BFFFh

Table 3. M58BW32F bottom boot block addresses (continued)

#	Size (Kbit)	Address range[1]
35	512	64000h-67FFFh
34	512	60000h-63FFFh
33	512	5C000h-5FFFFh
32	512	58000h-5BFFFh
31	512	54000h-57FFFh
30	512	50000h-53FFFh
29	512	4C000h-4FFFFh
28	512	48000h-4BFFFh
27	512	44000h-47FFFh
26	512	40000h-43FFFh
25	512	3C000h-3FFFFh
24	512	38000h-3BFFFh
23	512	34000h-37FFFh
22	512	30000h-33FFFh
21	512	2C000h-2FFFFh
20	512	28000h-2BFFFh
19	512	24000h-27FFFh
18	512	20000h-23FFFh
17	512	1C000h-1FFFFh
16	512	18000h-1BFFFh
15	512	14000h-17FFFh
14	512	10000h-13FFFh
13	512	0C000h-0FFFFh
12	512	08000h-0BFFFh
11	64	07800h-07FFFh
10	64	07000h-077FFh
9	64	06800h-06FFFh
8	64	06000h-067FFh
7	64	05800h-05FFFh
6	64	05000h-057FFh
5	64	04800h-04FFFh
4	64	04000h-047FFh
3	128	03000h-03FFFh
2	128	02000h-02FFFh
1	128	01000h-01FFFh[2]
0	128	00000h-00FFFh

1. Addresses are indicated in 32-bit word addressing.
2. OTP block.

Table 4. M58BW16F top boot block addresses

#	Size (Kbit)	Address range
38	64	7F800h-7FFFFh
37	64	7F000h-7F7FFh
36(1)	64	7E800h-7EFFFh
35(1)	64	7E000h-7E7FFh
34	64	7D800h-7DFFFh
33	64	7D000h-7D7FFh
32	64	7C800h-7CFFFh
31	64	7C000h-7C7FFh
30	512	78000h-7BFFFh
29	512	74000h-77FFFh
28	512	70000h-73FFFh
27	512	6C000h-6FFFFh
26	512	68000h-6BFFFh
25	512	64000h-67FFFh
24	512	60000h-63FFFh
23	512	5C000h-5FFFFh
22	512	58000h-5BFFFh
21	512	54000h-57FFFh
20	512	50000h-53FFFh
19	512	4C000h-4FFFFh
18	512	48000h-4BFFFh
17	512	44000h-47FFFh
16	512	40000h-43FFFh
15	512	3C000h-3FFFFh
14	512	38000h-3BFFFh
13	512	34000h-37FFFh
12	512	30000h-33FFFh
11	512	2C000h-2FFFFh
10	512	28000h-2BFFFh
9	512	24000h-27FFFh
8	512	20000h-23FFFh
7	512	1C000h-1FFFFh
6	512	18000h-1BFFFh
5	512	14000h-17FFFh
4	512	10000h-13FFFh
3	512	0C000h-0FFFFh
2	512	08000h-0BFFFh
1	512	04000h-07FFFh
0	512	00000h-03FFFh

1. OTP block.

Table 5. M58BW16F bottom boot block addresses

#	Size (Kbit)	Address range
38	512	7C000h-7FFFFh
37	512	78000h-7BFFFh
36	512	74000h-77FFFh
35	512	70000h-73FFFh
34	512	6C000h-6FFFFh
33	512	68000h-6BFFFh
32	512	64000h-67FFFh
31	512	60000h-63FFFh
30	512	5C000h-5FFFFh
29	512	58000h-5BFFFh
28	512	54000h-57FFFh
27	512	50000h-53FFFh
26	512	4C000h-4FFFFh
25	512	48000h-4BFFFh
24	512	44000h-47FFFh
23	512	40000h-43FFFh
22	512	3C000h-3FFFFh
21	512	38000h-3BFFFh
20	512	34000h-37FFFh
19	512	30000h-33FFFh
18	512	2C000h-2FFFFh
17	512	28000h-2BFFFh
16	512	24000h-27FFFh
15	512	20000h-23FFFh
14	512	1C000h-1FFFFh
13	512	18000h-1BFFFh
12	512	14000h-17FFFh
11	512	10000h-13FFFh
10	512	0C000h-0FFFFh
9	512	08000h-0BFFFh
8	512	04000h-07FFFh
7	64	03800h-03FFFh
6	64	03000h-037FFh
5	64	02800h-02FFFh
4	64	02000h-027FFh
3(1)	64	01800h-01FFFh
2(1)	64	01000h-017FFh
1	64	00800h-00FFFh
0	64	00000h-007FFh

1. OTP block.

2 Signal descriptions

See *Figure 1: Logic diagram* and *Table 1: Signal names*, for a brief overview of the signals connected to this device.

2.1 Address inputs (A0-Amax)

Amax is equal to A18 in the M58BW16F, and to A19 in the M58BW32F.

The Address inputs are used to select the cells to access in the memory array during Bus operations. During Bus Write operations they control the commands sent to the command interface of the Program/Erase controller. Chip Enable must be Low when selecting the addresses.

The Address inputs are latched on the rising edge of Latch Enable $\overline{L}$ or Burst Clock K, whichever occurs first, in a Read operation. The Address inputs are latched on the rising edge of Chip Enable, Write Enable or Latch Enable, whichever occurs first in a Write operation. The address latch is transparent when Latch Enable is Low, V_{IL}. The address is internally latched in an Erase or Program operation.

2.2 Data inputs/outputs (DQ0-DQ31)

The Data inputs/outputs output the data stored at the selected address during a Bus Read operation, or are used to input the data during a program operation. During Bus Write operations they represent the commands sent to the command interface of the Program/Erase controller. When used to input data or Write commands they are latched on the rising edge of Write Enable or Chip Enable, whichever occurs first.

When Chip Enable and Output Enable are both Low, V_{IL}, and Output Disable is at V_{IH}, the data bus outputs data from the memory array, the Electronic Signature, the Block Protection Configuration Register, the CFI information or the contents of Burst Configuration Register or Status Register. The data bus is high impedance when the device is deselected with Chip Enable at V_{IH}, Output Enable at V_{IH}, Output Disable at V_{IL} or Reset/Power-down at V_{IL}. The Status Register content is output on DQ0-DQ7 and DQ8-DQ31 are at V_{IL}.

2.3 Chip Enable ($\overline{E}$)

The Chip Enable, $\overline{E}$, input activates the memory control logic, input buffers, decoders and sense amplifiers. Chip Enable, $\overline{E}$, at V_{IH} deselects the memory and reduces the power consumption to the standby level.

2.4 Output Enable ($\overline{G}$)

The Output Enable, $\overline{G}$, gates the outputs through the data output buffers during a Read operation, when Output Disable $\overline{GD}$ is at V_{IH}. When Output Enable $\overline{G}$ is at V_{IH}, the outputs are high impedance independently of Output Disable.

2.5 Output Disable ($\overline{GD}$)

The Output Disable, $\overline{GD}$, deactivates the data output buffers. When Output Disable, $\overline{GD}$, is at V_{IH}, the outputs are driven by the Output Enable. When Output Disable, $\overline{GD}$, is at V_{IL}, the outputs are high impedance independently of Output Enable. The Output Disable pin must be connected to an external pull-up resistor as there is no internal pull-up resistor to drive the pin.

2.6 Write Enable ($\overline{W}$)

The Write Enable, $\overline{W}$, input controls writing to the command interface, input address and data latches. Both addresses and data can be latched on the rising edge of Write Enable (also see Latch Enable, $\overline{L}$).

2.7 Reset/Power-down ($\overline{RP}$)

The Reset/Power-down, $\overline{RP}$, is used to apply a hardware reset to the memory. A hardware reset is achieved by holding Reset/Power-down Low, V_{IL}, for at least t_{PLPH}. Writing is inhibited to protect data, the command interface and the Program/Erase controller are reset. The Status Register information is cleared and power consumption is reduced to the standby level (I_{DD1}). The device acts as deselected, that is the data outputs are high impedance.

After Reset/Power-down goes High, V_{IH}, the memory will be ready for Bus Read operations after a delay of t_{PHEL} or Bus Write operations after t_{PHWL}.

If Reset/Power-down goes Low, V_{IL}, during a Block Erase or a Program operation, the internal state machine handles the operation as a Program/Erase Suspend, so the maximum time defined in *Table 12: Program, Erase times and endurance cycles* must be applied.

During power-up power should be applied simultaneously to V_{DD} and V_{DDQIN} with $\overline{RP}$ held at V_{IL}. When the supplies are stable $\overline{RP}$ is taken to V_{IH}. Output Enable, $\overline{G}$, Chip Enable, $\overline{E}$, and Write Enable, $\overline{W}$, should be held at V_{IH} during power-up.

In an application, it is recommended to associate the Reset/Power-down pin, $\overline{RP}$, with the reset signal of the microprocessor. Otherwise, if a Reset operation occurs while the memory is performing an Erase or program operation, the memory may output the Status Register information instead of being initialized to the default Asynchronous Random Read mode.

See *Table 24* and *Figure 22: Reset, Power-down and Power-up AC waveforms - Control pins Low*, for more details.

2.8 Program/Erase Enable (PEN)

The Program/Erase Enable input, PEN, protects all blocks by preventing Program and Erase operations from modifying the data.
Prior to issuing a Program or Erase command, the Program/Erase Enable must be set to High (V_{IH}). If it is Low (V_{IL}), the Program or Erase operation is not accepted and an error is generated in the Status Register.

2.9 Latch Enable ($\overline{L}$)

The Bus Interface can be configured to latch the Address inputs on the rising edge of Latch Enable, $\overline{L}$, for Asynchronous Latch Enable Controlled Read or Write or Synchronous Burst Read operations. In Synchronous Burst Read operations the address is latched on the active edge of the Clock when Latch Enable is Low, V_{IL}. Once latched, the addresses may change without affecting the address used by the memory. When Latch Enable is Low, V_{IL}, the latch is transparent. Latch Enable, $\overline{L}$, can remain at V_{IL} for Asynchronous Random Read and Write operations.

2.10 Burst Clock (K)

The Burst Clock, K, is used to synchronize the memory with the external bus during Synchronous Burst Read operations. Bus signals are latched on the active edge of the Clock. In Synchronous Burst Read mode the address is latched on the first rising clock edge when Latch Enable is Low, V_{IL}, or on the rising edge of Latch Enable, whichever occurs first.

During Asynchronous Bus Operations the Clock is not used.

2.11 Burst Address Advance ($\overline{B}$)

The Burst Address Advance, $\overline{B}$, controls the advancing of the address by the internal address counter during Synchronous Burst Read operations.

Burst Address Advance, $\overline{B}$, is only sampled on the active clock edge of the Clock when the X-latency time has expired. If Burst Address Advance is Low, V_{IL}, the internal address counter advances. If Burst Address Advance is High, V_{IH}, the internal address counter does not change; the same data remains on the Data inputs/outputs and Burst Address Advance is not sampled until the Y-latency expires.

The Burst Address Advance, $\overline{B}$, may be tied to V_{IL}.

2.12 Valid Data Ready (R)

The Valid Data Ready output, R, can be used during Synchronous Burst Read operations to identify if the memory is ready to output data or not. The Valid Data Ready output can be configured to be active on the clock edge of the invalid data read cycle or one cycle before. Valid Data Ready, at V_{IH}, indicates that new data is or will be available. When Valid Data Ready is Low, V_{IL}, the previous data outputs remain active.

2.13 Write Protect ($\overline{WP}$)

The Write Protect, $\overline{WP}$, provides protection against Program or Erase operations. When Write Protect, $\overline{WP}$, is at V_{IL}, the protection status that has been configured in the Block Protection Configuration Register is activated. Program and Erase operations to protected blocks are disabled. When Write Protect $\overline{WP}$ is at V_{IH} all the blocks can be programmed or erased, if no other protection is used.

2.14 Supply voltage (V_{DD})

The supply voltage, V_{DD}, is the core power supply. All internal circuits draw their current from the V_{DD} pin, including the Program/Erase controller.

2.15 Output supply voltage (V_{DDQ})

The output supply voltage, V_{DDQ}, is the output buffer power supply for all operations (Read, Program and Erase) used for DQ0-DQ31 when used as outputs.

2.16 Input supply voltage (V_{DDQIN})

The input supply voltage, V_{DDQIN}, is the power supply for all input signal. Input signals are: K, $\overline{B}$, $\overline{L}$, $\overline{W}$, $\overline{GD}$, $\overline{G}$, $\overline{E}$, A0-Amax and DQ0-DQ31, when used as inputs.

2.17 Ground (V_{SS} and V_{SSQ})

The ground V_{SS} is the reference for the internal supply voltage V_{DD}. The ground V_{SSQ} is the reference for the output and input supplies $V_{DDQ,}$ and V_{DDQIN}. It is essential to connect V_{SS} and V_{SSQ} together.

Note: A 0.1 µF capacitor should be connected between the supply voltages, V_{DD}, V_{DDQ} and V_{DDQIN} and the grounds, V_{SS} and V_{SSQ} to decouple the current surges from the power supply. The PCB track widths must be sufficient to carry the currents required during all operations of the parts, see Table 18: DC characteristics, for maximum current supply requirements.

2.18 Don't use (DU)

This pin should not be used as it is internally connected. Its voltage level can be between V_{SS} and V_{DDQ} or leave it unconnected.

2.19 Not connected (NC)

This pin is not physically connected to the device.

3 Bus operations

Each bus operations that controls the memory is described in this section, see tables *6* and *7* Bus operations, for a summary. The bus operation is selected through the Burst Configuration Register; the bits in this register are described at the end of this section.

On power-up or after a hardware reset the memory defaults to Asynchronous Bus Read and Asynchronous Bus Write. No synchronous operation can be performed until the Burst Control Register has been configured.

The Electronic Signature, Block Protection Configuration, CFI or Status Register will be read in asynchronous mode regardless of the Burst Control Register settings.

Typically glitches of less than 5 ns on Chip Enable or Write Enable are ignored by the memory and do not affect bus operations.

3.1 Asynchronous Bus operations

For asynchronous bus operations refer to *Table 6* together with the following text. The read access will start at whichever of the three following events occurs last: valid address transition, Chip Enable, $\overline{E}$, going Low, V_{IL} or Latch Enable, $\overline{L}$, going Low, V_{IL}.

3.1.1 Asynchronous Bus Read

Asynchronous Bus Read operations read from the memory cells, or specific registers (Electronic Signature, Block Protection Configuration Register, Status Register, CFI and Burst Configuration Register) in the command interface. A valid bus operation involves setting the desired address on the Address inputs, applying a Low signal, V_{IL}, to Chip Enable and Output Enable and keeping Write Enable and Output Disable High, V_{IH}. The Data inputs/outputs will output the value, see *Figure 7: Asynchronous Bus Read AC waveforms*, and *Table 19: Asynchronous Bus Read AC characteristics*, for details of when the output becomes valid.

Asynchronous Read is the default read mode which the device enters on power-up or on return from Reset/Power-down.

3.1.2 Asynchronous Latch Controlled Bus Read

Asynchronous Latch Controlled Bus Read operations read from the memory cells or specific registers in the command interface. The address is latched in the memory before the value is output on the data bus, allowing the address to change during the cycle without affecting the address that the memory uses.

A valid bus operation involves setting the desired address on the Address inputs, setting Chip Enable and Latch Enable Low, V_{IL} and keeping Write Enable High, V_{IH}; the address is latched on the rising edge of Latch Enable. Once latched, the Address inputs can change. Set Output Enable Low, V_{IL}, to read the data on the Data inputs/outputs; see *Figure 8: Asynchronous Latch Controlled Bus Read AC waveforms* and *Table 19: Asynchronous Bus Read AC characteristics*, for details on when the output becomes valid.

Note that, since the Latch Enable input is transparent when set Low, V_{IL}, Asynchronous Bus Read operations can be performed when the memory is configured for Asynchronous Latch Enable bus operations by holding Latch Enable Low, V_{IL} throughout the bus operation.

3.1.3 Asynchronous Page Read

Asynchronous Page Read operations are used to read from several addresses within the same memory page. Each memory page is 4 double-words and is addressed by the address inputs A0 and A1.

Data is read internally and stored in the page buffer. Valid bus operations are the same as Asynchronous Bus Read operations but with different timings. The first read operation within the page has identical timings, subsequent reads within the same page have much shorter access times. If the page changes then the normal, longer timings apply again. Page Read does not support Latched Controlled Read.

See *Figure 11: Asynchronous Page Read AC waveforms*, and *Table 20: Asynchronous Page Read AC characteristics*, for details on when the outputs become valid.

3.1.4 Asynchronous Bus Write

Asynchronous Bus Write operations write to the command interface in order to send commands to the memory or to latch addresses and input data to program. Bus Write operations are asynchronous, the clock, K, is don't care during Bus Write operations.

A valid Asynchronous Bus Write operation begins by setting the desired address on the Address inputs, and setting Chip Enable, Write Enable and Latch Enable Low, V_{IL}, and Output Enable High, V_{IH}, or Output Disable Low, V_{IL}. The Address inputs are latched by the command interface on the rising edge of Chip Enable or Write Enable, whichever occurs first. Commands and input data are latched on the rising edge of Chip Enable, $\overline{E}$, or Write Enable, $\overline{W}$, whichever occurs first. Output Enable must remain High, and Output Disable Low, during the whole Asynchronous Bus Write operation.

See *Figure 12: Asynchronous Write AC waveforms*, and *Table 21: Asynchronous Write and Latch controlled Write AC characteristics*, for details of the timing requirements.

3.1.5 Asynchronous Latch Controlled Bus Write

Asynchronous Latch Controlled Bus Write operations write to the command interface in order to send commands to the memory or to latch addresses and input data to program. Bus Write operations are asynchronous, the clock, K, is Don't care during Bus Write operations.

A valid Asynchronous Latch Controlled Bus Write operation begins by setting the desired address on the Address inputs and pulsing Latch Enable Low, V_{IL}. The Address inputs are latched by the command interface on the rising edge of Latch Enable, Write Enable or Chip Enable, whichever occurs first. Commands and input data are latched on the rising edge of Chip Enable, $\overline{E}$, or Write Enable, $\overline{W}$, whichever occurs first. Output Enable must remain High, and Output Disable Low, during the whole Asynchronous Bus Write operation.

See *Figure 13: Asynchronous Latch controlled Write AC waveforms*, and *Table 21: Asynchronous Write and Latch controlled Write AC characteristics*, for details of the timing requirements.

3.1.6 Output Disable

The data outputs are high impedance when the Output Enable, $\overline{G}$, is at V_{IH} or Output Disable, $\overline{GD}$, is at V_{IL}.

3.1.7 Standby

When Chip Enable is High, V_{IH}, and the Program/Erase controller is idle, the memory enters Standby mode, the power consumption is reduced to the standby level (I_{DD1}) and the Data inputs/outputs pins are placed in the high impedance state regardless of Output Enable, Write Enable or Output Disable inputs.

The Standby mode can be disabled by setting the Standby Disable bit (M14) of the Burst Configuration Register to '1' (see *Table 18: DC characteristics*).

3.1.8 Reset/Power-down

The memory is in Reset/Power-down mode when Reset/Power-down, $\overline{RP}$, is at V_{IL}. The power consumption is reduced to the standby level (I_{DD1}) and the outputs are high impedance, independent of the Chip Enable, $\overline{E}$, Output Enable, $\overline{G}$, Output Disable, $\overline{GD}$, or Write Enable, $\overline{W}$, inputs. In this mode the device is write protected and both the Status and the Burst Configuration Registers are cleared. A recovery time is required when the $\overline{RP}$ input goes High.

Table 6. Asynchronous Bus operations(1)

Bus operation	Step	$\overline{E}$	$\overline{G}$	$\overline{GD}$	$\overline{W}$	$\overline{RP}$	$\overline{L}$	A0-Amax	DQ0-DQ31
Asynchronous Bus Read(2)		V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IH}	V_{IL}	Address	Data output
Asynchronous Latch Controlled Bus Read	Address Latch	V_{IL}	V_{IH}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	Address	High Z
	Read	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IH}	V_{IH}	X	Data output
Asynchronous Page Read		V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IH}	X	Address	Data output
Asynchronous Bus Write		V_{IL}	V_{IH}	X	V_{IL}	V_{IH}	V_{IL}	Address	Data input
Asynchronous Latch Controlled Bus Write	Address Latch	V_{IL}	V_{IH}	X	V_{IH}	V_{IH}	V_{IL}	Address	High Z
	Write	V_{IL}	V_{IH}	X	V_{IL}	V_{IH}	V_{IH}	X	Data input
Output Enable, $\overline{G}$		V_{IL}	V_{IH}	V_{IH}	V_{IH}	V_{IH}	X	X	High Z
Output Disable, $\overline{GD}$		V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{IH}	X	X	High Z
Standby		V_{IH}	X	X	X	V_{IH}	X	X	High Z
Reset/Power-down		X	X	X	X	V_{IL}	X	X	High Z

1. X = Don't care.
2. Data, Manufacturer code, Device code, Burst Configuration Register, Standby Status and Block Protection Configuration Register are read using the Asynchronous Bus Read command.

3.2 Synchronous Bus operations

For Synchronous Bus Operations refer to *Table 7* together with the following text. The read access will start at whichever of the three following events occurs last: valid address transition, Chip Enable, $\overline{E}$, going Low, V_{IL} or Latch Enable, $\overline{L}$, going Low, V_{IL}.

3.2.1 Synchronous Burst Read

Synchronous Burst Read operations are used to read from the memory at specific times synchronized to an external reference clock. The valid edge of the Clock signal is the rising edge. Once the Flash memory is configured in Burst mode, it is mandatory to have an active clock signal since the switching of the output buffer databus is synchronized to the rising edge of the clock. In the absence of clock, no data is output.

The burst type, length and latency can be configured. The different configurations for Synchronous Burst Read operations are described in the Burst Configuration Register section. Refer to *Figure 4* for examples of Synchronous Burst operations.

A valid Synchronous Burst Read operation begins when the Burst Clock is active and Chip Enable and Latch Enable are Low, V_{IL}. The burst start address is latched and loaded into the internal Burst Address counter on the valid Burst Clock K edge or on the rising edge of Latch Enable, whichever occurs first.

After an initial memory latency time, the memory outputs data each clock cycle. The Burst Address Advance $\overline{B}$ input controls the memory burst output. The second burst output is on the next clock valid edge after the Burst Address Advance $\overline{B}$ has been pulled Low.

Valid Data Ready, R, monitors if the memory burst boundary is exceeded and the Burst Controller of the microprocessor needs to insert wait states. When Valid Data Ready is Low on the rising clock edge, no new data is available and the memory does not increment the internal address counter at the active clock edge even if Burst Address Advance, $\overline{B}$, is Low.

Valid Data Ready may be configured (by bit M8 of Burst Configuration Register) to be valid immediately at the rising clock edge.

Synchronous Burst Read will be suspended if Burst Address Advance, $\overline{B}$, goes High, V_{IH}.

If Output Enable is at V_{IL} and Output Disable is at V_{IH}, the last data is still valid.

If Output Enable, $\overline{G}$, is at V_{IH} or Output Disable, $\overline{GD}$, is at V_{IL}, but the Burst Address Advance, $\overline{B}$, is at V_{IL} the internal Burst Address counter is incremented at each Burst Clock K rising edge.

The Synchronous Burst Read timing diagrams and AC characteristics are described in the AC and DC parameters section. See Figures *14*, *17*, *18* and *19*, and *Table 22*.

3.2.2 Synchronous Burst Read Suspend

During a Synchronous Burst Read operation it is possible to suspend the operation, freeing the data bus for other higher priority devices.

A valid Synchronous Burst Read operation is suspended when both Output Enable and Burst Address Advance are High, V_{IH}. The Burst Address Advance going High, V_{IH}, stops the Burst counter and the Output Enable going High, V_{IH}, inhibits the data outputs. The Synchronous Burst Read operation can be resumed by setting Output Enable Low.

Table 7. Synchronous Burst Read Bus operations(1)

Bus operation	Step	$\overline{E}$	$\overline{G}$	$\overline{GD}$	$\overline{RP}$	K	$\overline{L}$	$\overline{B}$	A0-Amax DQ0-DQ31
Synchronous Burst Read(2)	Address Latch	V_{IL}	V_{IH}	X	V_{IH}	R(3)	V_{IL}	X	Address input
	Read	V_{IL}	V_{IL}	V_{IH}	V_{IH}	R(3)	V_{IH}	V_{IL}	Data output
	Read Suspend	V_{IL}	V_{IH}	X	V_{IH}	X	V_{IH}	V_{IH}	High Z
	Read Resume	V_{IL}	V_{IL}	V_{IH}	V_{IH}	R(3)	V_{IH}	V_{IL}	Data output
	Burst Address Advance	V_{IL}	V_{IH}	X	V_{IH}	R(3)	V_{IH}	V_{IL}	High Z
	Read Abort, $\overline{E}$	V_{IH}	X	X	V_{IH}	X	X	X	High Z
	Read Abort, $\overline{RP}$	X	X	X	V_{IL}	X	X	X	High Z

1. X = Don't care, V_{IL} or V_{IH}.
2. M15 = 0, Bit M15 is in the Burst Configuration Register.
3. R = Rising edge.

3.3 Burst Configuration Register

The Burst Configuration Register is used to configure the type of bus access that the memory will perform.

The Burst Configuration Register is set through the command interface and will retain its information until it is re-configured, the device is reset, or the device goes into Reset/Power-down mode. The Burst Configuration Register bits are described in *Table 8*. They specify the selection of the Burst length, Burst type, Burst X and Y latencies and the Read operation. Refer to *Figure 4* for examples of Synchronous Burst configurations.

3.3.1 Read Select bit (M15)

The Read Select bit, M15, is used to switch between Asynchronous and Synchronous Bus Read operations. When the Read Select bit is set to '1', Bus Read operations are asynchronous; when the Read Select bit is set to '0', Bus Read operations are synchronous.

On reset or power-up the Read Select bit is set to'1' for asynchronous accesses.

3.3.2 Standby Disable bit (M14)

The Standby Disable bit, M14, is used to disable the Standby mode. When the Standby bit is '1', the device will not enter Standby mode when Chip Enable goes High, V_{IH}.

3.3.3 X-Latency bits (M13-M11)

The X-Latency bits are used during Synchronous Bus Read operations to set the number of clock edges between the address being latched and the edge where the first data become available. For correct operation the X-Latency bits can only assume the values in *Table 8: Burst Configuration Register*.

3.3.4 Y-Latency bit (M9)

The Y-Latency bit is used during Synchronous Bus Read operations to set the number of clock cycles between consecutive reads. The Y-Latency value depends on both the X-Latency value and the setting in M9.

When the Y-Latency is 1 the data changes each clock cycle.

3.3.5 Valid Data Ready bit (M8)

The Valid Data Ready bit controls the timing of the Valid Data Ready output pin, R. When the Valid Data Ready bit is ’0’ the Valid Data Ready output pin is driven Low for the rising clock edge when invalid data is output on the bus.

3.3.6 Wrap Burst bit (M3)

Burst Read can be confined inside the 4 double-word boundary (wrap) or overcome the boundary (no wrap). When the wrap burst bit is set to '1' the burst read does not wrap. The wrap mode is not available (M3 is always ‘1’).

3.3.7 Burst Length bit (M2-M0)

The Burst Length bits set the maximum number of double-words that can be output during a Synchronous Burst Read operation. Burst lengths of 4 or 8 are available.

Table 8: Burst Configuration Register gives the valid combinations of the Burst Length bits that the memory accepts.

If a Burst Read operation (no wrap) has been initiated the device will output data synchronously. Depending on the starting address, the device activates the Valid Data Ready output to indicate that a delay is necessary before the data is output. If the starting address is aligned to a 4 double word boundary, the 8-double-word burst mode will run without activating the Valid Data Ready output. If the starting address is not aligned to a 4 double word boundary, Valid Data Ready is activated to indicate that the device needs an internal delay to read the successive words in the array.

M10, M7 to M4 are reserved for future use.

Table 8. Burst Configuration Register

Bit	Description	Value	Description
M15	Read Select	0	Synchronous Burst Read
		1	Asynchronous Read (default at power-on)
M14	Standby Disable	0	Standby mode enabled (default at power-up)
		1	Standby mode disabled
M13-M11	X-Latency(1)	000	Reserved (default value)
		001	3, 3-1-1-1, 3-2-2-2
		010	4, 4-1-1-1, 4-2-2-2
		011	5, 5-1-1-1, 5-2-2-2
		100	6, 6-1-1-1, 6-2-2-2
		101	7, 7-1-1-1, 7-2-2-2
		110	8, 8-1-1-1, 8-2-2-2
		111	Reserved
M10		0	Reserved (default value)
		1	Reserved
M9	Y-Latency(2)	0	One Burst Clock cycle (default value)
		1	Two Burst Clock cycle
M8	Valid Data Ready	0	R valid Low during valid Burst Clock edge (default value)
		1	R valid Low 1 data cycle before valid Burst Clock edge
M7		0	Reserved (default value)
		1	Reserved
M6(3)		0	Falling Burst Clock edge (default value)
		1	Rising Burst Clock edge
M5-M4		00	Reserved (default value)
		01	Reserved
		10	Reserved
		11	Reserved
M3	Wrapping	0	Wrap (default value)
		1	No Wrap

Table 8. Burst Configuration Register (continued)

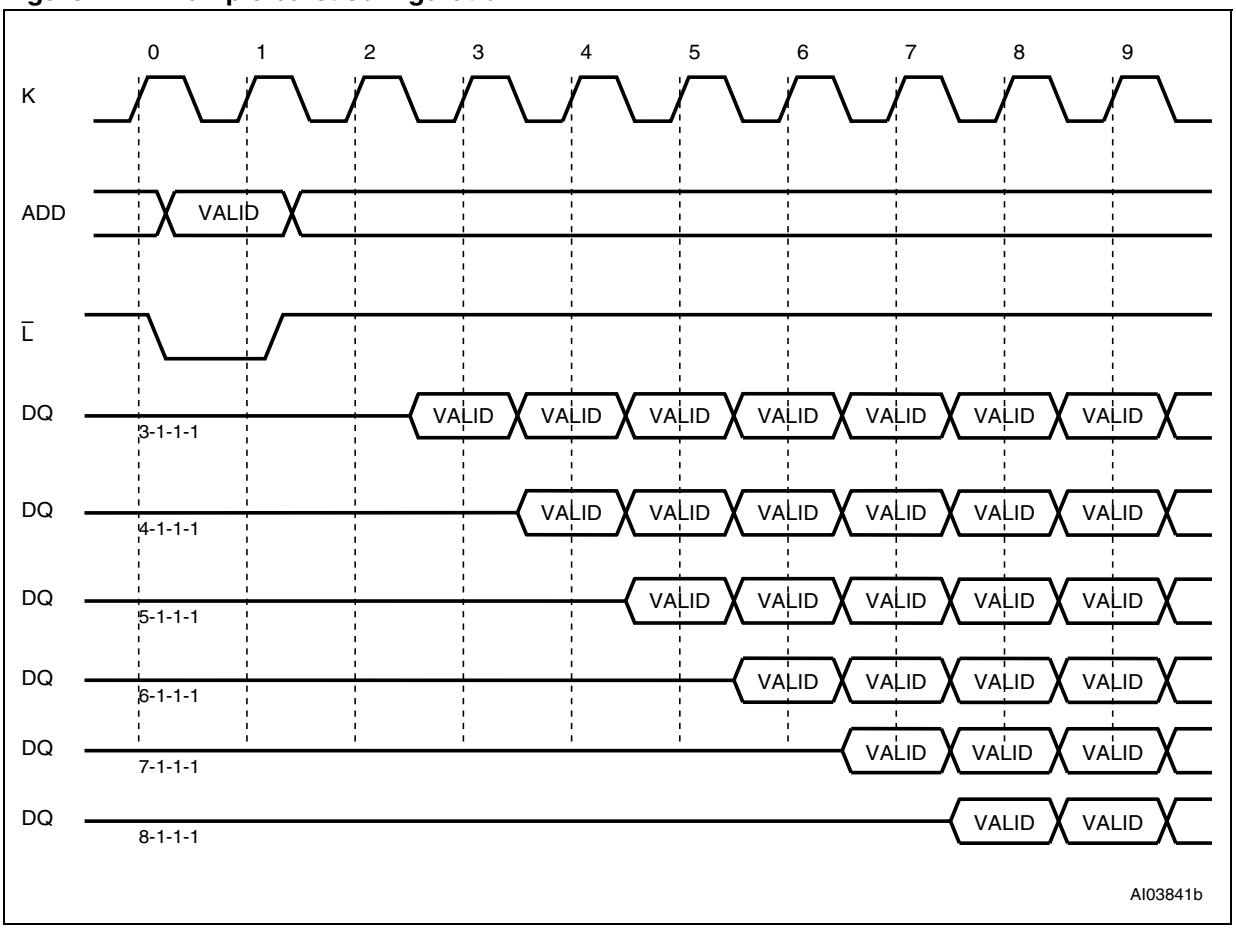
Bit	Description	Value	Description
M2-M0	Burst Length	000	Reserved (default value)
		001	4 double-words
		010	8 double-words
		011	Reserved
		100	Reserved
		101	Reserved
		110	Reserved
		111	Continuous

1. X latencies can be calculated as: $(t_{AVQV} - t_{LLKH} + t_{QVKH}) + t_{SYSTEM\ MARGIN} < (X - 1)\ t_K$. X is an integer number from 4 to 8, t_K is the clock period and $t_{SYSTEM\ MARGIN}$ is the time margin required for the calculation.
2. Y latencies can be calculated as: $t_{KHQV} + t_{SYSTEM\ MARGIN} + t_{QVKH} < Y\ t_K$.
3. The M6 bit is Don't care in the M58BW32F and the device has the Rising Burst Clock edge set. To maintain the compatibility this could be modified and read.

Table 9. Burst type definition

Start address	× 4 sequential	× 8 sequential
0	0-1-2-3	0-1-2-3-4-5-6-7
1	1-2-3-4	1-2-3-4-5-6-7-8
2	2-3-4-5	2-3-4-5-6-7-8-9
3	3-4-5-6	3-4-5-6-7-8-9-10
4	4-5-6-7	4-5-6-7-8-9-10-11
5	5-6-7-8	5-6-7-8-9-10-11-12
6	6-7-8-9	6-7-8-9-10-11-12-13
7	7-8-9-10	7-8-9-10-11-12-13-14
8	8-9-10-11	8-9-10-11-12-13-14-15

Figure 4. Example burst configuration X-1-1-1



4 Command interface

All Bus Write operations to the memory are interpreted by the command interface. Commands consist of one or more sequential Bus Write operations. The commands are summarized in *Table 10: Commands*. Refer to *Table 10* in conjunction with the text descriptions below.

4.1 Read Memory Array command

The Read Memory Array command returns the memory to Read mode. One Bus Write cycle is required to issue the Read Memory Array command and return the memory to Read mode. Subsequent Read operations will output the addressed memory array data. Once the command is issued the memory remains in Read mode until another command is issued. From Read mode Bus Read commands will access the memory array.

4.2 Read Electronic Signature command

The Read Electronic Signature command is used to read the Manufacturer code, the Device code, the Block Protection Configuration Register and the Burst Configuration Register. One Bus Write cycle is required to issue the Read Electronic Signature command. Once the command is issued, subsequent Bus Read operations, depending on the address specified, read the Manufacturer code, the Device code, the Block Protection Configuration or the Burst Configuration Register until another command is issued; see *Table 11: Read electronic signature*.

4.3 Read Query command

The Read Query command is used to read data from the common Flash interface (CFI) memory area. One Bus Write cycle is required to issue the Read Query command. Once the command is issued subsequent Bus Read operations, depending on the address specified, read from the common Flash interface memory area.

4.4 Read Status Register command

The Read Status Register command is used to read the Status Register. One Bus Write cycle is required to issue the Read Status Register command. Once the command is issued subsequent Bus Read operations read the Status Register until another command is issued.

The Status Register information is present on the output data bus (DQ0-DQ7) when Chip Enable $\overline{E}$ and Output Enable $\overline{G}$ are at V_{IL} and Output Disable is at V_{IH}.

An interactive update of the Status Register bits is possible by toggling Output Enable or Output Disable. It is also possible during a Program or Erase operation, by de-activating the device with Chip Enable at V_{IH} and then reactivating it with Chip Enable and Output Enable at V_{IL} and Output Disable at V_{IH}.

The content of the Status Register may also be read at the completion of a Program, Erase or Suspend operation. During a Block Erase or Program command, DQ7 indicates the Program/Erase controller status. It is valid until the operation is completed or suspended.

See the section on the Status Register and *Table 13* for details on the definitions of the Status Register bits.

4.5 Clear Status Register command

The Clear Status Register command can be used to reset bits 1, 3, 4 and 5 in the Status Register to ‘0’. One Bus Write is required to issue the Clear Status Register command. Once the command is issued the memory returns to its previous mode, subsequent Bus Read operations continue to output the same data.

The bits in the Status Register are sticky and do not automatically return to ‘0’ when a new Program, Erase, Block Protect or Block Unprotect command is issued. If any error occurs then it is essential to clear any error bits in the Status Register by issuing the Clear Status Register command before attempting a new Program, Erase or Resume command.

4.6 Block Erase command

The Block Erase command can be used to erase a block. It sets all of the bits in the block to ‘1’. All previous data in the block is lost. If the block is protected then the Erase operation will abort, the data in the block will not be changed and the Status Register will output the error.

Two Bus Write operations are required to issue the command; the first write cycle sets up the Block Erase command, the second write cycle confirms the Block Erase command and latches the block address in the Program/Erase controller and starts the Program/Erase controller. The sequence is aborted if the Confirm command is not given and the device will output the Status Register Data with bits 4 and 5 set to '1'.

Once the command is issued subsequent Bus Read operations read the Status Register. See the section on the Status Register for details on the definitions of the Status Register bits. During the Erase operation the memory will only accept the Read Status Register command and the Program/Erase Suspend command. All other commands will be ignored.

If PEN is at V_{IH}, the operation can be performed. If PEN goes below V_{IH}, the operation aborts, the PEN Status bit in the Status Register is set to ‘1’ and the command must be re-issued.

Typical Erase times are given in *Table 12*. See *Appendix A*, *Figure 28: Block Erase flowchart and pseudocode*, for a suggested flowchart on using the Block Erase command.

4.7 Erase All Main Blocks command

The Erase All Main Blocks command is used to erase all 63 main blocks, without affecting the parameter blocks.

Issuing the Erase All Main Blocks command sets every bit in each main block to '1'. All data previously stored in the main blocks are lost.

Two Bus Write cycles are required to issue the Erase All Main Blocks command. The first cycle sets up the command, the second cycle confirms the command and starts the Program/Erase controller. If the Confirm command is not given the sequence is aborted, and Status Register bits 4 and 5 are set to '1'.
If the address given in the second cycle is located in a protected block, the Erase All Main Blocks operation aborts. The data remains unchanged in all blocks and the Status Register outputs the error.

Once the Erase All Main Blocks command has been issued, subsequent Bus Read operations output the Status Register. See the *Status Register* section for details.

During an Erase All Main Blocks operation, only the Read Status Register command is accepted by the memory; any other command are ignored. Erase All Main Blocks, once started, cannot be suspended.

If PEN is at V_{IH}, the operation will be performed. If PEN is lower than V_{IH} the operation aborts and the Status Register PEN bit (bit 3) is set to '1'.

4.8 Program command

The Program command is used to program the memory array. Two Bus Write operations are required to issue the command; the first write cycle sets up the Program command, the second write cycle latches the address and data to be programmed and starts the Program/Erase controller. A program operation can be aborted by writing FFFFFFFFh to any address after the program set-up command has been given.

The Program command is also used to program the OTP block. Refer to *Table 10: Commands*, for details of the address.

Once the command is issued subsequent Bus Read operations read the Status Register. See the section on the Status Register for details on the definitions of the Status Register bits. During the Program operation the memory will only accept the Read Status Register command and the Program/Erase Suspend command. All other commands will be ignored.

If Reset/Power-down, $\overline{RP}$, falls to V_{IL} during programming the operation will be aborted.

If PEN is at V_{IH}, the operation can be performed. If PEN goes below V_{IH}, the operation aborts, the PEN Status bit in the Status Register is set to ‘1’ and the command must be re-issued.

See *Appendix A*, *Figure 26: Program flowchart and pseudocode*, for a suggested flowchart on using the Program command.

4.9 Write to Buffer and Program command

The Write to Buffer and Program command makes use of the device's double word (32 bit) Write Buffer to speed up programming.

Up to eight double words can be loaded into the Write Buffer and programmed into the memory.

Four successive steps are required to issue the command.

1. One Bus Write operation is required to set up the Write to Buffer and Program command. Any Bus Read operations will start to output the Status Register after the 1st cycle.
2. Use one Bus Write operation to write the selected memory block address (any address in the block where the values will be programmed can be used) along with the value N on the Data inputs/outputs, where N+1 is the number of words to be programmed. The maximum value of N+1 is 8 words.
3. Use N+1 Bus Write operations to load the address and data for each word into the write buffer. The address must be between Start address and Start address plus N, where Start address is the first word address.
4. Finally, use one Bus Write operation to issue the final cycle to confirm the command and start the Program operation.

If any address is outside the block boundaries or if the correct sequence is not followed, Status Register bits 4 and 5 are set to '1' and the operation will abort without affecting the data in the memory array. A protected block must be unprotected using the Blocks Unprotect command.

During a Write to Buffer and Program operation the memory will only accept the Read Status Register and the Program/Erase Suspend commands. All other commands are ignored. If PEN is at V_{IH}, the operation will be performed. If PEN is lower than V_{IH} the operation aborts and the Status Register PEN bit (bit 3) is set to '1'.

The Status Register should be cleared before re-issuing the command.

4.10 Program/Erase Suspend command

The Program/Erase Suspend command is used to pause a Program or Erase operation. The command will only be accepted during a Program or Erase operation. It can be issued at any time during a Program or Erase operation. The command is ignored if the device is already in suspend mode.

One Bus Write cycle is required to issue the Program/Erase Suspend command and pause the Program/Erase controller. Once the command is issued it is necessary to poll the Program/Erase Controller Status bit (bit 7) to find out when the Program/Erase controller has paused; no other commands will be accepted until the Program/Erase controller has paused. After the Program/Erase controller has paused, the memory will continue to output the Status Register until another command is issued.

During the polling period between issuing the Program/Erase Suspend command and the Program/Erase Controller pausing it is possible for the operation to complete. Once the Program/Erase Controller Status bit (bit 7) indicates that the Program/Erase controller is no longer active, the Program Suspend Status bit (bit 2) or the Erase Suspend Status bit (bit 6) can be used to determine if the operation has completed or is suspended. For timing on the delay between issuing the Program/Erase Suspend command and the Program/Erase controller pausing see *Table 12*.

During Program/Erase Suspend the Read Memory Array, Read Status Register, Read Electronic Signature, Read Query and Program/Erase Resume commands will be accepted by the command interface. Additionally, if the suspended operation was Erase then the Program, the Write to Buffer and Program, the Set/Clear Block Protection Configuration Register and the Program Suspend commands will also be accepted. When a program operation is completed inside a Block Erase Suspend the Read Memory Array command must be issued to reset the device in Read mode, then the Erase Resume command can be issued to complete the whole sequence. Only the blocks not being erased may be read or programmed correctly.

Erase operations can be suspended in a systematic and periodical way, however, in order to ensure the effectiveness of erase operations and avoid infinite erase times, it is imperative to wait a minimum time between successive Erase Resume and Erase Suspend commands. This time, called the minimum effective erase time, is given in *Table 12 on page 40*.

See *Appendix A*, *Figure 27: Program Suspend & Resume flowchart and pseudocode*, and *Figure 29: Erase Suspend & Resume flowchart and pseudocode*, for suggested flowcharts on using the Program/Erase Suspend command.

4.11 Program/Erase Resume command

The Program/Erase Resume command can be used to restart the Program/Erase controller after a Program/Erase Suspend operation has paused it. One Bus Write cycle is required to issue the Program/Erase Resume command.

See *Appendix A*, *Figure 27: Program Suspend & Resume flowchart and pseudocode*, and *Figure 29: Erase Suspend & Resume flowchart and pseudocode*, for suggested flowcharts on using the Program/Erase Suspend command.

4.12 Set Burst Configuration Register command

The Set Burst Configuration Register command is used to write a new value to the Burst Configuration Register which defines the burst length, type, X and Y latencies, Synchronous/Asynchronous Read mode.

Two Bus Write cycles are required to issue the Set Burst Configuration Register command. The first cycle writes the setup command. The second cycle writes the address where the new Burst Configuration Register content is to be written, and confirms the command. If the command is not confirmed, the sequence is aborted and the device outputs the Status Register with bits 4 and 5 set to '1'. Once the command is issued the memory returns to Read mode as if a Read Memory Array command had been issued.

The value for the Burst Configuration Register is always presented on A0-A15. M0 is on A0, M1 on A1, etc.; the other address bits are ignored.

4.13 Set Block Protection Configuration Register command

The Set Block Protection Configuration Register command is used to configure the Block Protection Configuration Register to 'protected', for a specific block. Protected blocks are fully protected from program or erase when $\overline{WP}$ pin is Low, V_{IL}. The status of a protected block can be changed to 'unprotected' by using the Clear Block Protection Configuration Register command. At power-up, all block are configured as 'protected'.

Two bus operations are required to issue a Set Block Protection Configuration Register command:

- The first cycle writes the setup command
- The second write cycle specifies the address of the block to protect and confirms the command. If the command is not confirmed, the sequence is aborted and the device outputs the Status Register with bits 4 and 5 set to '1'.

To protect multiple blocks, the Set Block Protection Configuration Register command must be repeated for each block.

Any attempt to re-protect a block already protected does not change its status.

4.14 Clear Block Protection Configuration Register command

The Clear Block Protection Configuration Register command is used to configure the Block Protection Configuration Register to 'unprotected', for a specific block thus allowing program/erase operations to this block, regardless of the $\overline{WP}$ pin status.

Two bus operations are required to issue a Clear Block Protection Configuration Register command:

- The first cycle writes the setup command
- The second write cycle specifies the address of the block to unprotect and confirms the command. If the command is not confirmed, the sequence is aborted and the device outputs the Status Register with bits 4 and 5 set to '1'.

To unprotect multiple blocks, the Clear Block Protection Configuration Register command must be repeated for each block.

Any attempt to unprotect a block already unprotected does not affect its status.

Table 10. Commands(1)

Command		Cycles	Bus operations											
			1st cycle			2nd cycle			3rd cycle			4th cycle		
			Op.	Addr.	Data	Op.	Addr.	Data	Op.	Addr.	Data	Op.	Addr.	Data
Read Memory Array		≥ 2	Write	X	FFh	Read	RA	RD						
Read Electronic Signature(2)		≥ 2	Write	X	90h	Read	IDA	IDD						
Read Status Register		1	Write	X	70h									
Read Query		≥ 2	Write	X	98h	Read	RA	RD						
Clear Status Register		1	Write	X	50h									
Block Erase		2	Write	55h	20h	Write	BA	D0h						
Erase All Main Blocks		2	Write	55h	80h	Write	AAh	D0h						
Program	any block	2	Write	AAh	40h 10h	Write	PA	PD						
	OTP block	2	Write	AAh	40h	Write	PA	PD						
Write to Buffer and Program		N+4	Write	AAh	E8h	Write	BA	N	Write	PA	PD	Write	X	D0h
Program/Erase Suspend		1	Write	X	B0h									
Program/Erase Resume		1	Write	X	D0h									
Set Burst Configuration Register		Š3	Write	X	60h	Write	BCRh	03h	Read	RA	RD			
Set Block Protection Configuration Register		2	Write	X	60h	Write	BA	01h						
Clear Block Protection Configuration Register		2	Write	X	60h	Write	BA	D0h						

1. X Don't care; RA Read Address, RD Read Data, ID Device Code, IDA Identifier Address, IDD Identifier Data, SRD Status Register Data, PA Program Address; PD Program Data, QA Query Address, QD Query Data, BA Any address in the Block, BCR Burst Configuration Register value, N+1 number of Words to program, BA Block address.
2. The Manufacturer code, the Device code, the Burst Configuration Register, and the Block Protection Configuration Register of each block are read using the Read Electronic Signature command.

Table 11. Read electronic signature

Code	Device	Amax-A0	DQ31-DQ0
Manufacturer	All	00000h	00000020h
Device	M58BW16FT	00001h	0000883Ah
	M58BW16FB	00001h	00008839h
	M58BW32FT	00001h	00008838h
	M58BW32FB	00001h	00008837h
Burst Configuration Register		00005h	BCR(1)
Block Protection Configuration Register	All	SBA+02h(2)	00000000h (Unprotected)
			00000001h (Protected)

1. BCR = Burst Configuration Register.
2. SBA is the start address of each block.

Table 12. Program, Erase times and endurance cycles(1)

Parameters	M58BW16F			M58BW32F			Unit
	Min	Typ	Max	Min	Typ	Max	
Full Chip Program		15	20		15	20	s
Double Word Program		15	35		15	35	µs
512 Kbit Block Erase		1	2		1	2	s
128 Kbit Block Erase		0.8	1.6		0.8	1.6	s
64 Kbit Block Erase		0.6	1.2		0.6	1.2	s
Erase all main blocks		45	60		30	50	s
Program Suspend Latency time			10			10	µs
Erase Suspend Latency time			30			30	µs
Minimum effective erase time(2)			40			40	µs
Program/Erase cycles (per block)			100,000			100,000	cycles

1. T_A = –40 to 125 °C, V_{DD} = 2.7 V to 3.6 V, V_{DDQ} = 2.6 V to V_{DD}.
2. The minimum effective erase time is defined as the minimum time required between the last Erase Resume command and the next Erase Suspend command for the internal Flash memory Program/Erase controller to be able to execute its algorithm.

5 Status Register

The Status Register provides information on the current or previous Program, Erase or Block Protect operation. The various bits in the Status Register convey information and errors on the operation. They are output on DQ7-DQ0.

To read the Status Register the Read Status Register command can be issued. The Status Register is automatically read after Program, Erase, Block Protect, Program/Erase Resume commands. The Status Register can be read from any address.

The contents of the Status Register can be updated during an erase or program operation by toggling the Output Enable or Output Disable pins or by de-activating (Chip Enable, V_{IH}) and then reactivating (Chip Enable and Output Enable, V_{IL}, and Output Disable, V_{IH}.) the device.

The Status Register bits are summarized in *Table 13: Status Register bits*. Refer to *Table 13* in conjunction with the following text descriptions.

5.1 Program/Erase Controller Status (bit 7)

The Program/Erase Controller Status bit indicates whether the Program/Erase controller is active or inactive. When the Program/Erase Controller Status bit is set to ‘0’, the Program/Erase controller is active; when bit 7 is set to ‘1’, the Program/Erase controller is inactive.

The Program/Erase Controller Status is set to ‘0’ immediately after a Program/Erase Suspend command is issued until the Program/Erase Controller pauses. After the Program/Erase Controller pauses the bit is set to ‘1’.

During Program and Erase operations the Program/Erase Controller Status bit can be polled to find the end of the operation. The other bits in the Status Register should not be tested until the Program/Erase controller completes the operation and the bit is set to ‘1’.

After the Program/Erase controller completes its operation the Erase Status (bit 5), Program Status (bit 4) bits should be tested for errors.

5.2 Erase Suspend Status (bit 6)

The Erase Suspend Status bit indicates that an Erase operation has been suspended and is waiting to be resumed. The Erase Suspend Status should only be considered valid when the Program/Erase Controller Status bit is set to ‘1’ (Program/Erase controller inactive); after a Program/Erase Suspend command is issued the memory may still complete the operation rather than entering the Suspend mode.

When the Erase Suspend Status bit is set to ‘0’, the Program/Erase controller is active or has completed its operation; when the bit is set to ‘1’, a Program/Erase Suspend command has been issued and the memory is waiting for a Program/Erase Resume command.

When a Program/Erase Resume command is issued the Erase Suspend Status bit returns to ‘0’.

5.3 Erase Status (bit 5)

The Erase Status bit can be used to identify if the memory has failed to verify that the block has erased correctly. The Erase Status bit should be read once the Program/Erase Controller Status bit is High (Program/Erase controller inactive).

When the Erase Status bit is set to ‘0’, the memory has successfully verified that the block has erased correctly. When the Erase Status bit is set to ‘1’, the Program/Erase controller has applied the maximum number of pulses to the block and still failed to verify that the block has erased correctly.

Once set to ‘1’, the Erase Status bit can only be reset to ‘0’ by a Clear Status Register command or a hardware reset. If set to ‘1’ it should be reset before a new Program or Erase command is issued, otherwise the new command will appear to fail.

5.4 Program/Write to Buffer and Program Status (bit 4)

The Program/Write to Buffer and Program Status bit is used to identify a Program failure or a Write to Buffer and Program failure. Bit 4 should be read once the Program/Erase Controller Status bit is High (Program/Erase controller inactive).

When bit 4 is set to ‘0’ the memory has successfully verified that the device has programmed correctly. When bit 4 is set to ‘1’ the device has failed to verify that the data has been programmed correctly.

Once set to ‘1’, the Program Status bit can only be reset to ‘0’ by a Clear Status Register command or a hardware reset. If set to ‘1’ it should be reset before a new Program or Erase command is issued, otherwise the new command will appear to fail.

5.5 PEN Status (bit 3)

The PEN Status bit can be used to identify if a Program or Erase operation has been attempted when PEN is Low, V_{IL}.

When bit 3 is set to ‘0’ no Program or Erase operations have been attempted with PEN Low, V_{IL}, since the last Clear Status Register command, or hardware reset.

When bit 3 is set to ‘1’ a Program or Erase operation has been attempted with PEN Low, V_{IL}.

Once set to ‘1’, bit 3 can only be reset by a Clear Status Register command or a hardware reset. If set to ‘1’ it should be reset before a new Program or Erase command is issued, otherwise the new command will appear to fail.

5.6 Program Suspend Status (bit 2)

The Program Suspend Status bit indicates that a Program operation has been suspended and is waiting to be resumed. The Program Suspend Status should only be considered valid when the Program/Erase Controller Status bit is set to ‘1’ (Program/Erase Controller inactive); after a Program/Erase Suspend command is issued the memory may still complete the operation rather than entering the Suspend mode.

When the Program Suspend Status bit is set to ‘0’, the Program/Erase controller is active or has completed its operation; when the bit is set to ‘1’, a Program/Erase Suspend command has been issued and the memory is waiting for a Program/Erase Resume command.

When a Program/Erase Resume command is issued the Program Suspend Status bit returns to ‘0’.

5.7 Block Protection Status (bit 1)

The Block Protection Status bit can be used to identify if a Program or Erase operation has tried to modify the contents of a protected block.

When the Block Protection Status bit is set to ‘0’, no Program or Erase operations have been attempted to protected blocks since the last Clear Status Register command or hardware reset; when the Block Protection Status bit is set to ‘1’, a Program or Erase operation has been attempted on a protected block.

Once set to ‘1’, the Block Protection Status bit can only be reset Low by a Clear Status Register command or a hardware reset. If set to ‘1’ it should be reset before a new Program or Erase command is issued, otherwise the new command will appear to fail.

5.8 Bit 0

Reserved bit (set to ‘1’).

Table 13. Status Register bits

Bit	Name	Logic level	Definition
7	Program/Erase Controller Status	’1’	Ready
		’0’	Busy
6	Erase Suspend Status	’1’	Suspended
		’0’	In progress or completed
5	Erase Status	’1’	Erase error
		’0’	Erase success
4	Program Status,	’1’	Program error
		’0’	Program success
3	PEN Status bit	‘0’	No program or erase attempted
		‘1’	Program or erase attempted
2	Program Suspend Status	’1’	Suspended
		’0’	In progress or completed
1	Erase/Program in a protected block	’1’	Program/erase on protected block, abort
		’0’	No operations to protected blocks
0	Reserved	’1’	Reserved

6 Maximum rating

Stressing the device above the ratings listed in *Table 14: Absolute maximum ratings*, may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the Numonyx SURE Program and other relevant quality documents.

Table 14. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		Min	Max	
T_{BIAS}	Temperature under bias	–40	125	°C
T_{STG}	Storage temperature	–55	155	°C
V_{IO}	Input or output voltage	–0.6	V_{DDQ} + 0.6 V_{DDQIN} + 0.6	V
V_{DD}, V_{DDQ}, V_{DDQIN}	Supply voltage	–0.6	4.2	V

Table 15. Data retention

Power supply V_{DD}	Unit	External temperature		Unit
		25 °C	**125** °C	
0	V	20	7	Years
2.5	V	–	25	Years
2.7	V	–	15	Years

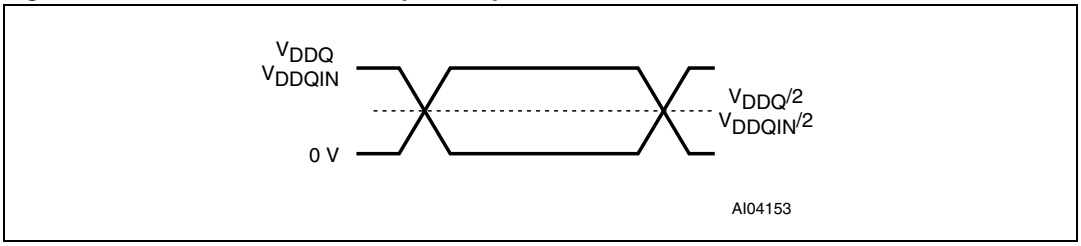
7 DC and AC parameters

This section summarizes the operating and measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC characteristics tables that follow, are derived from tests performed under the measurement conditions summarized in *Table 16: Operating and AC measurement conditions*. Designers should check that the operating conditions in their circuit match the measurement conditions when relying on the quoted parameters.

Table 16. Operating and AC measurement conditions

Parameter		M58BW16F, M58BW32F				Units
		45 ns		55 ns		
		Min	Max	Min	Max	
Supply voltage (V_{DD})		2.7	3.6	2.5	3.3	V
Input/output supply voltage (V_{DDQ})		2.4	3.6	2.4	3.6	V
Ambient temperature (T_A)	Grade 3	–40	125	–40	125	°C
Load capacitance (C_L)		30		30		pF
Clock rise and fall times			3		3	ns
Input rise and fall times			3		3	ns
Input pulses voltages		0 to V_{DDQ}		0 to V_{DDQ}		V
Input and output timing ref. voltages		$V_{DDQ}/2$		$V_{DDQ}/2$		V

Figure 5. AC measurement input/output waveform



1. $V_{DD} = V_{DDQ}$.

Figure 6. AC measurement load circuit

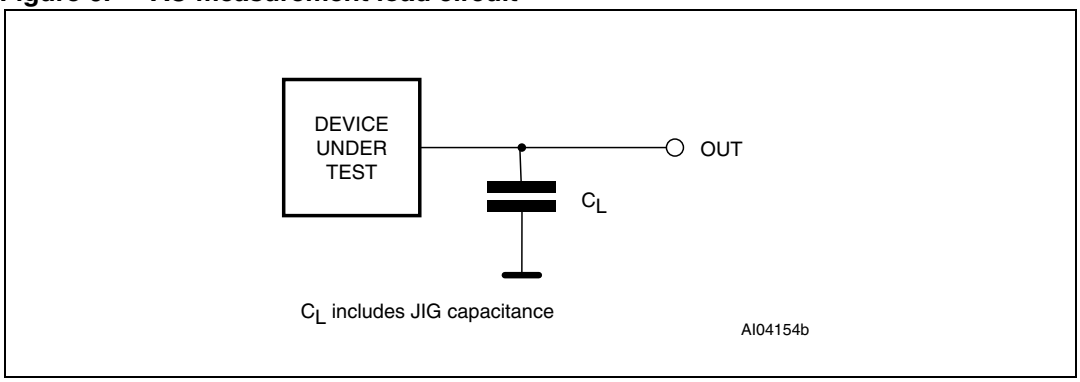


Table 17. Device capacitance(1)(2)

Symbol	Parameter	Test condition	Typ	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V	6	8	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V	8	12	pF

1. T_A = 25 °C, f = 1 MHz.
2. Sampled only, not 100% tested.

Table 18. DC characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
I_{LI}	Input Leakage current	0 V≤V_{IN} ≤V_{DDQIN}			±1	µA
I_{LO}	Output Leakage current	0 V ≤V_{OUT} ≤V_{DDQ}			±5	µA
I_{DD}	Supply current (Random Read)	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IH}, f_{add} = 6 MHz			25	mA
I_{DDP-UP}(1)	Supply current (power-up)				20	mA
I_{DDB}	Supply current (Burst Read)	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IH}, f_{clock} = 75 MHz			50	mA
I_{DD1}(2)	Supply current (Standby)	$\overline{E}$ = $\overline{RP}$ = V_{DD} ± 0.2 V			150	µA
I_{DD2}	Supply current (Program or Erase)	Program, Erase in progress			30	mA
I_{DD3}	Supply current (Erase/Program Suspend)	$\overline{E}$ = V_{IH}			150	µA
I_{DD4}	Supply current (Standby Disable)			5	10	mA
V_{IL}	Input Low voltage		–0.5		0.2V_{DDQIN}	V
V_{IH}	Input High voltage (for DQ lines)		0.8V_{DDQIN}		V_{DDQ} + 0.3	V
V_{IH}	Input High voltage (for input only lines)		0.8V_{DDQIN}		3.6	V
V_{OL}	Output Low voltage	I_{OL} = 100 µA			0.1	V
V_{OH}	Output High voltage CMOS	I_{OH} = –100 µA	V_{DDQ} –0.1			V
V_{LKO}	V_{DD} supply voltage (Erase and Program lockout)				2.2	V

1. I_{DDP-UP} is the current needed from the device until $\overline{RP}$ goes to its logic high level when the power supply is stable (t_{VDHPH}). See *Figure 22*and *Figure 23*.
2. The Standby mode can be disabled by setting the Standby Disable bit (M14) of the Burst Configuration Register to ‘1’.

Figure 7. Asynchronous Bus Read AC waveforms

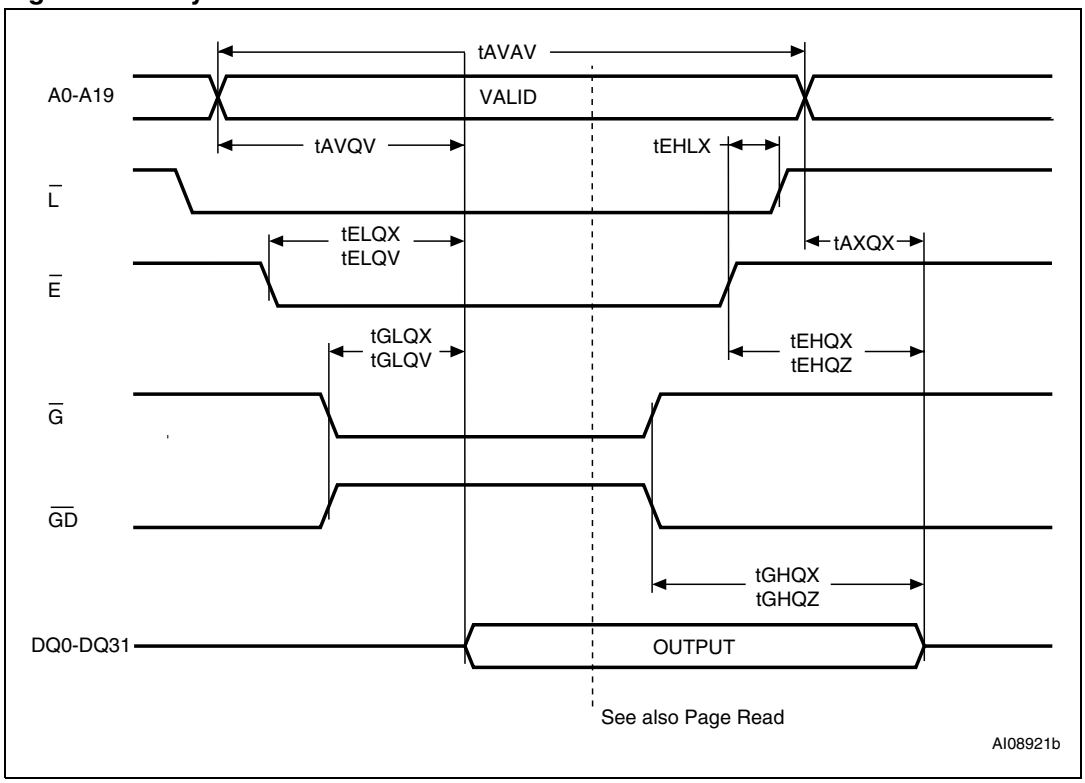


Figure 8. Asynchronous Latch Controlled Bus Read AC waveforms

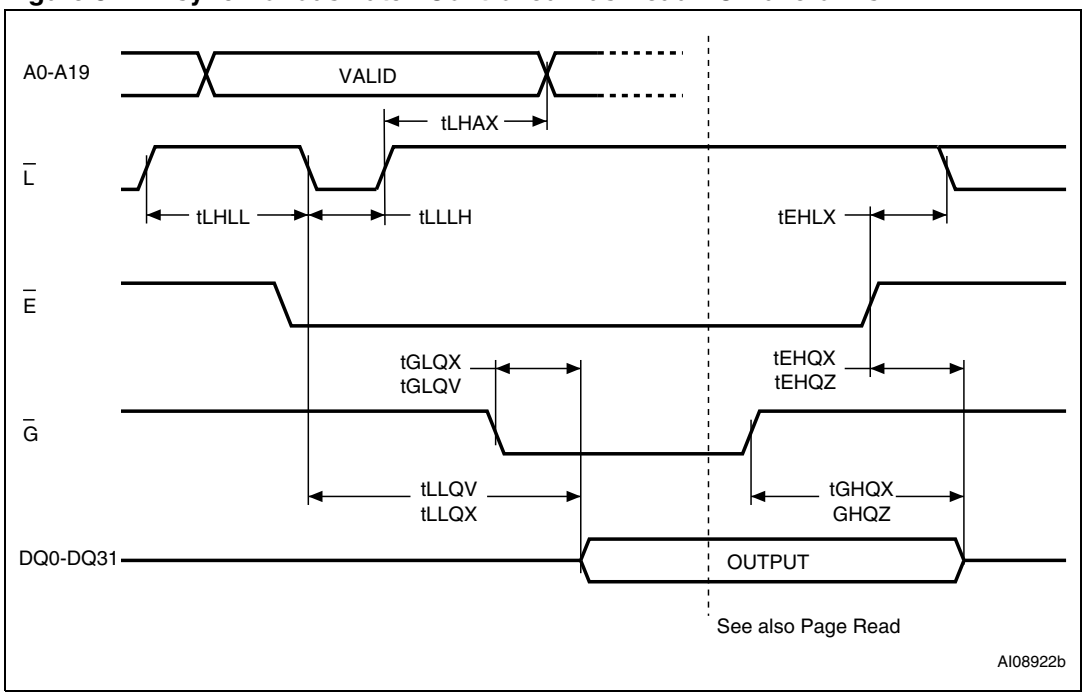


Figure 9. Asynchronous Chip Enable Controlled Bus Read AC waveforms

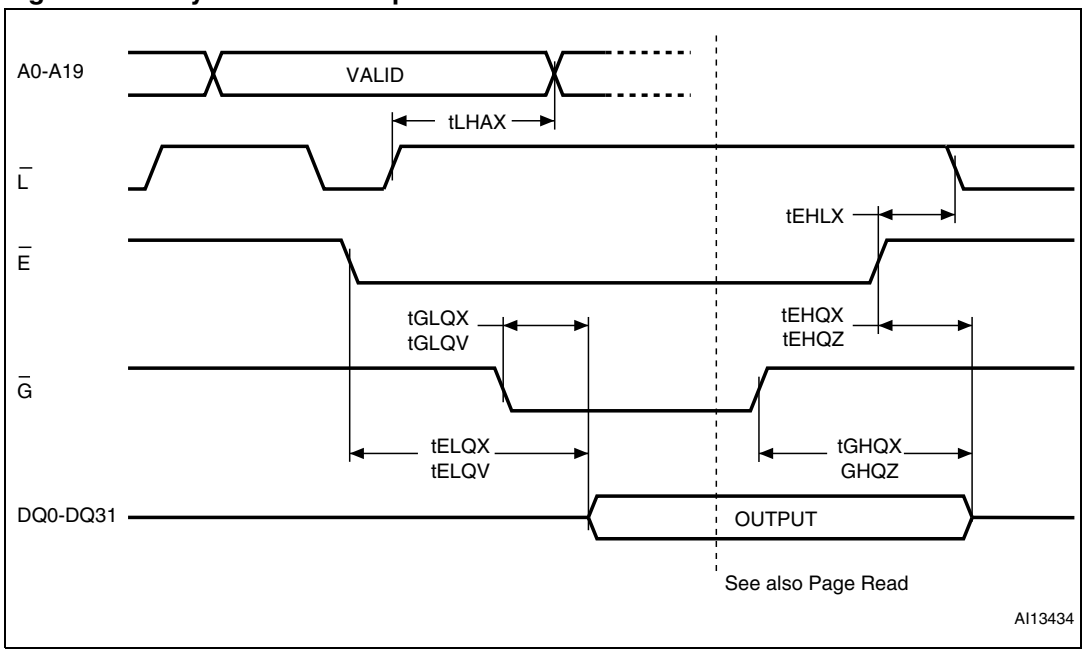


Figure 10. Asynchronous Address Controlled Bus Read AC waveforms

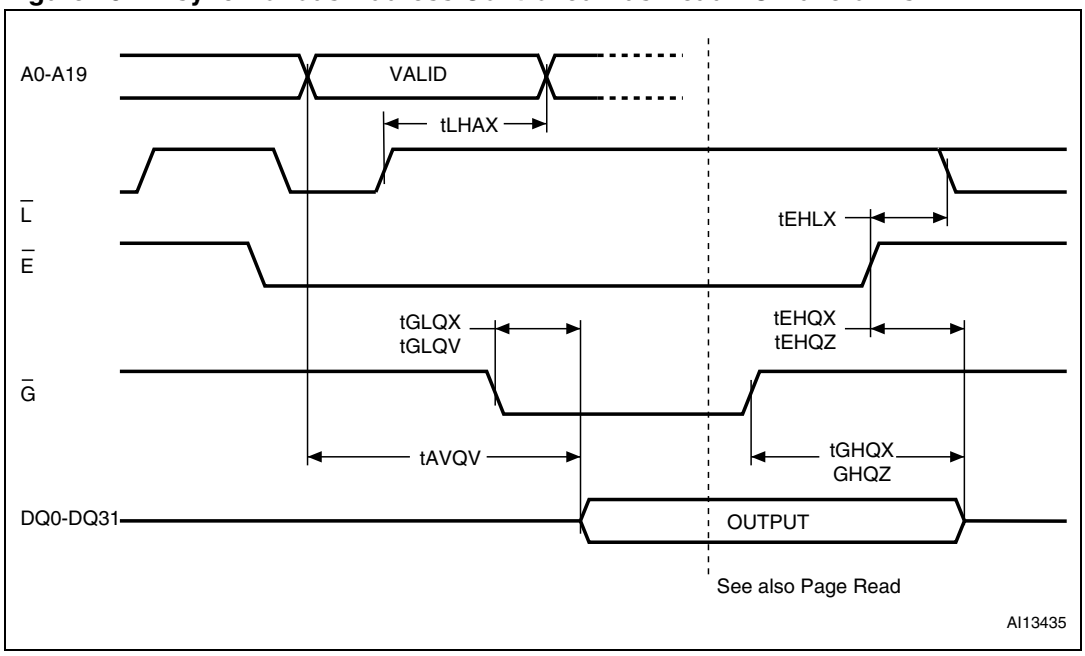


Table 19. Asynchronous Bus Read AC characteristics

Symbol	Parameter	Test condition		M58BWxxF		Unit
				45	55	
t_{AVAV}	Address Valid to Address Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	Min	45	55	ns
t_{AVQV}	Address Valid to Output Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	Max	45	55	ns
t_{AXQX}	Address Transition to Output Transition	$\overline{L} = V_{IL}$, $\overline{G} = V_{IL}$	Min	0	0	ns
t_{EHLX}	Chip Enable High to Latch Enable Transition		Min	0	0	ns
t_{EHQX}	Chip Enable High to Output Transition	$\overline{G} = V_{IL}$	Min	0	0	ns
t_{EHQZ}	Chip Enable High to Output Hi-Z	$\overline{G} = V_{IL}$	Max	20	20	ns
t_{ELQV}(1)	Chip Enable Low to Output Valid	$\overline{G} = V_{IL}$	Max	45	55	ns
t_{GHQX}	Output Enable High to Output Transition	$\overline{E} = V_{IL}$	Min	0	0	ns
t_{GHQZ}	Output Enable High to Output Hi-Z	$\overline{E} = V_{IL}$	Max	15	15	ns
t_{GLQV}	Output Enable Low to Output Valid	$\overline{E} = V_{IL}$	Max	15	15	ns
t_{GLQX}	Output Enable Low to Output Transition	$\overline{E} = V_{IL}$	Min	0	0	ns
t_{LHAX}	Latch Enable High to Address Transition	$\overline{E} = V_{IL}$	Min	5	5	ns
t_{LHLL}	Latch Enable High to Latch Enable Low		Min	10	10	ns
t_{LLLH}	Latch Enable Low to Latch Enable High	$\overline{E} = V_{IL}$	Min	10	10	ns
t_{LLQV}	Latch Enable Low to Output Valid Chip Enable Low to Output Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	Max	45	55	ns
t_{LLQX}	Latch Enable Low to Output Transition	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	Min	0	0	ns
t_{ELQX}	Chip Enable Low to Output Transition	$\overline{L} = V_{IL}$, $\overline{G} = V_{IL}$	Min	0	0	ns

1. Output Enable $\overline{G}$ may be delayed up to $t_{ELQV} - t_{GLQV}$ after the falling edge of Chip Enable $\overline{E}$ without increasing t_{ELQV}.

Figure 11. Asynchronous Page Read AC waveforms

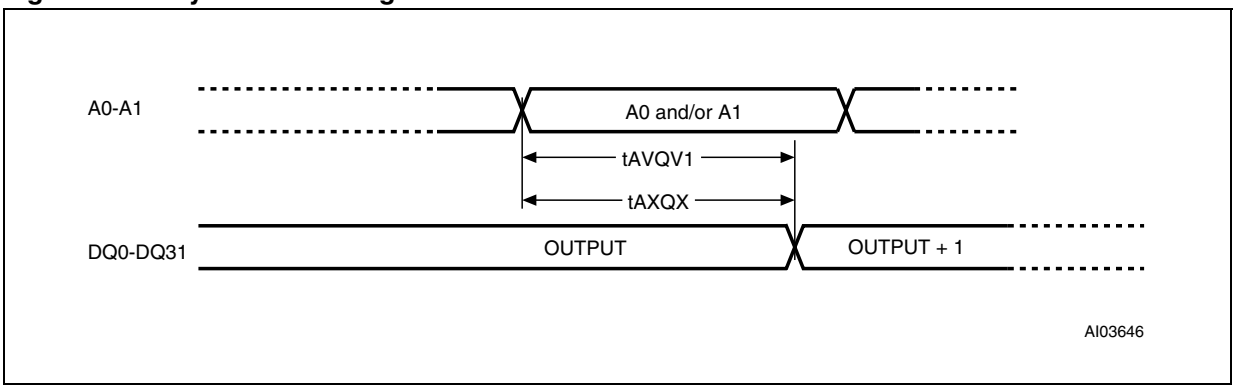


Table 20. Asynchronous Page Read AC characteristics(1)

Symbol	Parameter	Test condition		M58BWxxF		Unit
				45	55	
t_{AVQV1}	Address Valid to Output Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	Max	25	25	ns
t_{AXQX}	Address Transition to Output Transition	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	Min	0	0	ns

1. For other timings see *Table 19: Asynchronous Bus Read AC characteristics*.

Figure 12. Asynchronous Write AC waveforms

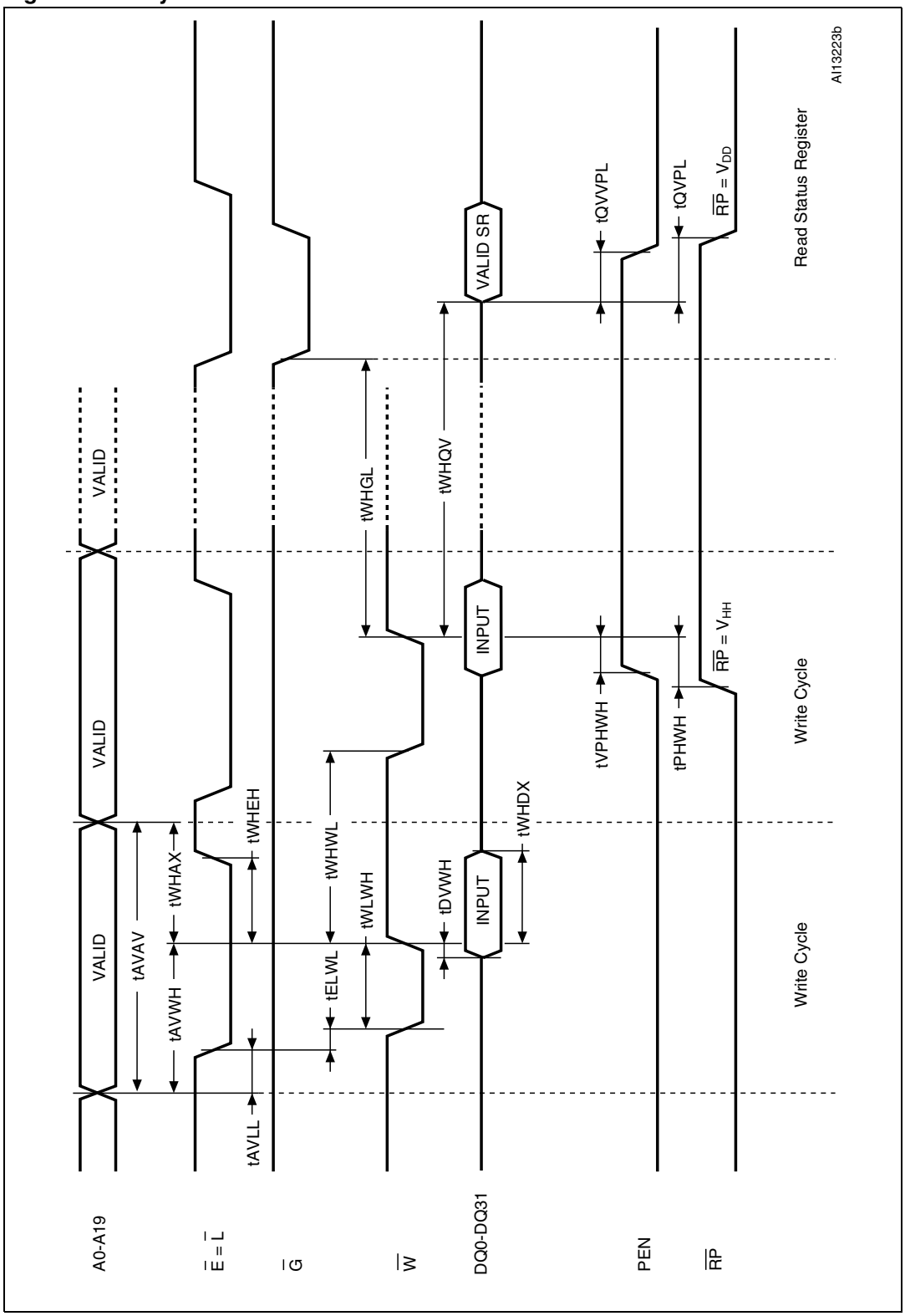


Figure 13. Asynchronous Latch controlled Write AC waveforms

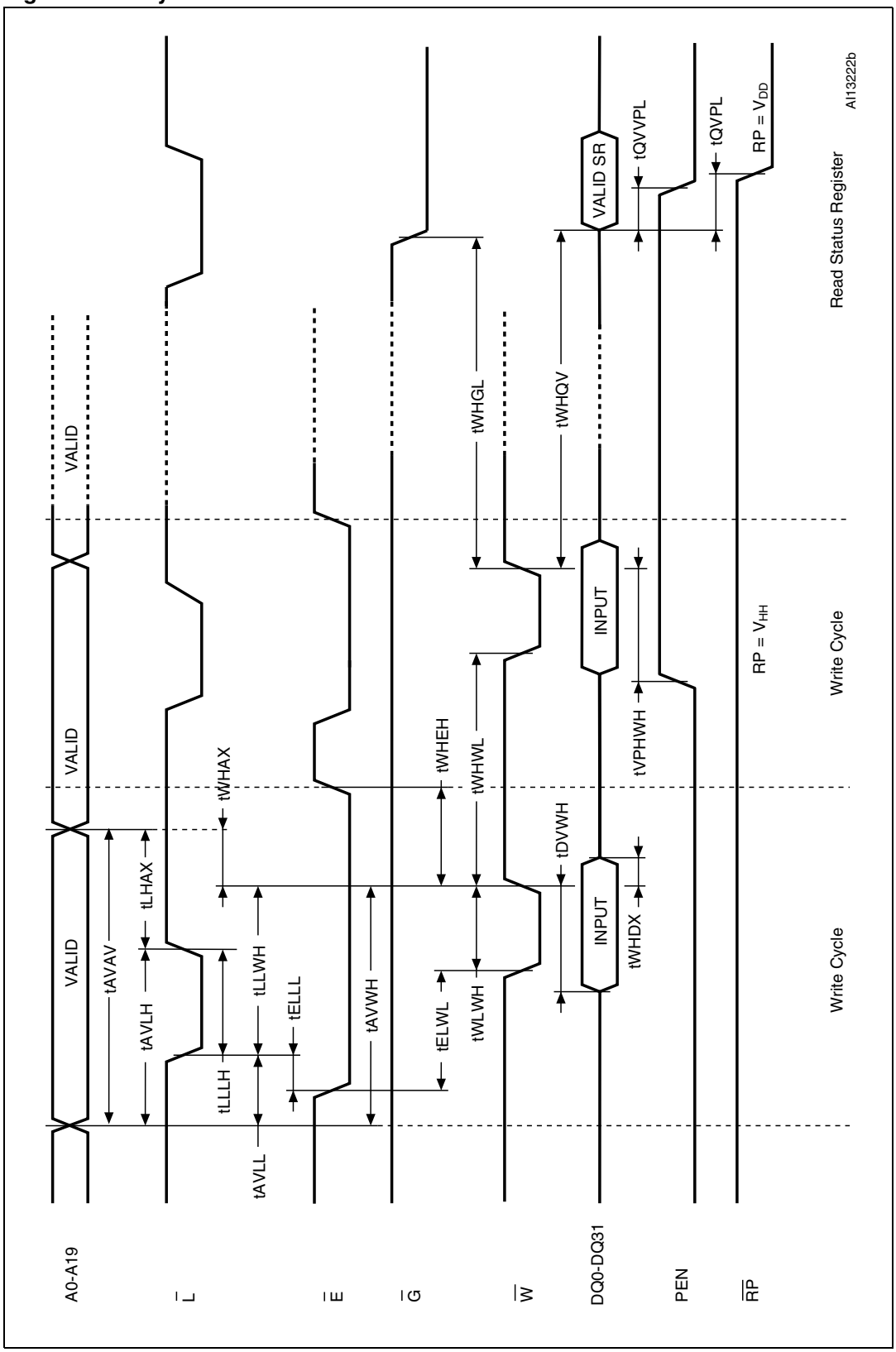


Table 21. Asynchronous Write and Latch controlled Write AC characteristics

Symbol	Parameter	Test condition		M58BWxxF		Unit
				45	55	
t_{AVAV}	Address Valid to Address Valid		Min	45	55	ns
t_{AVLH}	Address Valid to Latch Enable High		Min	8	8	ns
t_{AVLL}	Address Valid to Latch Enable Low		Min	0	0	ns
t_{AVWH}	Address Valid to Write Enable High	$\overline{E} = V_{IL}$	Min	25	30	ns
t_{DVWH}	Data Input Valid to Write Enable High	$\overline{E} = V_{IL}$	Min	25	30	ns
t_{ELLL}	Chip Enable Low to Latch Enable Low		Min	0	0	ns
t_{ELWL}	Chip Enable Low to Write Enable Low		Min	0	0	ns
t_{LHAX}	Latch Enable High to Address Transition		Min	5	5	ns
t_{LLLH}	Latch Enable Low to Latch Enable High		Min	10	10	ns
t_{LLWH}	latch Enable Low to Write Enable High	$\overline{E} = V_{IL}$	Min	25	30	ns
t_{QVVPL}	Output Valid to PEN Low		Min	0	0	ns
t_{VPHWH}	PEN High to Write Enable High		Min	0	0	ns
t_{WHAX}	Write Enable High to Address Transition	$\overline{E} = V_{IL}$	Min	0	0	ns
t_{WHDX}	Write Enable High to Input Transition	$\overline{E} = V_{IL}$	Min	0	0	ns
t_{WHEH}	Write Enable High to Chip Enable High		Min	0	0	ns
t_{WHGL}	Write Enable High to Output Enable Low		Min	150	150	ns
t_{WHQV}	Write Enable High to Output Valid		Min	165	165	ns
t_{WHWL}	Write Enable High to Write Enable Low		Min	20	20	ns
t_{WLWH}	Write Enable Low to Write Enable High	$\overline{E} = V_{IL}$	Min	25	30	ns
t_{QVPL}	Output Valid to Reset/Power-down Low		Min	0	0	ns

Figure 14. Synchronous Burst Read, Latch Enable controlled (data valid from 'n' clock rising edge)

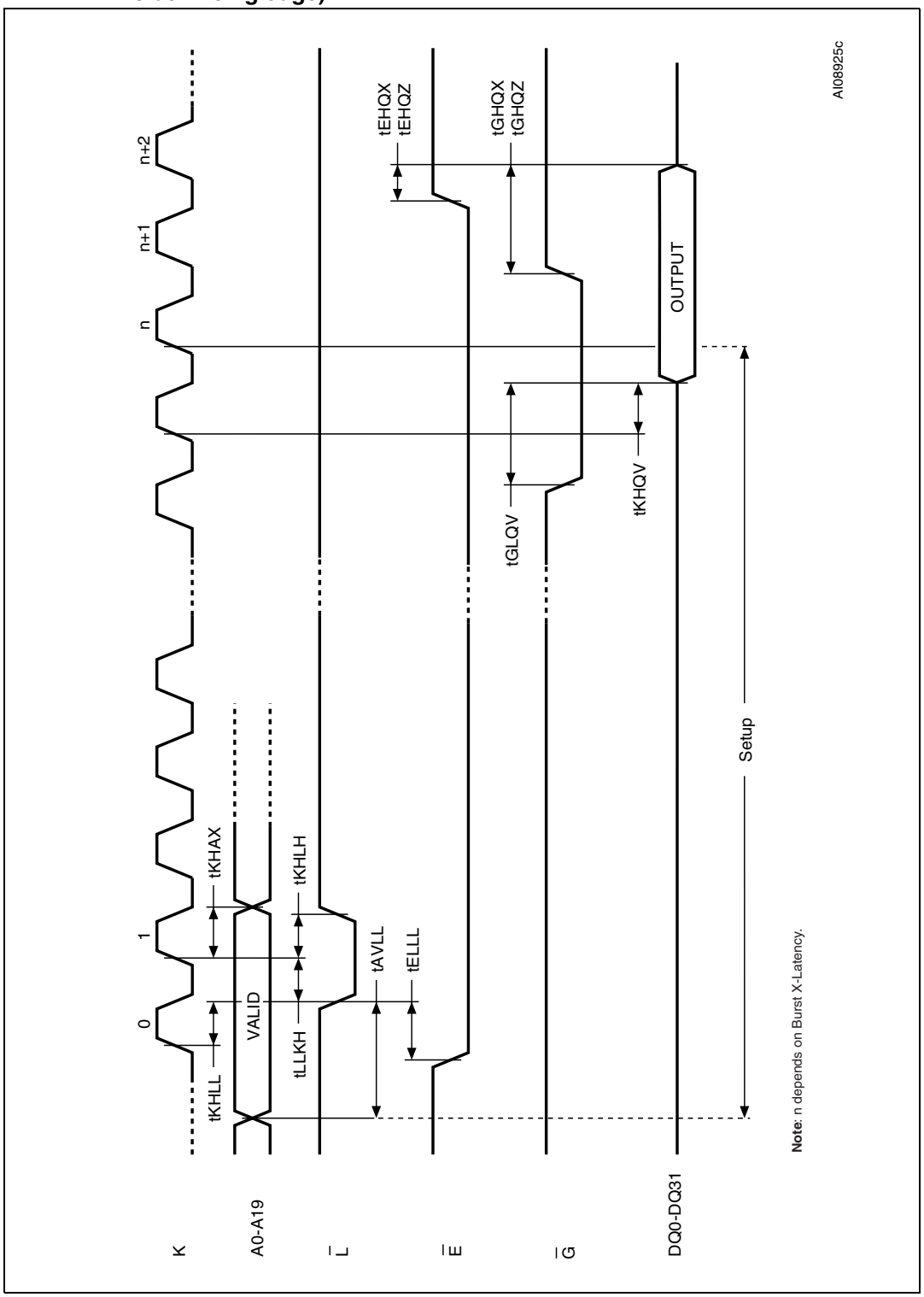


Figure 15. Synchronous Burst Read, Chip Enable controlled (data valid from 'n' clock rising edge)

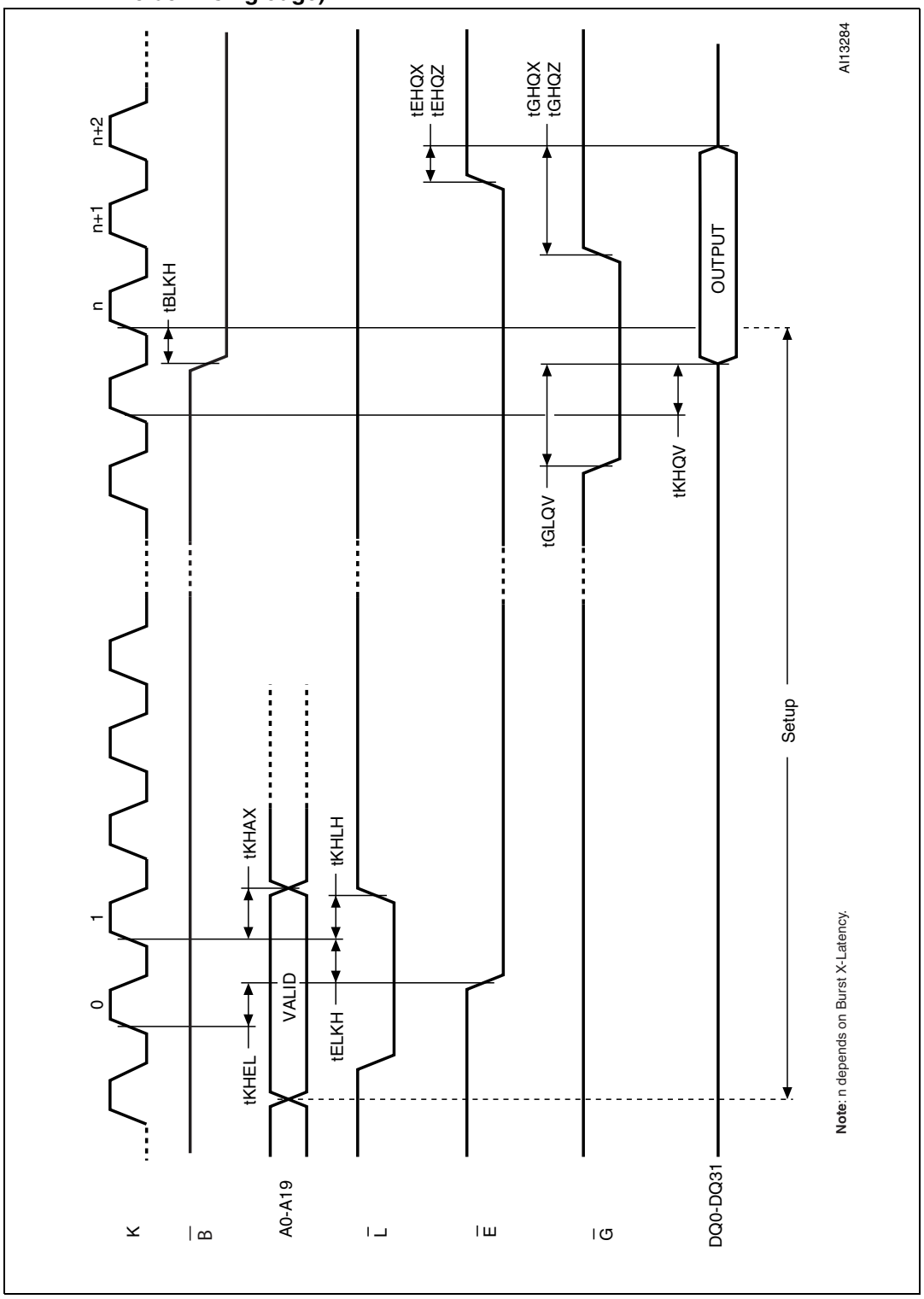


Figure 16. Synchronous Burst Read, Valid Address transition controlled (data valid from 'n' clock rising edge)

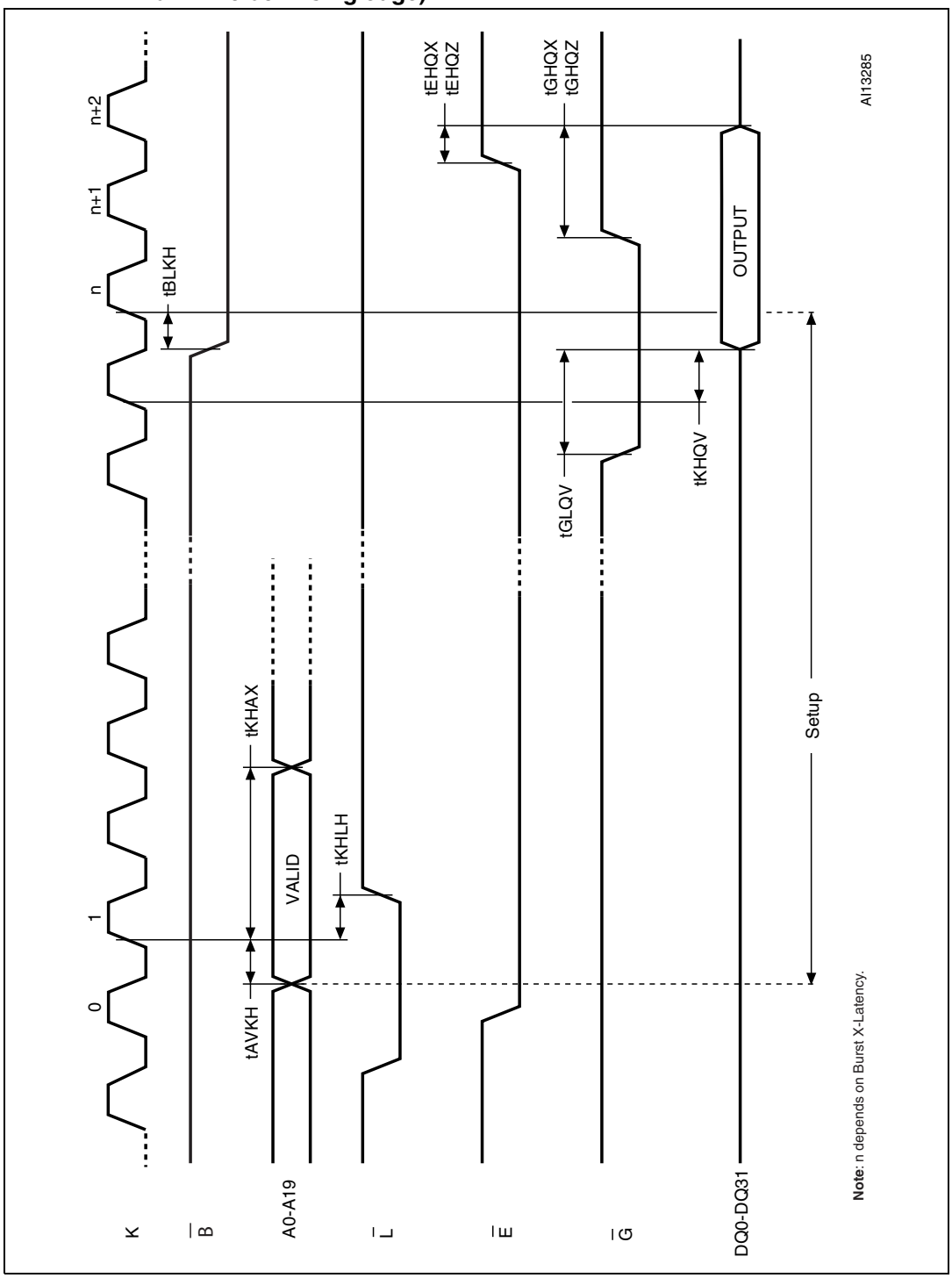
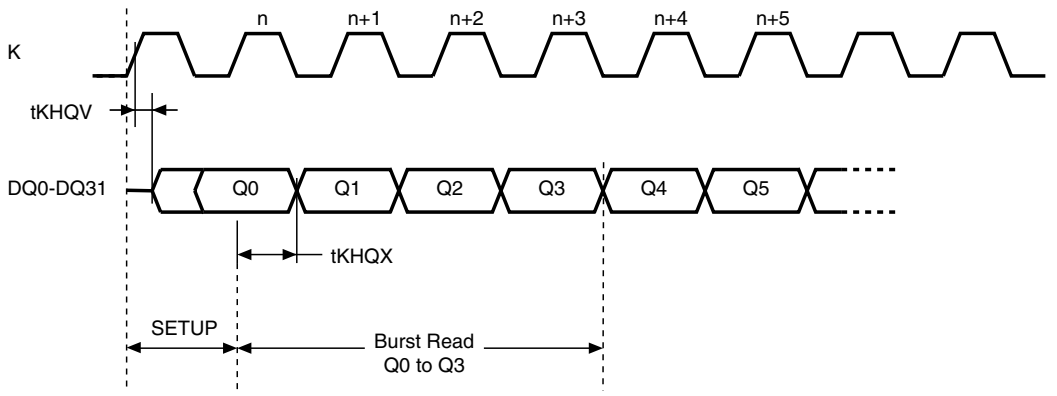
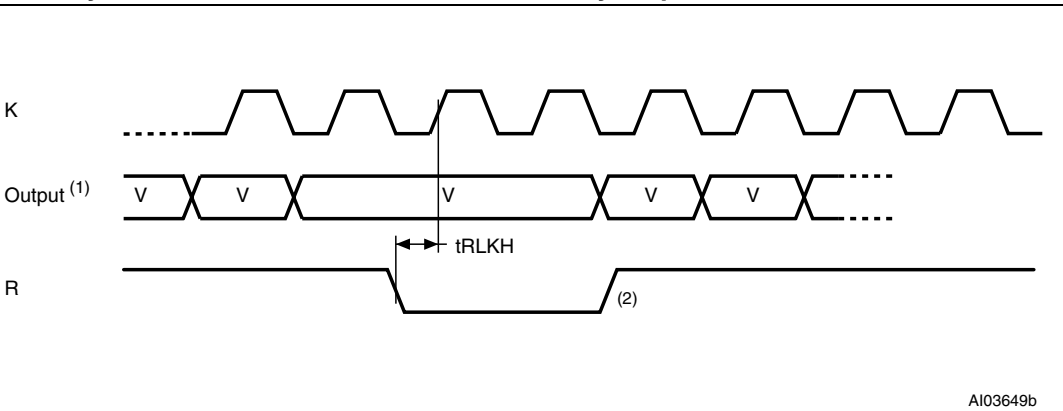


Figure 17. Synchronous Burst Read (data valid from 'n' clock rising edge)



1. For set up signals and timings see Synchronous Burst Read.

Figure 18. Synchronous Burst Read - valid data ready output



1. Valid Data Ready = Valid Low during valid clock edge.
2. V= Valid output.
3. The internal timing of R follows DQ.

Figure 19. Synchronous Burst Read - Burst Address Advance

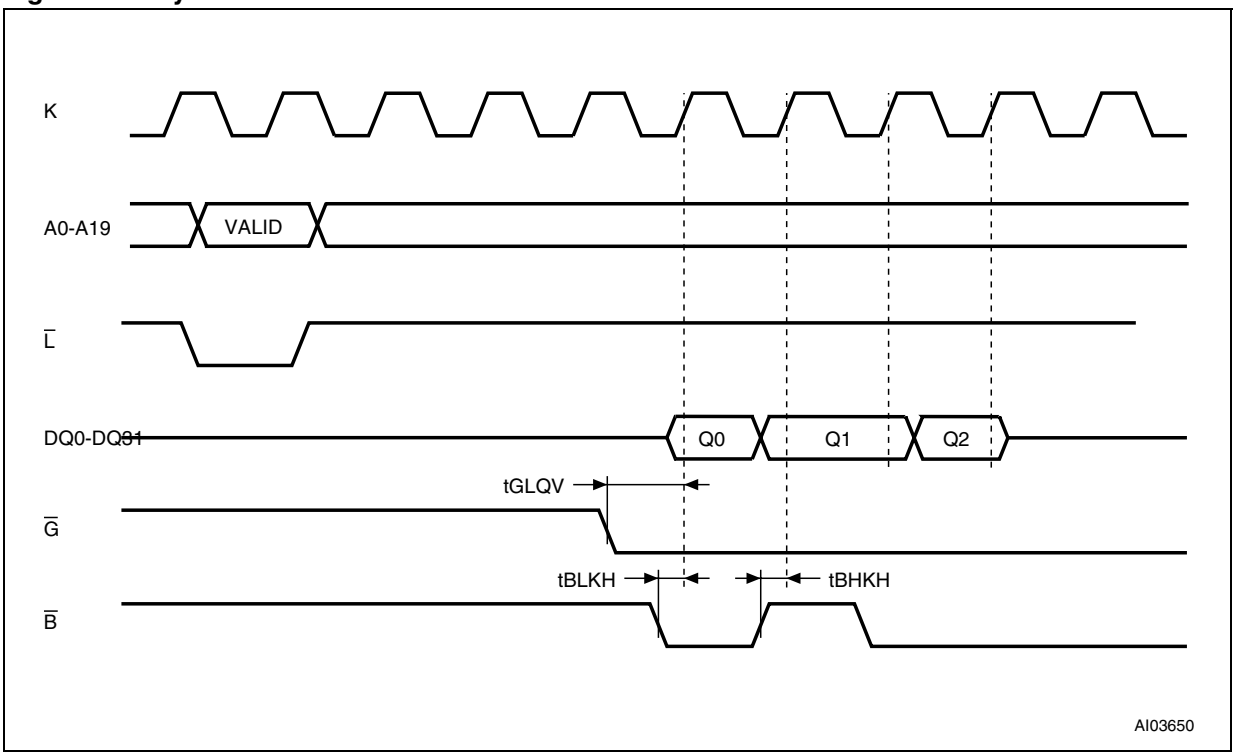


Figure 20. Clock input AC waveform

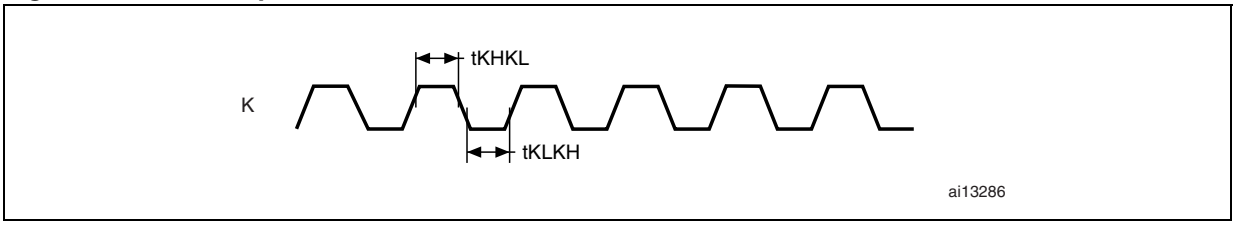
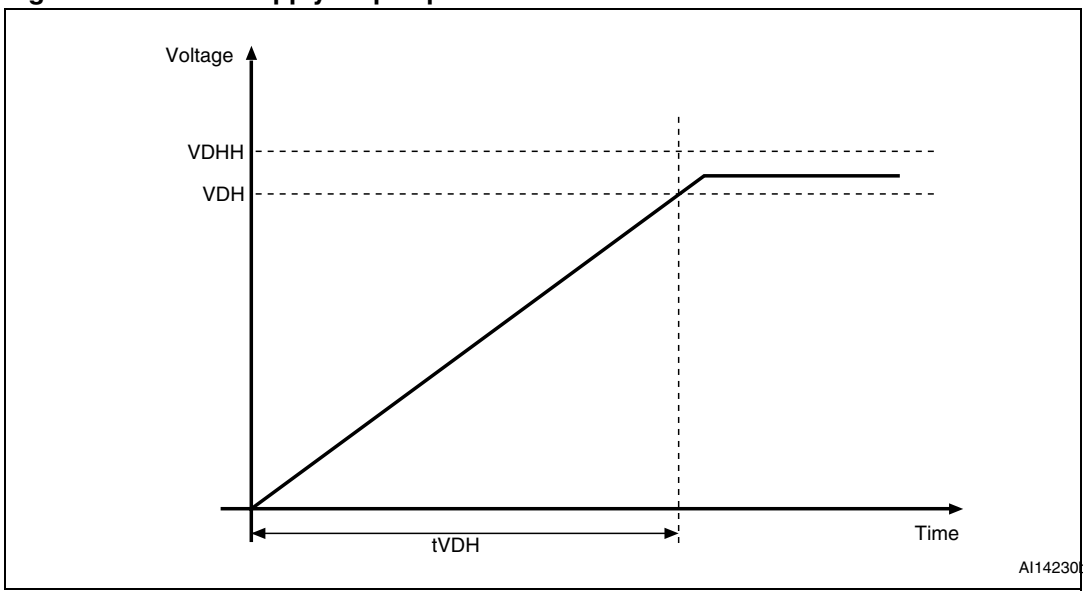


Table 22. Synchronous Burst Read AC characteristics(1)(2)

Symbol	Parameter	Test condition			M58BWxxF		Unit
					45	55	
f	Clock frequency	X-Latency = 3		Max	40	33	MHz
		X-Latency = 4		Max	56	40	MHz
		X-Latency = 5 or 6		Max	75	56	MHz
t_{AVKH}	Address Valid to Valid Clock Edge	$\overline{E} = V_{IL}$, $\overline{L} = V_{IL}$ X-Latency = 3		Min	12	13	ns
		$\overline{E} = V_{IL}$, $\overline{L} = V_{IL}$ X-Latency = 4, 5 or 6		Min	6	7	ns
t_{KHKL}	Clock High time			Min	6	6	ns
t_{KLKH}	Clock Low time			Min	6	6	ns
t_{BHKH}	Burst Address Advance High to Valid Clock Edge	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$, $\overline{L} = V_{IH}$		Min	8	8	ns
t_{BLKH}	Burst Address Advance Low to Valid Clock Edge	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$, $\overline{L} = V_{IH}$		Min	8	8	ns
t_{ELKH}	Chip Enable Low to Valid Clock Edge	$\overline{L} = V_{IL}$ X-Latency = 3		Min	12	13	ns
		$\overline{L} = V_{IL}$ X-Latency = 4, 5 or 6		Min	6	7	ns
t_{GLQV}	Output Enable Low to Output Valid	$\overline{E} = V_{IL}$, $\overline{L} = V_{IH}$		Max	15	15	ns
t_{KHAX}	Valid Clock Edge to Address Transition	$\overline{E} = V_{IL}$		Min	5	5	ns
t_{KHEL}	Valid Clock Edge to Chip Enable Low	$\overline{L} = V_{IL}$		Min	0	0	ns
t_{KHLL}	Valid Clock Edge to Latch Enable Low	$\overline{E} = V_{IL}$		Min	0	0	ns
t_{KHLH}	Valid Clock Edge to Latch Enable High	$\overline{E} = V_{IL}$		Min	0	0	ns
t_{KHQX}	Valid Clock Edge to Output Transition	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$, $\overline{L} = V_{IH}$		Min	2	2	ns
t_{LLKH}	Latch Enable Low to Valid Clock Edge	$\overline{E} = V_{IL}$ X-Latency = 3		Min	12	13	ns
		$\overline{E} = V_{IL}$ X-Latency = 4, 5 or 6	M58BW16F	Min	6	5	ns
			M58BW32F	Min	6	7	ns
t_{RLKH}	Valid Data Ready Low to Valid Clock Edge	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$, $\overline{L} = V_{IH}$		Min	6	6	ns
t_{KHQV}	Valid Clock Edge to Output Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$, $\overline{L} = V_{IH}$		Max	8	8	ns

1. Data output should be read on the valid clock edge.
2. For other timings see *Table 19: Asynchronous Bus Read AC characteristics*.

Figure 21. Power supply slope specification



1. Please refer to the application note AN2601.

Table 23. Power supply AC and DC characteristics

Symbol	Description	Min	Max	Unit
V_{DH}	Minimum value of power supply (V_{DD})(1)	$0.9V_{DD}$		V
V_{DHH}	Maximum value of power supply (V_{DD})		3.6	V
t_{VDH}	Time required from power supply to reach the V_{DH} value	300	50000	µs

1. This threshold is 90% of the minimum value allowed to V_{DD}.

Figure 22. Reset, Power-down and Power-up AC waveforms - Control pins Low

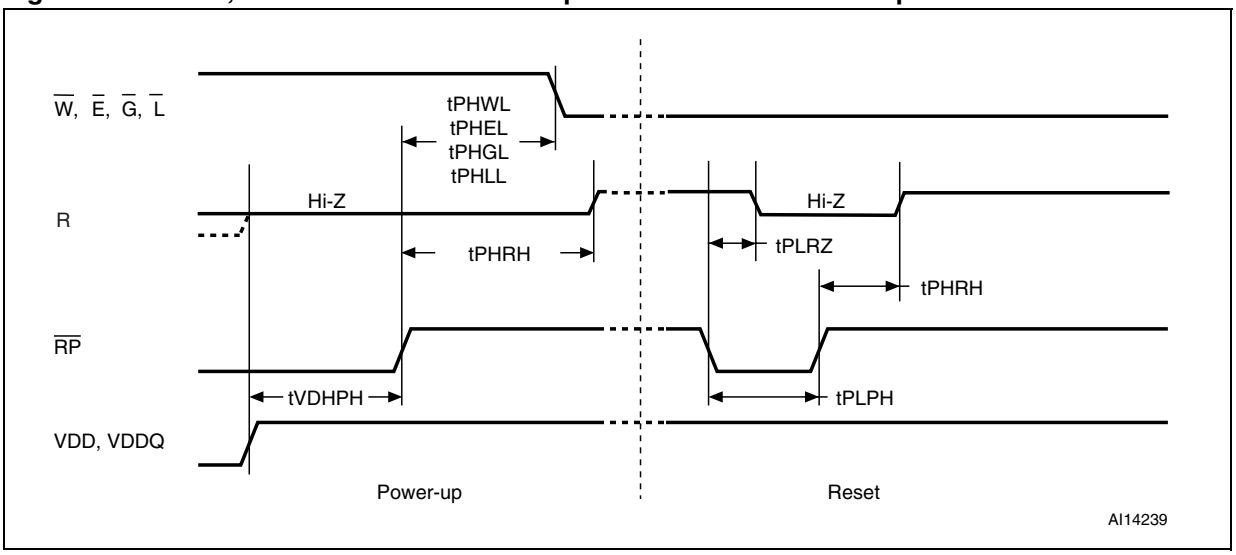


Figure 23. Reset, Power-down and Power-up AC waveforms - Control pins toggling

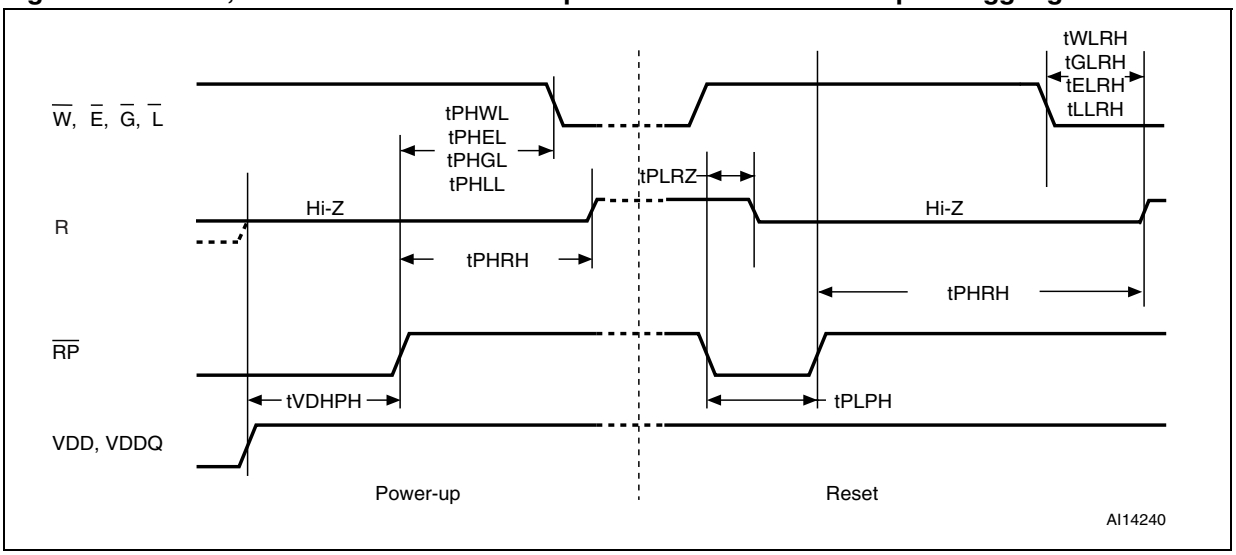


Table 24. Reset, Power-down and Power-up AC characteristics

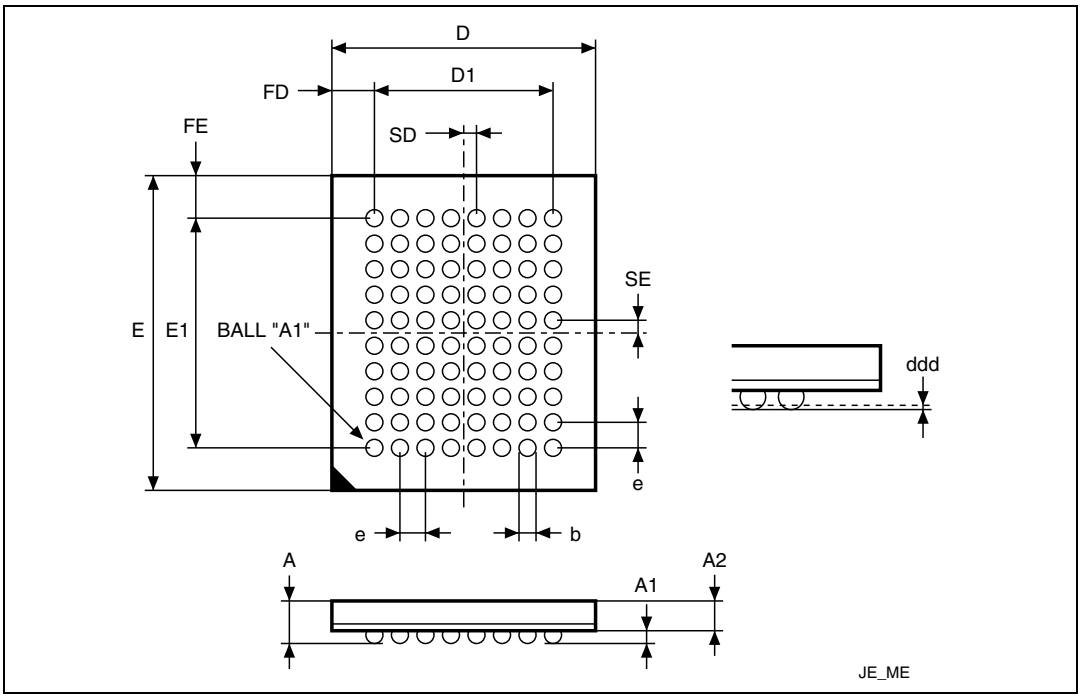
Symbol	Parameter	Min	Max	Unit
t_{PHEL}	Reset/Power-down High to Chip Enable Low	50		ns
t_{PHLL}	Reset/Power-down High to Latch Enable Low	50		ns
t_{PHQV}(1)	Reset/Power-down High to Output Valid		95	ns
t_{PHWL}	Reset/Power-down High to Write Enable Low	50		ns
t_{PHGL}	Reset/Power-down High to Output Enable Low	50		ns
t_{PLPH}	Reset/Power-down Low to Reset/Power-down High	100		ns
t_{PHRH}(1)	Reset/Power-down High to Valid Data Ready High		95	ns
t_{VDHPH}	Supply voltages High to Reset/Power-down High	50		µs
t_{PLRZ}	Reset/Power-down Low to Data Ready High Impedance		80	ns
t_{WLRH}	Write Enable Low to Data Ready High Impedance		80	ns
t_{GLRH}	Output Enable Low to Data Ready High Impedance		80	ns
t_{ELRH}	Chip Enable Low to Data Ready High Impedance		80	ns
t_{LLRH}	Latch Enable Low to Data Ready High Impedance		80	ns

1. This time is $t_{PHEL} + t_{AVQV}$ or $t_{PHEL} + t_{ELQV}$.

8 Package mechanical

In order to meet environmental requirements, Numonyx offers these devices in ECOPACK® packages. ECOPACK® packages are lead-free. The category of second-level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label.

Figure 24. LBGA80 10 × 12 mm - 8 × 10 ball array, 1 mm pitch, bottom view package outline

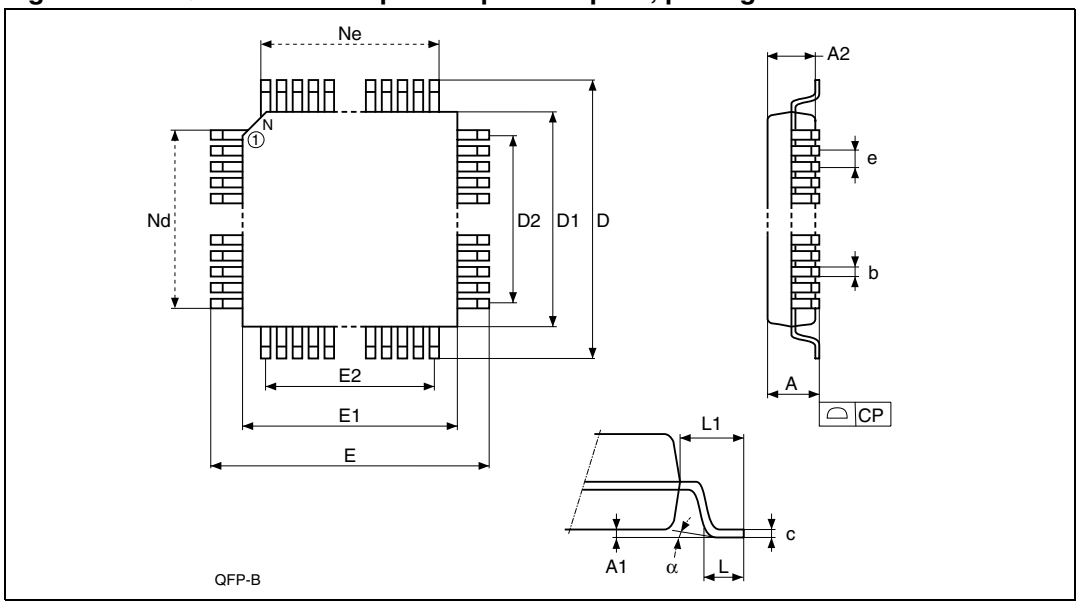


1. Drawing is not to scale.

Table 25. LBGA80 10 × 12 mm - 8 × 10 active ball array, 1 mm pitch, package mechanical data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.60			0.063
A1		0.40			0.016	
A2			1.05			0.041
b	0.60			0.024		
D	10.00	–	–	0.394	–	–
D1	7.00	–	–	0.276	–	–
ddd			0.15			0.006
E	12.00	–	–	0.472	–	–
E1	9.00	–	–	0.354	–	–
e	1.00	–	–	0.039	–	–
FD	1.50	–	–	0.059	–	–
FE	1.50	–	–	0.059	–	–
SD	0.50			0.020		
SE	0.50			0.020		

Figure 25. PQFP80 - 80 lead plastic quad flat pack, package outline



1. Drawing is not to scale.

Table 26. PQFP80 - 80 lead plastic quad flat pack, package mechanical data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A			3.40			0.134
A1		0.25			0.010	
A2	2.80	2.55	3.05	0.110	0.100	0.120
b		0.30	0.45		0.012	0.018
CP			0.10			0.004
c		0.13	0.23		0.005	0.009
D	23.20	22.95	23.45	0.913	0.903	0.923
D1	20.00	19.90	20.10	0.787	0.783	0.791
D2	18.40	–	–	0.724	–	–
e	0.80	–	–	0.031	–	–
E	17.20	16.95	17.45	0.677	0.667	0.687
E1	14.00	13.90	14.10	0.551	0.547	0.555
E2	12.00	–	–	0.472	–	–
L	0.80	0.65	0.95	0.031	0.026	0.037
L1	1.60	–	–	0.063	–	–
α		0°	7°		0°	7°
N	80			80		
Nd	24			24		
Ne	16			16		

9 Ordering information

Table 27. Ordering information scheme

Example: M58BW32F T 4 T 3 T

Device type

M58

Architecture

B = Burst mode

Operating voltage

W = [2.7 V to 3.6 V] V_{DD} range for 45 ns speed class
[2.5 V to 3.3 V] V_{DD} range for 55 ns speed class
[2.4 V to V_{DD}] V_{DDQ} range for 45 ns and 55 ns speed classes

Device function

32F = 32 Mbit (x 32), boot block, burst, 0.11 µm technology
16F = 16 Mbit (x 32), boot block, burst, 0.11 µm technology

Array matrix

T = Top boot
B = Bottom boot

Speed

4 = 45 ns
5 = 55 ns

Package

T = PQFP80
ZA = LBGA80, 1.0 mm pitch

Device grade

3 = Automotive grade certified(1), –40 to 125 °C

Option

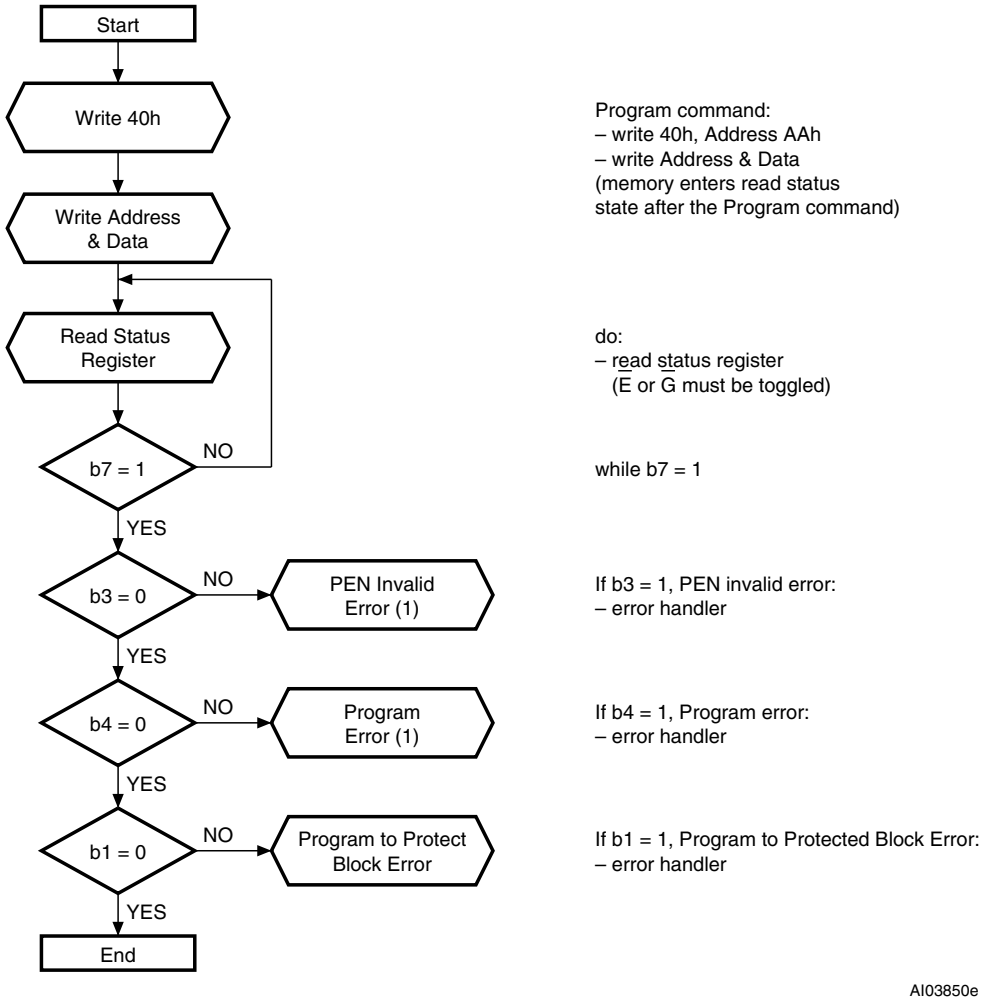
Blank = Standard packing
T = Tape & reel packing
F = ECOPACK® package, tape & reel 24 mm packing

1. Qualified & characterized according to AEC Q100 & Q003 or equivalent, advanced screening according to AEC Q001 & Q002 or equivalent.

Devices are shipped from the factory with the memory content bits erased to ’1’.
For a list of available options (speed, package, etc) or for further information on any aspect of this device, please contact the Numonyx Sales Office nearest to you.

Appendix A Flowcharts

Figure 26. Program flowchart and pseudocode



1. If an error is found, the Status Register must be cleared before further P/E operations.

Figure 27. Program Suspend & Resume flowchart and pseudocode

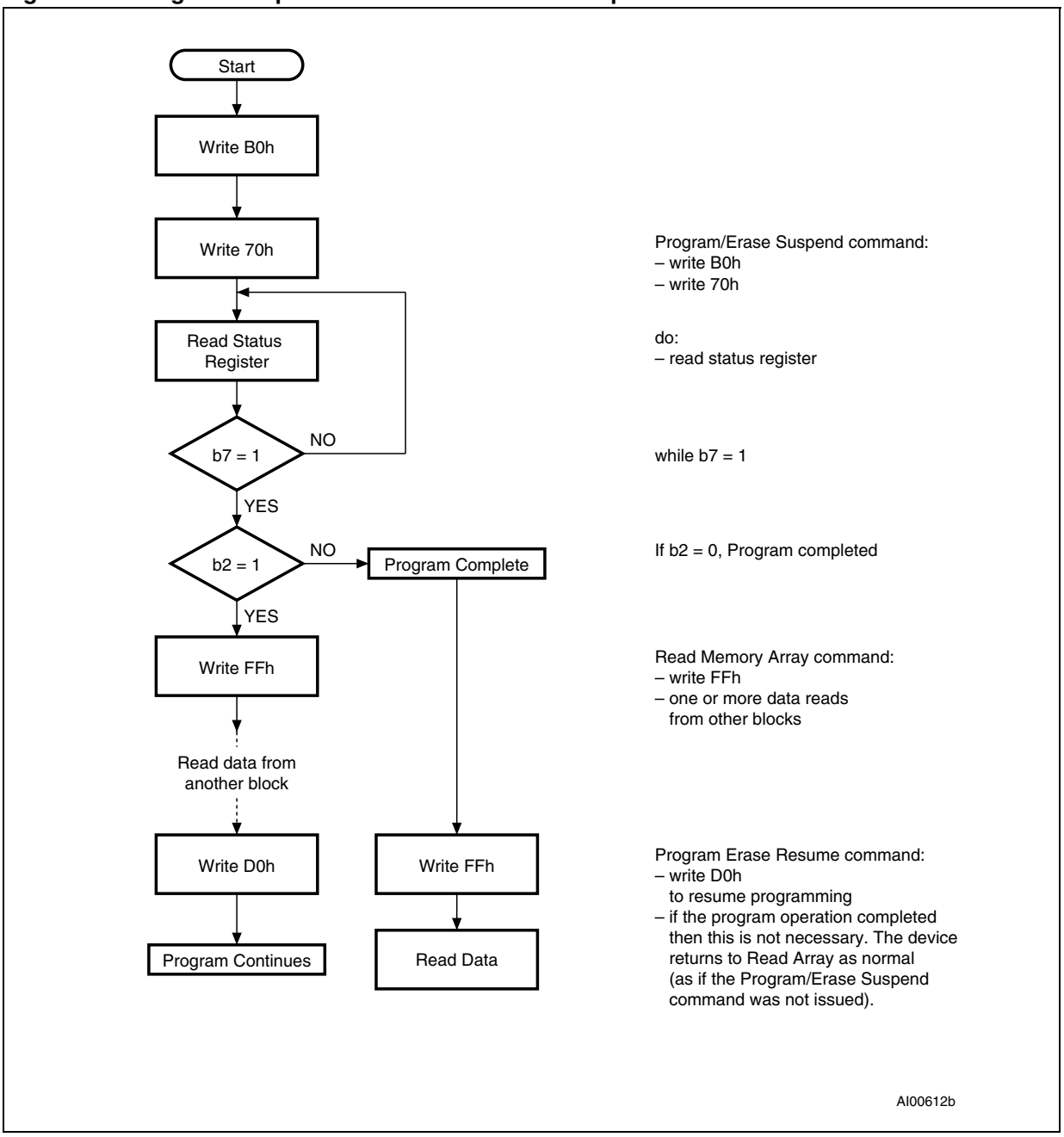
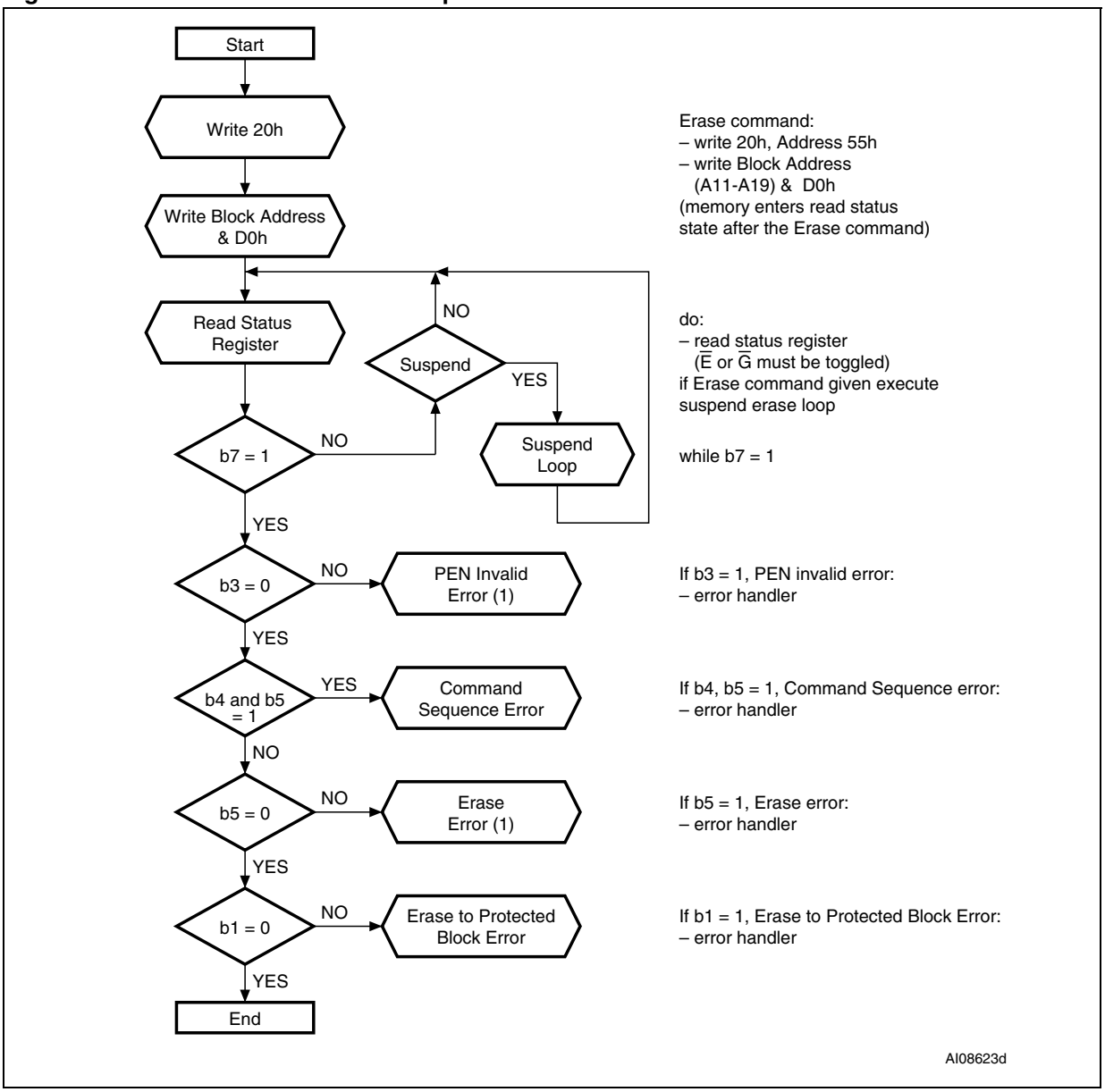
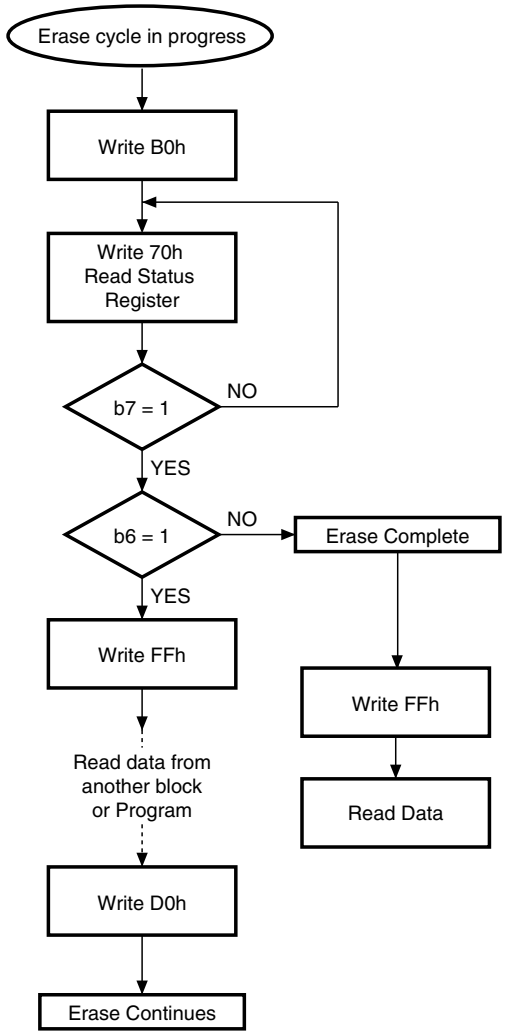


Figure 28. Block Erase flowchart and pseudocode



1. If an error is found, the Status Register must be cleared before further Program/Erase operations.

Figure 29. Erase Suspend & Resume flowchart and pseudocode



Program/Erase Suspend command

Do:
– Read status register while b7 = 1
(b7 = Program/Erase status bit)

If b6 = 0, Erase is completed
(b6 = Erase Suspend status bit)

The device returns to Read mode as normal
(as if the Program/Erase Suspend was not issued).

Read Memory Array command:
– Write FFh
– One or more data reads
from other blocks

Program/Erase Resume command:
– Write D0h to resume the Erase
operation

AI00615c

Figure 30. Power-up sequence followed by Synchronous Burst Read

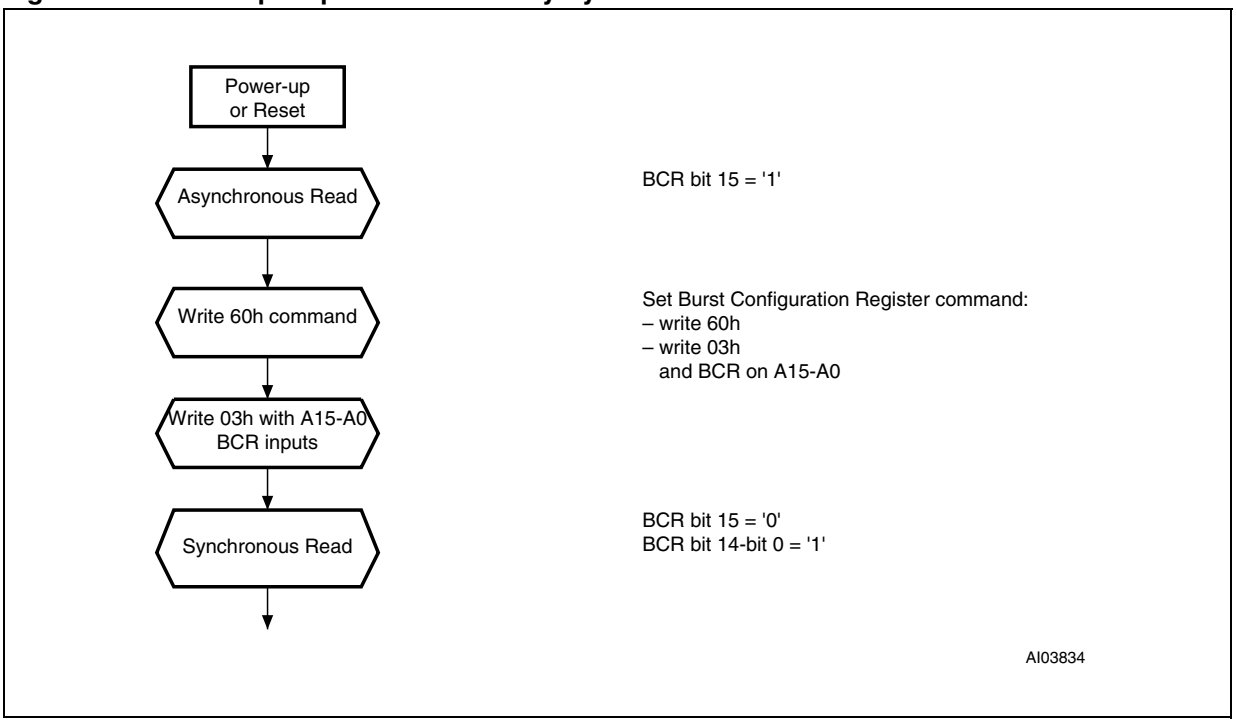


Figure 31. Command interface and Program/Erase controller flowchart (a)

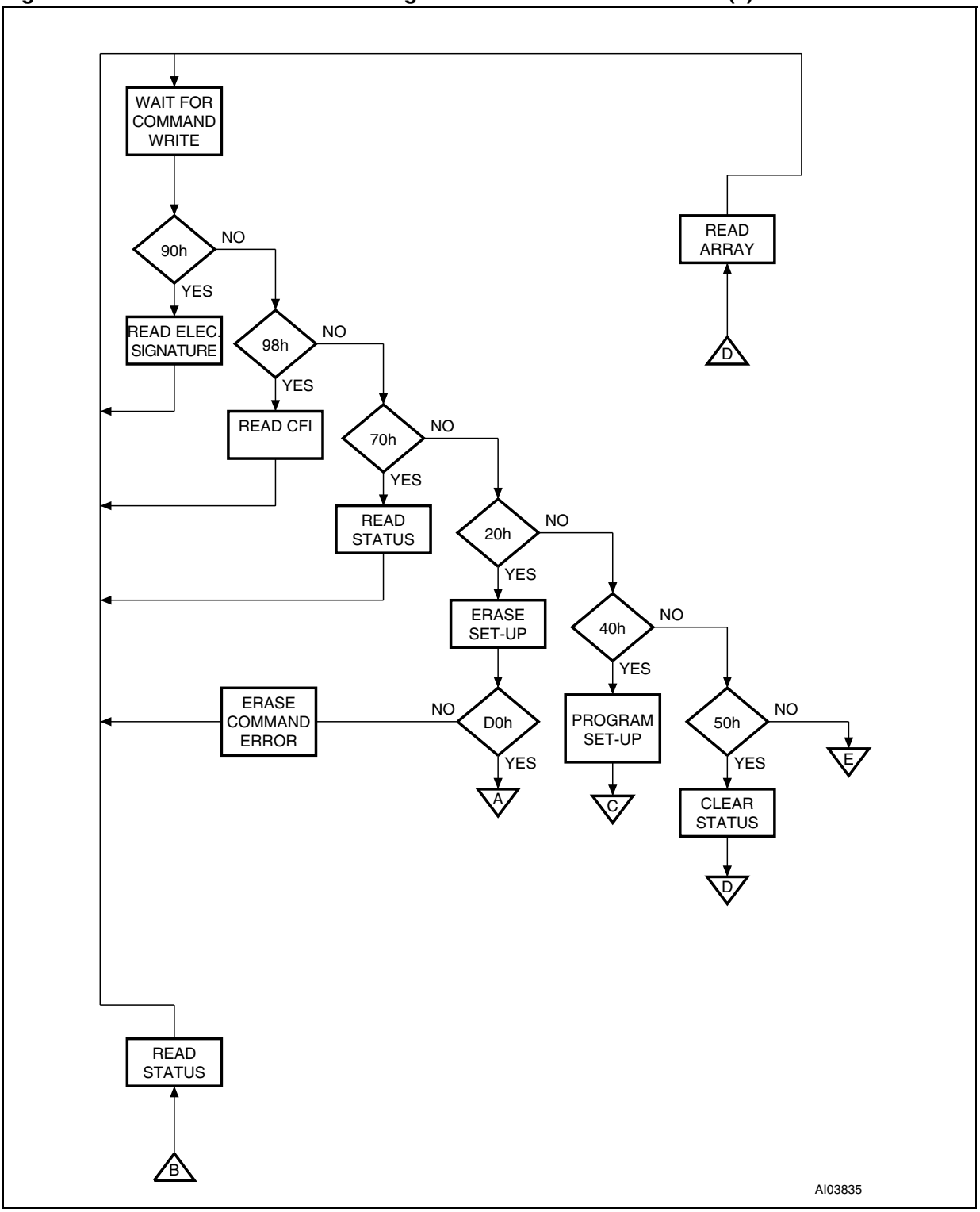


Figure 32. Command interface and Program/Erase controller flowchart (b)

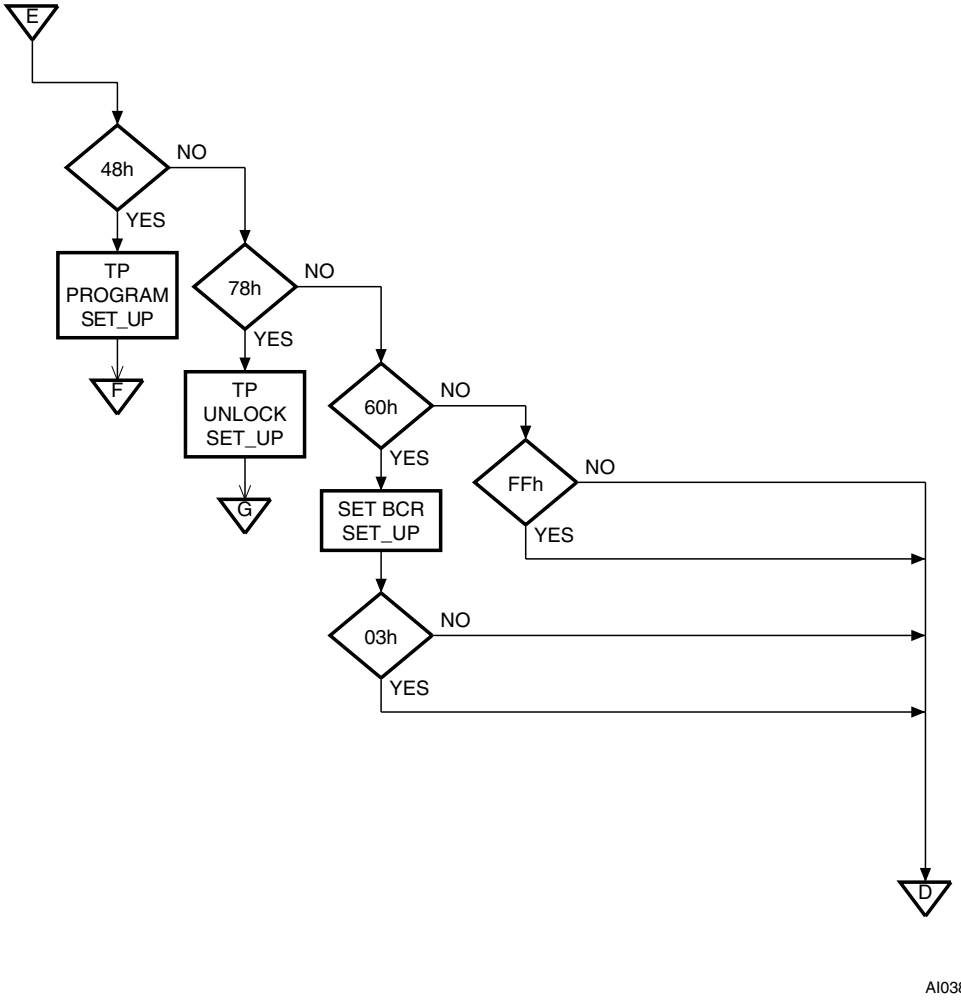


Figure 33. Command interface and Program/Erase controller flowchart (c)

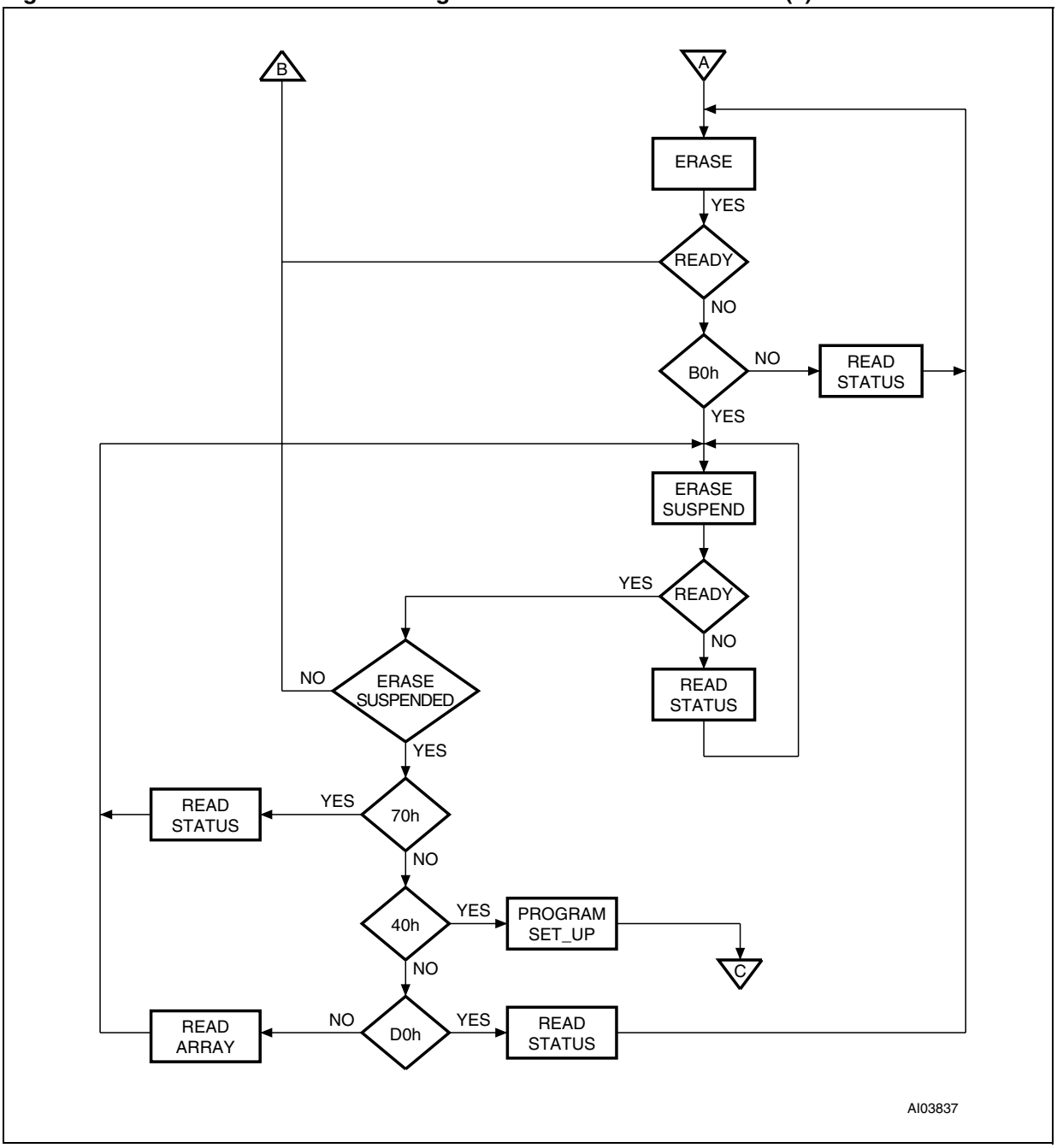


Figure 34. Command interface and Program/Erase controller flowchart (d)

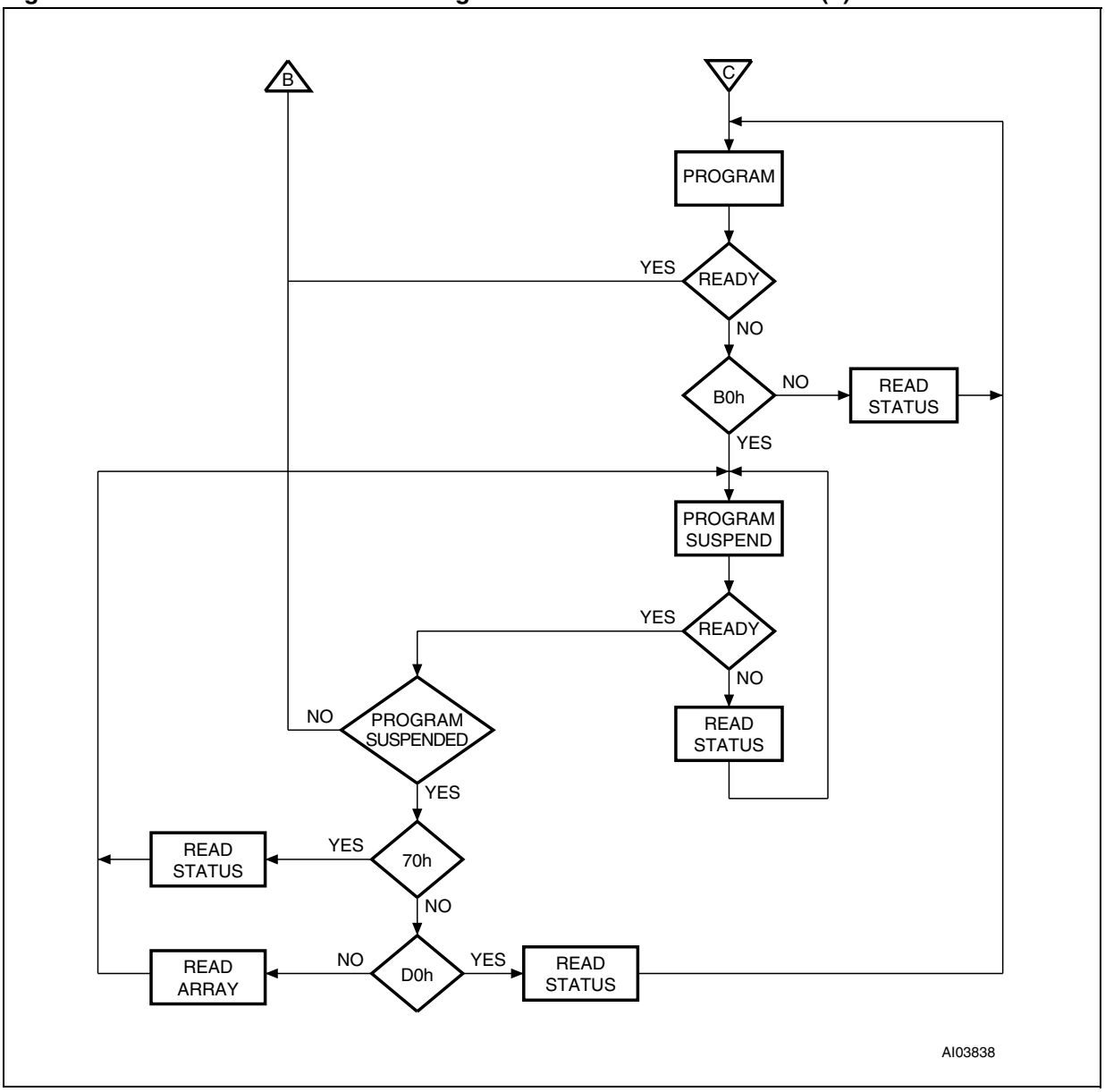
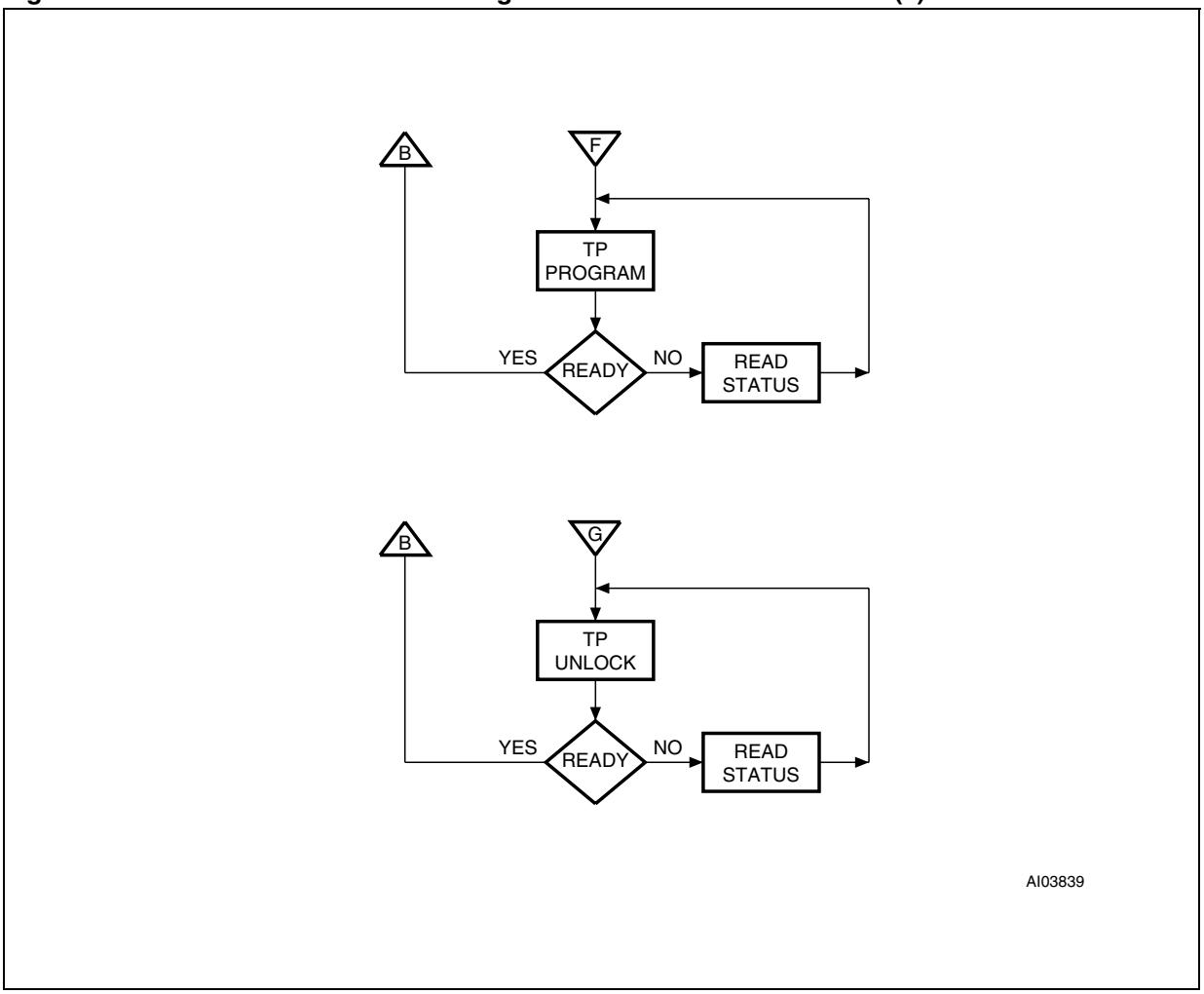


Figure 35. Command interface and Program/Erase controller flowchart (e)



Appendix B Common Flash interface (CFI)

The common Flash interface is a JEDEC approved, standardized data structure that can be read from the Flash memory device. It allows a system software to query the device to determine various electrical and timing parameters, density information and functions supported by the memory. The system can interface easily with the device, enabling the software to upgrade itself when necessary.

When the CFI Query command (RCFI) is issued the device enters CFI Query mode and the data structure is read from the memory. *Table 28*, *Table 29*, *Table 30*, *Table 33* and *Table 32* show the addresses used to retrieve the data.

Table 28. Query structure overview

Offset	Sub-section name	Description	
00h	0020h	Manufacturer code	Numonyx
01h	883A 8839 8838 8837	Device code	M58BW16FT (top) M58BW16FB (bottom) M58BW32FT (top) M58BW32FB (bottom)
10h	CFI query identification string	Command set ID and algorithm data offset	
1Bh	System interface information	Device timing and voltage information	
27h	Device geometry definition	Flash memory layout	
P(h)(1)	Primary algorithm-specific extended query table	Additional information specific to the primary algorithm (optional)	
A(h)(2)	Alternate algorithm-specific extended query table	Additional information specific to the alternate algorithm (optional)	

1. Offset 15h defines P which points to the primary algorithm extended query address table.
2. Offset 19h defines A which points to the alternate algorithm extended query address table.

Table 29. CFI - Query address and data output(1)(2)

Address A0-Amax	Data		Instruction
10h	51h	"Q"	51h; "Q" Query ASCII string 52h; "R" 59h; "Y"
11h	52h	"R"	
12h	59h	"Y"	
13h	03h		Primary vendor: Command set and control interface ID code
14h	00h		
15h	35h (M58BW16F) 39h (M58BW32F)		Primary algorithm extended query address table: P(h)
16h	00h		
17h	00h		Alternate vendor: Command set and control interface ID code
18h	00h		
19h	00h		Alternate algorithm extended query address table
1Ah	00h		

1. The x 8 or byte address and the x 16 or word address mode are not available.
2. Query data are always presented on DQ7-DQ0. DQ31-DQ8 are set to '0'.

Table 30. CFI - device voltage and timing specification

Address A0-Amax	Data	Description	Value
1Bh	27h(1)	V_{DD} min	2.7 V
1Ch	36h(1)	V_{DD} max	3.6 V
1Dh	xxxx xxxxh	Reserved	
1Eh	xxxx xxxxh	Reserved	
1Fh	04h	2^n µs typical for word, double word program	16 µs
20h	xxxx xxxxh	Reserved	
21h	0Ah	2^n ms, typical time-out for Erase Block	1 s
22h	xxxx xxxxh	Reserved	
23h	xxxx xxxxh	Reserved	
24h	xxxx xxxxh	Reserved	
25h	xxxx xxxxh	Reserved	
26h	xxxx xxxxh	Reserved	

1. Bits are coded in binary code decimal, bit7 to bit4 are scaled in Volts and bit3 to bit0 in mV.

Table 31. M58BW16F device geometry definition

Address A0-Amax	Data	Description	Value
27h	15h	2^n number of bytes memory size	2 Mbytes
28h	03h	Device interface sync./async.	x 32
29h	00h	Organization sync./async.	Async.
2Ah	00h	Maximum number of byte in multi-byte program = 2^n	32 bytes
2Bh	00h		
2Ch	02h	Bit7-0 = number of Erase Block regions in device	2
2Dh	1Eh	Number (n-1) of Erase Blocks of identical size; n=31	31 blocks
2Eh	00h		
2Fh	00h	Erase Block region information x 256 bytes per Erase Block (64 Kbytes)	512 Kbits
30h	01h		
31h	07h	Number (n-1) of Erase Blocks of identical size; n=8	8 blocks
32h	00h		
33h	20h	Erase Block region information x 256 bytes per Erase Block (8 Kbytes)	64 Kbits
34h	00h		

Table 32. M58BW16F extended query information

Address offset	Address Amax-A0	Data (hex)		Description
(P)h	35h	50	P	Query ASCII string - extended table
(P+1)h	36h	52	R	
(P+2)h	37h	49	Y	
(P+3)h	38h	31h		Major revision number
(P+4)h	39h	31h		Minor revision number
(P+5)h	3Ah	86h		Optional feature: (1=yes, 0=no) bit0, Chip Erase supported (0= no) bit1, Suspend Erase supported (1=yes) bit2, Suspend Program supported (1=yes) bit3, Lock/Unlock supported (0=no) bit4, Queue Erase supported (0=no) bit5, Instant individual block locking (0=no) bit6, Protection bits supported (0=no) bit7, Page Read supported (1=yes) bit8, Synchronous Read supported (1=yes) Bit9, Reserved
(P+6)h	3Bh	01h		Synchronous Read supported
(P+7)h	3Ch	00h		
(P+8)h	3Dh	00h		
(P+9)h	3Eh	01h		Function allowed after Suspend: Program allowed after Erase Suspend (1=yes) Bit 7-1 reserved for future use
(P+A)h-(P+D)h	3Fh-42h	Reserved		
(P+13)h-(P+40)h	48h-7Fh	Reserved		
(P+41)h	80h	xxxx xxxxh		Unique device ID - 1 (16 bits)
(P+42)h	81h	xxxx xxxxh		Unique device ID - 2 (16 bits)
(P+43)h	82h	xxxx xxxxh		Unique device ID - 3 (16 bits)
(P+44)h	83h	xxxx xxxxh		Unique device ID - 4 (16 bits)

Table 33. M58BW32F device geometry definition

Address A0-Amax	Data	Description	Value
27h	15h	2^n number of bytes memory size	4 Mbytes
28h	03h	Device interface sync./async.	x 32
29h	00h	Organization sync./async.	Async.
2Ah	00h	Maximum number of byte in multi-byte program = 2^n	32 bytes
2Bh	00h		
2Ch	02h	Bit7-0 = number of Erase Block regions in device	3
2Dh	1Eh	Number (n-1) of Erase Block regions of identical size; n = 31	62 blocks
2Eh	00h		
2Fh	00h	Erase Block region information x 256 bytes per Erase Block (64 Kbytes)	512 Kbits
30h	01h		
31h	07h	Number (n-1) of Erase blocks of identical size; n = 8	8 blocks
32h	00h		
33h	20h	Erase Block region information x 256 bytes per Erase Block (8 Kbytes)	64 Kbits
34h	00h		
35h	03h	Number (n-1) of Erase Block of identical size; n = 8	8 blocks
36h	00h		
37h	40h	Erase Block region information x 256 bytes per Erase block (16 Kbytes)	128 Kbits
38h	00h		

Table 34. M58BW32F extended query information

Address offset	Address Amax-A0	Data (hex)		Description
(P)h	39h	50	P	Query ASCII string - extended table
(P+1)h	3Ah	52	R	
(P+2)h	3Bh	49	Y	
(P+3)h	3Ch	31h		Major revision number
(P+4)h	3Dh	31h		Minor revision number
(P+5)h	3Eh	86h		Optional feature: (1=yes, 0=no) bit0, Chip Erase supported (0= no) bit1, Suspend Erase supported (1=yes) bit2, Suspend Program supported (1=yes) bit3, Lock/Unlock supported (0=no) bit4, Queue Erase supported (0=no) bit5, Instant individual block locking (0=no) bit6, Protection bits supported (0=no) bit7, Page Read supported (1=yes) bit8, Synchronous Read supported (1=yes) Bit 9, Reserved
(P+6)h	3Fh	01h		Synchronous Read supported
(P+7)h	40h	00h		
(P+8)h	41h	00h		
(P+9)h	42h	01h		Function allowed after Suspend: Program allowed after Erase Suspend (1=yes) Bit 7-1 reserved for future use
(P+A)h-(P+D)h	43h-46h	Reserved		
(P+13)h-(P+40)h	4Ch-7Fh	Reserved		
(P+41)h	80h	xxxx xxxxh		Unique device ID - 1 (16 bits)
(P+42)h	81h	xxxx xxxxh		Unique device ID - 2 (16 bits)
(P+43)h	82h	xxxx xxxxh		Unique device ID - 3 (16 bits)
(P+44)h	83h	xxxx xxxxh		Unique device ID - 4 (16 bits)

Table 35. Protection register information

Address A0-Amax	Data		Instruction	Value	
	M58BW16FT M58BW16FB	M58BW32FT M58BW32FB		M58BW16FT M58BW16FB	M58BW32FT M58BW32FB
(P+E)h	0x02 0x02	0x01 0x01	Number of Protection register field in JEDEC ID space, Block region information X256 bytes	2 x 64 Kb 2 x 64 Kb	1 x 128 Kb 1 x 128 Kb
(P+F)h	0x01 0xFE	0x01 0xFE	Protection field: this field describes user-available OTP Protection Register bytes. Bits 7-0=physical low address Bits 15-8=physical high address Bits 23-16='n', 2n=Factory pre-programmed bytes Bits 31-24='n', 2n=user programmable bytes	-	-
(P+10)h	0x01 0xFE	0x01 0xFE		-	-
(P+11)h	0x0 0x0	0x0 0x0		-	-
x256	0x12 0x12	0x12 0x12		2 x 64 Kb 2 x 64 Kb	1 x 128 Kb 1 x 128 Kb

Appendix C Block protection

OTP protection

The OTP protection is an user-enabled feature that permanently protects specific blocks, so called “OTP blocks”, against modify operations (program/erase). It is available:

- on one specific 128-kbit parameter block in the M58BW32F- block 1 (01000h-01FFFh) for bottom devices or block 72 (FE000h-FEFFFh) for top devices
- on two specific 64-kbit parameter blocks in the M58BW16F- block 2 and 3 (01000h-01FFFh) for bottom devices or block 36 and 35 (7E000h-7EFFFh) for top devices.

The default state is unprotected. However, once the protection has been enabled, it is impossible to disable it and the OTP blocks will remain “modify protected” for ever.

Obviously, this information is stored in internal non volatile registers.

Activation sequence

If the user wants to make the OTP protection effective on a part, he has to issue the Lock OTP protection command.

The Lock OTP protection requires 2 write cycles:

- write (ADD=000AAh, DATA=49h) - Lock OTP Protection command 1
- write (ADD=00003h, DATA=0000 0000h) - Lock OTP Protection command 2

This sequence of commands has to be given with the Tuning Protection unlocked (if this protection is enabled on the part) and with Write Protect Enable WP_N=’1’. The user can check its execution polling on the SR in the same way as a normal Program Word command.

The program duration lasts about 35 µs like for a standard Program Word command. It is also possible to detect the end of the operation by polling the Status Register.

Any Erase attempt returns A3h in the Status Register while any Program attempt returns 93h.

Once the first write cycle of the Lock OTP protection command is issued, a wrong address on second write cycle will cause the activation sequence to fail. The Status Register allows detecting this event and its value is then B1h (invalid sequence).

As a consequence, the protection is not active and the sequence must be restarted.

The Lock OTP Protection command cannot be suspended.

10 Revision history

Table 36. Document revision history

Date	Revision	Changes
09-Jun-2006	1	Initial release.
23-Nov-2006	2	V_{PEN} signal renamed as PEN and *Program/Erase Enable (PEN)* modified. Continuous burst and wrap options are not available, X-Latencies 7 and 8 removed (see *Table 8: Burst Configuration Register* and *Table 9: Burst type definition*). Notes removed below *Table 8*. t_{WHQV} timing modified in *Table 21: Asynchronous Write and Latch controlled Write AC characteristics*. I_{DD} max modified and I_{DD4} added to *Table 18: DC characteristics*. t_{AXQX} modified in *Table 20: Asynchronous Page Read AC characteristics*. Read access specified in *Asynchronous Bus Read* and *Synchronous Burst Read*. t_{AVKH} and t_{ALKH} added and t_{KHQV} for 55 ns modified in *Table 22: Synchronous Burst Read AC characteristics*. *Figure 9*, *Figure 10*, *Figure 18* and *Figure 19* added. Double Word Program max modified and Minimum effective erase time added to *Table 12: Program, Erase times and endurance cycles*. All Asynchronous Bus Read AC characteristics brought together in *Table 19: Asynchronous Bus Read AC characteristics*. t_{LLEL} removed from *Table 19* and *Figure 7*. *Appendix B: Common Flash interface (CFI)* modified.
01-Oct-2007	3	*Table 8: Burst Configuration Register*, *Table 30: CFI - device voltage and timing specification* and *Table 33: M58BW32F device geometry definition* updated. Minimum values for t_{KHKL}, t_{KLKH} and t_{LLKH} modified in *Table 22: Synchronous Burst Read AC characteristics*. t_{PHLL}, t_{PHRH}, t_{VDHPH}, t_{WLRH}, t_{GLRH}, t_{ELRH}, and t_{LLRH} added in *Table 24: Reset, Power-down and Power-up AC characteristics*. t_{PLRH} removed from *Table 24*. Modified *Figure 22: Reset, Power-down and Power-up AC waveforms - Control pins Low* and *Section 3.3.3: X-Latency bits (M13-M11)*. *Appendix C: Block protection*, *Figure 23: Reset, Power-down and Power-up AC waveforms - Control pins toggling* and *Table 35: Protection register information* added.
15-Jan-2008	4	Updated mechanical data of the LBGA package and *Table 8: Burst Configuration Register*, *Table 12: Program, Erase times and endurance cycles*, *Table 18: DC characteristics*, *Table 21: Asynchronous Write and Latch controlled Write AC characteristics*, *Table 22: Synchronous Burst Read AC characteristics*, and *Section 2.7: Reset/Power-down (RP)*. Added *Figure 21: Power supply slope specification* and *Table 23: Power supply AC and DC characteristics*. Minor text changes.
19-Mar-2008	5	Applied Numonyx branding.

Please Read Carefully: