

To all our customers

Regarding the change of names mentioned in the document, such as Mitsubishi Electric and Mitsubishi XX, to Renesas Technology Corp.

The semiconductor operations of Hitachi and Mitsubishi Electric were transferred to Renesas Technology Corporation on April 1st 2003. These operations include microcomputer, logic, analog and discrete devices, and memory chips other than DRAMs (flash memory, SRAMs etc.) Accordingly, although Mitsubishi Electric, Mitsubishi Electric Corporation, Mitsubishi Semiconductors, and other Mitsubishi brand names are mentioned in the document, these names have in fact all been changed to Renesas Technology Corp. Thank you for your understanding. Except for our corporate trademark, logo and corporate statement, no changes whatsoever have been made to the contents of the document, and these changes do not constitute any alteration to the contents of the document itself.

Note : Mitsubishi Electric will continue the business operations of high frequency & optical devices and power devices.

Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

MITSUBISHI MICROCOMPUTERS

M35061-XXXSP/FP

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

DESCRIPTION

M35061-XXXSP/FP is CATV screen display control IC which can display 40 (horizontal) X 17 (vertical). It has built-in SYRAM which can be used with character ROM.

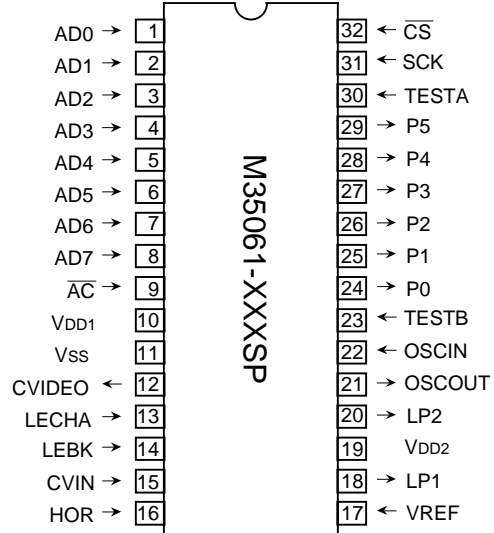
It uses a silicon gate CMOS process and M35061-XXXSP housed in a small 32-pin shrink DIP package, and M35061-XXXFP housed in a small 32-pin shrink SOP package. For M35061-002SP/FP that is a standard ROM version of M35061-XXXSP/FP, the character pattern is also mentioned.

FEATURES

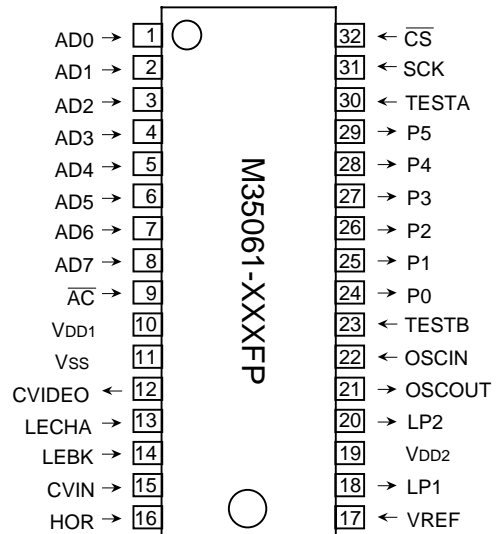
- Screen composition 40 characters X 17 lines
(at scrolling 40 characters X 16 lines)
- Number of characters displayed 680 (Max.)
- Character composition 12 X 13 dot matrix
- Characters available character ROM 128 characters
SYRAM 7 characters
- Character sizes available horizontal 2 (once, twice)
vertical 2 (once, twice)
setting by every line
- Display locations available
Horizontal direction 486 locations
Vertical direction 235 locations
- Blinking character units
Cycle ... approximately 1 second, or approximately 0.5 seconds
(per screen)
Duty 25%, 50% or 75%
(per screen)
- Data input 8-bit parallel X 3
- Coloring Character coloring 8 colors choices per character
(Note)
Background coloring 8 colors choices per character
(Note)
Raster coloring 8 colors choices per screen
- Blanking Character size blanking
Border size blanking
Matrix-outline
Halftone blanking
Can be set by every line
- General-purpose output ports Combined port output 6
(switching to RGB output)
- RAM erase Display RAM erasing by every line
SYRAM erasing separately
- Scrolling Bit by bit smooth scroll implemented by software
- Composite synchronizing signal generation Built-in
(PAL, NTSC, M-PAL)
- Display oscillation circuit Built-in
- Synchronous separation circuit Built-in
- Synchronous correction circuit Built-in

Note: Superimpose coloring is available. (NTSC, PAL, M-PAL)

PIN CONFIGURATION (TOP VIEW)



Outline 32P4B

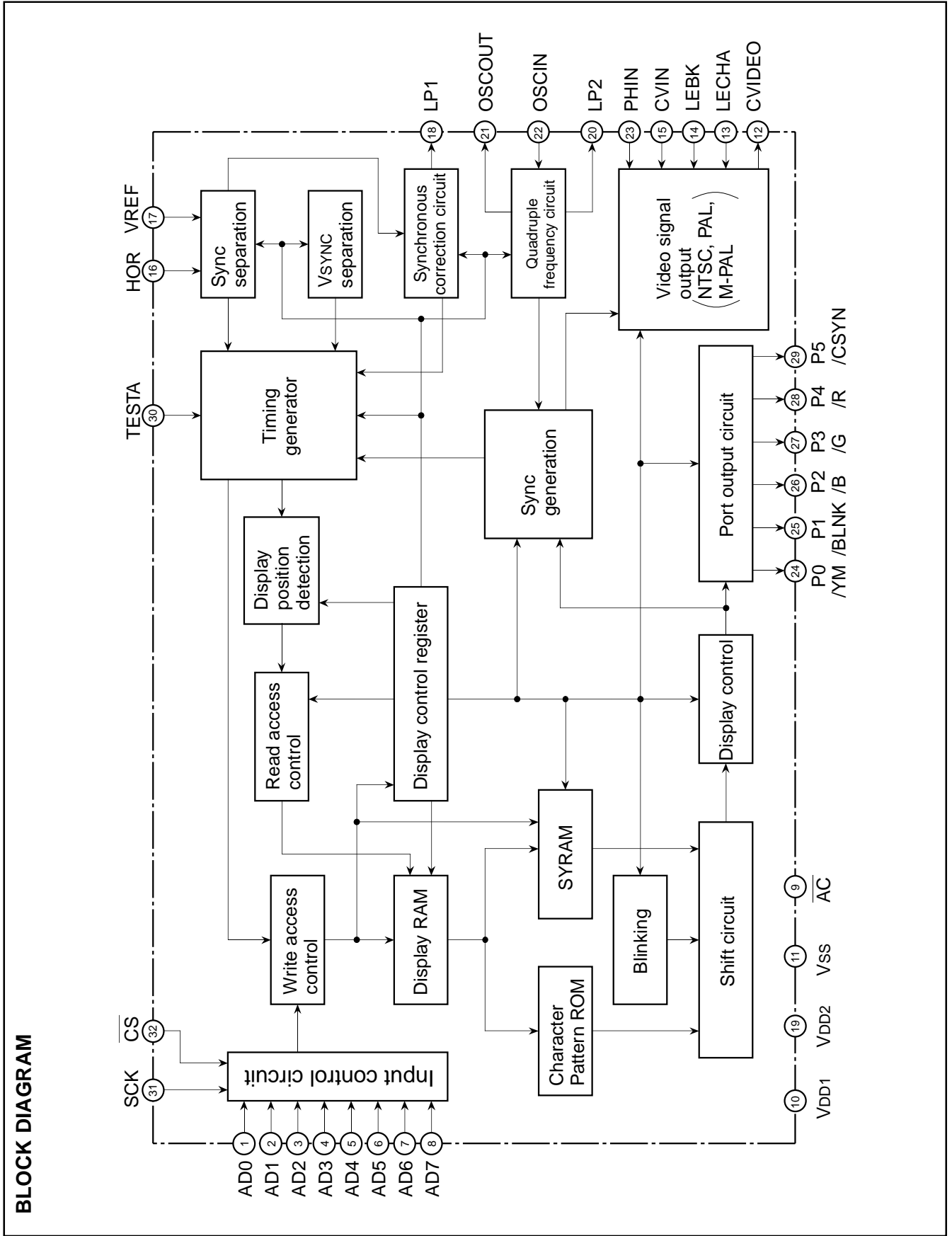


Outline 32P2W-A

PIN DESCRIPTION

Symbol	Pin name	Input/Output	Function
AD0~AD7	Parallel data input	Input	These input pins determine address and data of display control register and display data memory by 8-bit parallel. Hysteresis input is required.
AC	Auto-clear input	Input	When this input pin transitions from "H" to "L", the device is reset. Built-in a pull-up resistor. Hysteresis input is required.
VDD1	Power pin	—	Digital power supply pin. This pin must be connected to +5 V.
VSS	Earthing pin	—	Ground pin. This pin must be connected to 0 V.
CVIDEO	Composite video signal output	Output	This pin outputs the composite video signal. The output signal is 2 VP-P. In superimpose mode, this pin's signal consists of the OSD signal combined with the input composite signal CVIN.
LECHA	Character level input	Input	This input pin is used for controlling the "white" character color level of the OSD signal.
LEBK	Black level input	Input	This input pin is used for controlling the "black" character color level of the OSD signal.
CVIN	Composite video signal input	Input	This pin inputs the external composite video signal. In superimpose mode, this pin's signal consists of the OSD signal combined with the external composite video signal.
HOR	Synchronous signal input	Input	This pin inputs the external composite video signal. This pin inputs the clamped external video signal, sync-sep internal.
VREF	Slice level input	Input	This input pin is used to determine the slice voltage for extracting the sync signals from the video composite signal.
LP1	Filter output 1	Output	This is filter output pin 1.
VDD2	Power pin	—	Analog power supply pin. This pin must be connected to +5 V.
LP2	Filter output 2	Output	This is filter output pin 2.
OSCOUT	fsc I/O pin for synchronous signal generating	Output	These are the sub-carrier oscillation (fsc) input pins for synchronous signal generating. NTSC (3.580 MHz), PAL (4.434 MHz), M-PAL (3.576 MHz) (Note).
OSCIN		Input	
PHIN	PHASE control input	Input	Control the phase changing by scanning line by PAL, M-PAL method.
P0	Port output	Output	This output pin can be configured to port P0 or YM output.
P1	Port output	Output	This output pin can be configured to port P1 or BLNK output.
P2	Port output	Output	This output pin can be configured to port P2 or B output.
P3	Port output	Output	This output pin can be configured to port P3 or G output.
P4	Port output	Output	This output pin can be configured to port P4 or R output.
P5	Port output	Output	This output pin can be configured to port P5 or CSYN output.
TESTA	Test input	Input	Factory test pin. The pin must be connected to GND.
SCK	Clock input for data input	Input	This pin is enabled when the CS pin is "L". Data input to pins AD0 to AD7 is latched at the rising edge of this signal. This pin is hysteresis input.
CS	Chip select input	Input	This is chip selection input pin. When this pin is "L", transmission is enabled. This pin is hysteresis input.

Note: fsc signal inputrefer to "note on when fsc signal input".



M35061-XXXSP/FP

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

MEMORY CONSTRUCTION

Address 00016 to 2A716 are assigned to the display RAM, 2A816 to 2B016 are assigned to the display control registers and 30016 to 36C16 are assigned to SYRAM.

The internal circuit is reset and all display control registers (address 2A816 to 2B016) are set to "0". The memory constitution of display RAM and register is shown in Figure 1 and the memory constitution of SYRAM is shown in Figure 2.

Table 1 The memory constitution of display RAM and register

add- ress	DA17	DA16	DA15	DA14	DA13	DA12	DA11	DA10	DAF	DAE	DAD	DAC	DAB	DAA	DA9	DA8	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0
00016	SB	SG	SR	0	0	0	SYC2	SYC1	SYC0	BB	BG	BR	BLINK	CB	CG	CR	0	C6	C5	C4	C3	C2	C1	C0
λ	SY color setting			0	0	0	SYRAM setting			Raster color setting			BLINK	Character color setting			0	Character setting						
2A716	SB	SG	SR	0	0	0	SYC2	SYC1	SYC0	BB	BG	BR	BLINK	CB	CG	CR	0	C6	C5	C4	C3	C2	C1	C0
2A816	—	TEST 3	TEST 2	TEST 1	TEST 0	TEST 11	TEST 10	HP8	HP7	HP6	HP5	HP4	HP3	HP2	HP1	HP0	VP7	VP6	VP5	VP4	VP3	VP2	VP1	VP0
2A916	—	—	—	BLINK 3	BLINK 2	BLINK 1	BLINK 0	HSZ 16	HSZ 15	HSZ 14	HSZ 13	HSZ 12	HSZ 11	HSZ 10	HSZ 9	HSZ 8	HSZ 7	HSZ 6	HSZ 5	HSZ 4	HSZ 3	HSZ 2	HSZ 1	HSZ 0
2AA16	—	—	—	TEST 12	EQP	TEST 20	HIDE	VSZ 16	VSZ 15	VSZ 14	VSZ 13	VSZ 12	VSZ 11	VSZ 10	VSZ 9	VSZ 8	VSZ 7	VSZ 6	VSZ 5	VSZ 4	VSZ 3	VSZ 2	VSZ 1	VSZ 0
2AB16	—	—	TEST 26	TEST 25	PHASE 2	PHASE 1	PHASE 0	DSP0 16	DSP0 15	DSP0 14	DSP0 13	DSP0 12	DSP0 11	DSP0 10	DSP0 09	DSP0 08	DSP0 07	DSP0 06	DSP0 05	DSP0 04	DSP0 03	DSP0 02	DSP0 01	DSP0 00
2AC16	—	—	—	TEST 21	LINE B	LINE G	LINE R	DSP1 16	DSP1 15	DSP1 14	DSP1 13	DSP1 12	DSP1 11	DSP1 10	DSP1 09	DSP1 08	DSP1 07	DSP1 06	DSP1 05	DSP1 04	DSP1 03	DSP1 02	DSP1 01	DSP1 00
2AD16	—	TEST 23	TEST 22	SERS 0	—	—	—	ERS 16	ERS 15	ERS 14	ERS 13	ERS 12	ERS 11	ERS 10	ERS 9	ERS 8	ERS 7	ERS 6	ERS 5	ERS 4	ERS 3	ERS 2	ERS 1	ERS 0
2AE16	—	—	—	—	—	SEND 4	SEND 3	SEND 2	SEND 1	SEND 0	SST 4	SST 3	SST 2	SST 1	SST 0	SLIN 4	SLIN 3	SLIN 2	SLIN 1	SLIN 0	SBIT 3	SBIT 2	SBIT 1	SBIT 0
2AF16	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0	ALL24	SRAND 2	SRAND 1	SRAND 0	PTD 5	PTD 4	PTD 3	PTD 2	PTD 1	PTD 0	PTC 5	PTC 4	PTC 3	PTC 2	PTC 1	PTC 0
2B016	—	TEST 19	TEST 18	TEST 17	TEST 24	LEVEL 2	LEVEL 1	LEVEL 0	INT NON	PAL NTSC	MPAL	PALH	TEST 16	TEST 15	SEPV1	SEPV0	BLK	—	DSP ONV	DSP ON	—	SEL COR	SCOR	EX

TEST_n (n = number) is MITSUBISHI test memory. Set 0 to all bits.

Table 2 The memory constitution of SYRAM

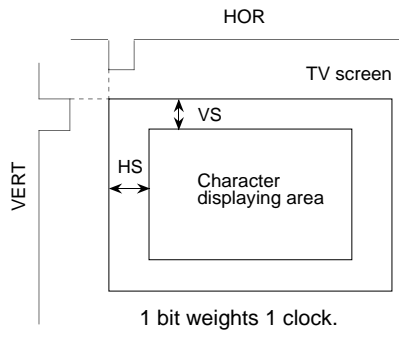
add- ress	DA17 ~ DAD	DAC	DAB	DAA	DA9	DA8	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0	SYRAM code
30016 λ 30C16	0	SYEX	S00B	S00A	S009	S008	S007	S006	S005	S004	S003	S002	S001	S000	0016
31016 λ 31C16	0	SYEX	S01B	S01A	S019	S018	S017	S016	S015	S014	S013	S012	S011	S010	0116
λ	∴	∴	λ											λ	
35016 λ 35C16	0	SYEX	S05B	S05A	S059	S058	S057	S056	S055	S054	S053	S052	S051	S050	0516
36016 λ 36C16	0	SYEX	S06B	S06A	S069	S068	S067	S066	S065	S064	S063	S062	S061	S060	0616

λ : Name or value changes by definite ratio.
∴ : The same name or value continues.

REGISTERS DESCRIPTION

(1) Address 2A816

DA	Register	Contents		Remarks						
		Status	Function							
0	VP0	⓪	If VS is the vertical display start location, $VS = H \times \left(\sum_{n=0}^7 2^n VP_n \right)$ H: Cycle with the horizontal synchronizing pulse	The vertical start location is specified using the 8 bits from VP7 to VP0. VP7 to VP0 < 1416 are not available.						
		1								
		⓪								
		1								
		⓪								
		1								
		⓪								
		1								
1	VP1	⓪	If HS is the horizontal display start location, $HS = T \times \left(\sum_{n=0}^8 2^n HP_n + 9 \right)$ T: Cycle with the display clock	The horizontal start location is specified using the 9 bits from HP8 to HP0. HP8 to HP0 < 1916 are not available.						
		1								
2	VP2	⓪			If HS is the horizontal display start location, $HS = T \times \left(\sum_{n=0}^8 2^n HP_n + 9 \right)$ T: Cycle with the display clock	The horizontal start location is specified using the 9 bits from HP8 to HP0. HP8 to HP0 < 1916 are not available.				
		1								
3	VP3	⓪					If HS is the horizontal display start location, $HS = T \times \left(\sum_{n=0}^8 2^n HP_n + 9 \right)$ T: Cycle with the display clock	The horizontal start location is specified using the 9 bits from HP8 to HP0. HP8 to HP0 < 1916 are not available.		
		1								
4	VP4	⓪							If HS is the horizontal display start location, $HS = T \times \left(\sum_{n=0}^8 2^n HP_n + 9 \right)$ T: Cycle with the display clock	The horizontal start location is specified using the 9 bits from HP8 to HP0. HP8 to HP0 < 1916 are not available.
		1								
5	VP5	⓪	If HS is the horizontal display start location, $HS = T \times \left(\sum_{n=0}^8 2^n HP_n + 9 \right)$ T: Cycle with the display clock	The horizontal start location is specified using the 9 bits from HP8 to HP0. HP8 to HP0 < 1916 are not available.						
		1								
6	VP6	⓪			If HS is the horizontal display start location, $HS = T \times \left(\sum_{n=0}^8 2^n HP_n + 9 \right)$ T: Cycle with the display clock	The horizontal start location is specified using the 9 bits from HP8 to HP0. HP8 to HP0 < 1916 are not available.				
		1								
7	VP7	⓪					If HS is the horizontal display start location, $HS = T \times \left(\sum_{n=0}^8 2^n HP_n + 9 \right)$ T: Cycle with the display clock	The horizontal start location is specified using the 9 bits from HP8 to HP0. HP8 to HP0 < 1916 are not available.		
		1								
8	HP0	⓪							If HS is the horizontal display start location, $HS = T \times \left(\sum_{n=0}^8 2^n HP_n + 9 \right)$ T: Cycle with the display clock	The horizontal start location is specified using the 9 bits from HP8 to HP0. HP8 to HP0 < 1916 are not available.
		1								
9	HP1	⓪	If HS is the horizontal display start location, $HS = T \times \left(\sum_{n=0}^8 2^n HP_n + 9 \right)$ T: Cycle with the display clock	The horizontal start location is specified using the 9 bits from HP8 to HP0. HP8 to HP0 < 1916 are not available.						
		1								
A	HP2	⓪			If HS is the horizontal display start location, $HS = T \times \left(\sum_{n=0}^8 2^n HP_n + 9 \right)$ T: Cycle with the display clock	The horizontal start location is specified using the 9 bits from HP8 to HP0. HP8 to HP0 < 1916 are not available.				
		1								
B	HP3	⓪					If HS is the horizontal display start location, $HS = T \times \left(\sum_{n=0}^8 2^n HP_n + 9 \right)$ T: Cycle with the display clock	The horizontal start location is specified using the 9 bits from HP8 to HP0. HP8 to HP0 < 1916 are not available.		
		1								
C	HP4	⓪							If HS is the horizontal display start location, $HS = T \times \left(\sum_{n=0}^8 2^n HP_n + 9 \right)$ T: Cycle with the display clock	The horizontal start location is specified using the 9 bits from HP8 to HP0. HP8 to HP0 < 1916 are not available.
		1								
D	HP5	⓪	If HS is the horizontal display start location, $HS = T \times \left(\sum_{n=0}^8 2^n HP_n + 9 \right)$ T: Cycle with the display clock	The horizontal start location is specified using the 9 bits from HP8 to HP0. HP8 to HP0 < 1916 are not available.						
		1								
E	HP6	⓪			If HS is the horizontal display start location, $HS = T \times \left(\sum_{n=0}^8 2^n HP_n + 9 \right)$ T: Cycle with the display clock	The horizontal start location is specified using the 9 bits from HP8 to HP0. HP8 to HP0 < 1916 are not available.				
		1								
F	HP7	⓪					If HS is the horizontal display start location, $HS = T \times \left(\sum_{n=0}^8 2^n HP_n + 9 \right)$ T: Cycle with the display clock	The horizontal start location is specified using the 9 bits from HP8 to HP0. HP8 to HP0 < 1916 are not available.		
		1								
10	HP8	⓪							If HS is the horizontal display start location, $HS = T \times \left(\sum_{n=0}^8 2^n HP_n + 9 \right)$ T: Cycle with the display clock	The horizontal start location is specified using the 9 bits from HP8 to HP0. HP8 to HP0 < 1916 are not available.
		1								
11	TEST10	⓪	Test mode (Must be cleared to 0.)							
		1								
12	TEST11	⓪	Test mode (Must be cleared to 0.)							
		1								
13	TEST0	⓪	Test mode (Must be cleared to 0.)							
		1								
14	TEST1	⓪	Test mode (Must be cleared to 0.)							
		1								
15	TEST2	⓪	Test mode (Must be cleared to 0.)							
		1								
16	TEST3	⓪	Test mode (Must be cleared to 0.)							
		1								
17	—	⓪	Must be cleared to 0.							
		1								



Note: The mark ⓪ around the status value means the reset status by the "L" level is input to \overline{AC} pin.

(2) Address 2A916

DA	Register	Contents		Remarks													
		Status	Function														
0	HSZ0	⓪ 1	<table border="1"> <tr> <th>HSZx</th> <th>Horizontal direction character size</th> </tr> <tr> <td>0</td> <td>1T/dot</td> </tr> <tr> <td>1</td> <td>2T/dot</td> </tr> </table> <p style="text-align: right;">T: Display clock</p>	HSZx	Horizontal direction character size	0	1T/dot	1	2T/dot	Set to line 0 of display RAM							
HSZx	Horizontal direction character size																
0	1T/dot																
1	2T/dot																
1	HSZ1	⓪ 1		Set to line 1 of display RAM													
2	HSZ2	⓪ 1		Set to line 2 of display RAM													
3	HSZ3	⓪ 1		Set to line 3 of display RAM													
4	HSZ4	⓪ 1		Set to line 4 of display RAM													
5	HSZ5	⓪ 1		Set to line 5 of display RAM													
6	HSZ6	⓪ 1		Set to line 6 of display RAM													
7	HSZ7	⓪ 1		Set to line 7 of display RAM													
8	HSZ8	⓪ 1		Set to line 8 of display RAM													
9	HSZ9	⓪ 1		Set to line 9 of display RAM													
A	HSZ10	⓪ 1		Set to line 10 of display RAM													
B	HSZ11	⓪ 1		Set to line 11 of display RAM													
C	HSZ12	⓪ 1		Set to line 12 of display RAM													
D	HSZ13	⓪ 1		Set to line 13 of display RAM													
E	HSZ14	⓪ 1	Set to line 14 of display RAM														
F	HSZ15	⓪ 1	Set to line 15 of display RAM														
10	HSZ16	⓪ 1	Set to line 16 of display RAM														
11	BLINK0	⓪ 1	<table border="1"> <tr> <th colspan="2" rowspan="2"></th> <th colspan="2">BLINK0</th> </tr> <tr> <th>0</th> <th>1</th> </tr> <tr> <th rowspan="2">BLINK1</th> <th>0</th> <td>Blinking OFF</td> <td>Duty 25%</td> </tr> <tr> <th>1</th> <td>Duty 50%</td> <td>Duty 75%</td> </tr> </table>			BLINK0		0	1	BLINK1	0	Blinking OFF	Duty 25%	1	Duty 50%	Duty 75%	Blinking duty ratio can be altered.
		BLINK0															
		0	1														
BLINK1	0	Blinking OFF	Duty 25%														
	1	Duty 50%	Duty 75%														
12	BLINK1	⓪ 1															
13	BLINK2	⓪ 1	Cycle approximately 1 second. Cycle approximately 0.5 second.	Blinking cycle can be altered.													
14	BLINK3	⓪ 1	Normal blinking Normal character, reversed character alternation display.	Character is in flashing state. Character is always displayed (normal character, reversed character).													
15	—	⓪ 1	Must be cleared to 0.														
16	—	⓪ 1															
17	—	⓪ 1															

(3) Address 2AA₁₆

DA	Register	Contents		Remarks															
		Status	Function																
0	VSZ0	⓪	VSZx	Vertical direction character size	Set to line 0 of display RAM														
		1																	
1	VSZ1	⓪	0	1H/dot	Set to line 1 of display RAM														
		1																	
2	VSZ2	⓪	1	2H/dot	Set to line 2 of display RAM														
		1																	
3	VSZ3	⓪	H: Horizontal synchronous pulse		Set to line 3 of display RAM														
		1																	
4	VSZ4	⓪			H: Horizontal synchronous pulse		Set to line 4 of display RAM												
		1																	
5	VSZ5	⓪					H: Horizontal synchronous pulse		Set to line 5 of display RAM										
		1																	
6	VSZ6	⓪							H: Horizontal synchronous pulse		Set to line 6 of display RAM								
		1																	
7	VSZ7	⓪									H: Horizontal synchronous pulse		Set to line 7 of display RAM						
		1																	
8	VSZ8	⓪											H: Horizontal synchronous pulse		Set to line 8 of display RAM				
		1																	
9	VSZ9	⓪													H: Horizontal synchronous pulse		Set to line 9 of display RAM		
		1																	
A	VSZ10	⓪															H: Horizontal synchronous pulse		Set to line 10 of display RAM
		1																	
B	VSZ11	⓪																	H: Horizontal synchronous pulse
		1																	
C	VSZ12	⓪	H: Horizontal synchronous pulse																
		1																	
D	VSZ13	⓪			H: Horizontal synchronous pulse														
		1																	
E	VSZ14	⓪					H: Horizontal synchronous pulse												
		1																	
F	VSZ15	⓪							H: Horizontal synchronous pulse										
		1																	
10	VSZ16	⓪									H: Horizontal synchronous pulse								
		1																	
11	HIDE	⓪											SYRAM writing over						
		1											SYRAM writing over or character erasing						
12	TEST20	⓪											Test mode (Must be cleared to 0.)						
		1																	
13	EQP	⓪											It does not include equivalent pulse.						
		1											It includes equivalent pulse.						
14	TEST12	⓪											Test mode (Must be cleared to 0.)						
		1																	
15	—	⓪	Must be cleared to 0.																
		1																	
16	—	⓪																	
		1																	
17	—	⓪																	
		1																	

M35061-XXXSP/FP

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

(4) Address 2AB16

DA	Register	Status	Contents			Remarks																																																	
			Function																																																				
0	DSP0 00	⓪ 1	<table border="1"> <tr> <td>DSP0XX \ DSP1XX</td> <td>0</td> <td>1</td> </tr> <tr> <td>0</td> <td>Character</td> <td>Border</td> </tr> <tr> <td>1</td> <td>Matrix-outline</td> <td>Halftone (Note)</td> </tr> </table>	DSP0XX \ DSP1XX	0	1	0	Character	Border	1	Matrix-outline	Halftone (Note)			Set to line 0 of display RAM																																								
DSP0XX \ DSP1XX	0	1																																																					
0	Character	Border																																																					
1	Matrix-outline	Halftone (Note)																																																					
1	DSP0 01	⓪ 1			Set to line 1 of display RAM																																																		
2	DSP0 02	⓪ 1			Set to line 2 of display RAM																																																		
3	DSP0 03	⓪ 1	Set by combination of DSP0xx (address 2AB16) and DSP1xx (address 2AC16).			Set to line 3 of display RAM																																																	
4	DSP0 04	⓪ 1	At internal synchronous mode (EX = 1), display monitor signal area is all blanking signal (BLNK output) area.			Set to line 4 of display RAM																																																	
5	DSP0 05	⓪ 1	<p>Note: For half-tone display, it is necessary to input the external composite video signal to the CVIN pin, and externally connect a 100 to 200 resistor in series. However, the half-tone display is possible only with superimposed displays.</p>			Set to line 5 of display RAM																																																	
6	DSP0 06	⓪ 1				Set to line 6 of display RAM																																																	
7	DSP0 07	⓪ 1				Set to line 7 of display RAM																																																	
8	DSP0 08	⓪ 1				Set to line 8 of display RAM																																																	
9	DSP0 09	⓪ 1				Set to line 9 of display RAM																																																	
A	DSP0 10	⓪ 1				Set to line 10 of display RAM																																																	
B	DSP0 11	⓪ 1				Set to line 11 of display RAM																																																	
C	DSP0 12	⓪ 1				Set to line 12 of display RAM																																																	
D	DSP0 13	⓪ 1				Set to line 13 of display RAM																																																	
E	DSP0 14	⓪ 1				Set to line 14 of display RAM																																																	
F	DSP0 15	⓪ 1	Set to line 15 of display RAM																																																				
10	DSP0 16	⓪ 1	Set to line 16 of display RAM																																																				
11	PHASE 0	⓪ 1	<table border="1"> <thead> <tr> <th>PHASE</th> <th>PHASE</th> <th>PHASE</th> <th colspan="2">Color</th> </tr> <tr> <td>2</td> <td>1</td> <td>0</td> <th>SELCOR=0</th> <th>SELCOR=1</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>Black</td> <td>Black</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>Red</td> <td>Red-2</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>Green</td> <td>Green-2</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>Yellow</td> <td>Yellow</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>Blue</td> <td>Gray</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>Magenta</td> <td>Yellow-2</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>Cyan</td> <td>Cyan</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>White</td> <td>White</td> </tr> </tbody> </table>		PHASE	PHASE	PHASE	Color		2	1	0	SELCOR=0	SELCOR=1	0	0	0	Black	Black	0	0	1	Red	Red-2	0	1	0	Green	Green-2	0	1	1	Yellow	Yellow	1	0	0	Blue	Gray	1	0	1	Magenta	Yellow-2	1	1	0	Cyan	Cyan	1	1	1	White	White	Raster color setting.
PHASE	PHASE	PHASE	Color																																																				
2	1	0	SELCOR=0	SELCOR=1																																																			
0	0	0	Black	Black																																																			
0	0	1	Red	Red-2																																																			
0	1	0	Green	Green-2																																																			
0	1	1	Yellow	Yellow																																																			
1	0	0	Blue	Gray																																																			
1	0	1	Magenta	Yellow-2																																																			
1	1	0	Cyan	Cyan																																																			
1	1	1	White	White																																																			
12	PHASE 1	⓪ 1																																																					
13	PHASE 2	⓪ 1			Refer Fig 3, 4 about phase angle.																																																		
14	TEST25	⓪ 1	Test mode (Must be cleared to 0.)																																																				
15	TEST26	⓪ 1																																																					
16	—	⓪ 1	Must be cleared to 0.																																																				
17	—	⓪ 1																																																					

(5) Address 2AC16

DA	Register	Status	Contents			Remarks																																																	
			Function																																																				
0	DSP1 00	① 1	<table border="1"> <tr> <td>DSP0XX \ DSP1XX</td> <td>0</td> <td>1</td> </tr> <tr> <td>0</td> <td>Character</td> <td>Border</td> </tr> <tr> <td>1</td> <td>Matrix-outline</td> <td>Halftone (Note)</td> </tr> </table>			DSP0XX \ DSP1XX	0	1	0	Character	Border	1	Matrix-outline	Halftone (Note)	Set to line 0 of display RAM																																								
DSP0XX \ DSP1XX	0	1																																																					
0	Character	Border																																																					
1	Matrix-outline	Halftone (Note)																																																					
1	DSP1 01	① 1				Set to line 1 of display RAM																																																	
2	DSP1 02	① 1				Set to line 2 of display RAM																																																	
3	DSP1 03	① 1	Set by combination of DSP0xx (address 2AB16) and DSP1xx (address 2AC16). At internal synchronous mode (EX = 1), display monitor signal area is all blanking signal (BLNK output) area. Note: For half-tone display, it is necessary to input the external composite video signal to the CVIN pin, and externally connect a 100 to 200 resistor in series. However, the half-tone display is possible only with superimposed displays.			Set to line 3 of display RAM																																																	
4	DSP1 04	① 1				Set to line 4 of display RAM																																																	
5	DSP1 05	① 1				Set to line 5 of display RAM																																																	
6	DSP1 06	① 1				Set to line 6 of display RAM																																																	
7	DSP1 07	① 1				Set to line 7 of display RAM																																																	
8	DSP1 08	① 1				Set to line 8 of display RAM																																																	
9	DSP1 09	① 1				Set to line 9 of display RAM																																																	
A	DSP1 10	① 1				Set to line 10 of display RAM																																																	
B	DSP1 11	① 1				Set to line 11 of display RAM																																																	
C	DSP1 12	① 1				Set to line 12 of display RAM																																																	
D	DSP1 13	① 1				Set to line 13 of display RAM																																																	
E	DSP1 14	① 1				Set to line 14 of display RAM																																																	
F	DSP1 15	① 1				Set to line 15 of display RAM																																																	
10	DSP1 16	① 1				Set to line 16 of display RAM																																																	
11	LINER	① 1				<table border="1"> <thead> <tr> <th rowspan="2">LINE B</th> <th rowspan="2">LINE G</th> <th rowspan="2">LINE R</th> <th colspan="2">Color</th> </tr> <tr> <th>SELCOR=0</th> <th>SELCOR=1</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>Black</td> <td>Black</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>Red</td> <td>Red-2</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>Green</td> <td>Green-2</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>Yellow</td> <td>Yellow</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>Blue</td> <td>Gray</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>Magenta</td> <td>Yellow-2</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>Cyan</td> <td>Cyan</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>White</td> <td>White</td> </tr> </tbody> </table>		LINE B	LINE G	LINE R	Color		SELCOR=0	SELCOR=1	0	0	0	Black	Black	0	0	1	Red	Red-2	0	1	0	Green	Green-2	0	1	1	Yellow	Yellow	1	0	0	Blue	Gray	1	0	1	Magenta	Yellow-2	1	1	0	Cyan	Cyan	1	1	1	White	White	SYRAM color setting. Color is decided by DAC bit (SYEX) of SYRAM or HIDE register.
LINE B	LINE G	LINE R				Color																																																	
						SELCOR=0	SELCOR=1																																																
0	0	0	Black	Black																																																			
0	0	1	Red	Red-2																																																			
0	1	0	Green	Green-2																																																			
0	1	1	Yellow	Yellow																																																			
1	0	0	Blue	Gray																																																			
1	0	1	Magenta	Yellow-2																																																			
1	1	0	Cyan	Cyan																																																			
1	1	1	White	White																																																			
12	LINEG	① 1			Refer Fig. 3, 4 about phase angle.																																																		
13	LINEB	① 1																																																					
14	TEST21	① 1	Test mode (Must be cleared to 0.)																																																				
15	—	① 1																																																					
16	—	① 1	Must be cleared to 0.																																																				
17	—	① 1																																																					

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

(6) Address 2AD₁₆

DA	Register	Contents		Remarks							
		Status	Function								
0	ERS0	0	Erase display RAM	Set to line 0 of display RAM							
		1									
1	ERS1	0	ERSx RAM erase	Set to line 1 of display RAM							
		1	0 do not erase								
2	ERS2	0	1 do erase	Set to line 2 of display RAM							
		1									
3	ERS3	0	Do not set "1" more than 2 bits at the same time. The setting is not retained even if the bit is set to "1". Therefore, it is not necessary to cancel it.	Set to line 3 of display RAM							
		1									
4	ERS4	0			Set to line 4 of display RAM						
		1									
5	ERS5	0				Set to line 5 of display RAM					
		1									
6	ERS6	0					Set to line 6 of display RAM				
		1									
7	ERS7	0						Set to line 7 of display RAM			
		1									
8	ERS8	0							Set to line 8 of display RAM		
		1									
9	ERS9	0								Set to line 9 of display RAM	
		1									
A	ERS10	0									Set to line 10 of display RAM
		1									
B	ERS11	0									Set to line 11 of display RAM
		1									
C	ERS12	0									Set to line 12 of display RAM
		1									
D	ERS13	0									Set to line 13 of display RAM
		1									
E	ERS14	0									Set to line 14 of display RAM
		1									
F	ERS15	0									Set to line 15 of display RAM
		1									
10	ERS16	0									Set to line 16 of display RAM
		1									
11	-	0							Must be cleared to 0.		
		1									
12	-	0									
		1									
13	-	0									
		1									
14	SERS0	0		do not erase SYRAM							Set to SYRAM code 00 ₁₆ to 06 ₁₆ (Note)
		1		erase SYRAM							
15	TEST22	0		Test mode (Must be cleared to 0.)							
		1									
16	TEST23	0									
		1									
17	—	0		Must be cleared to 0.							
		1									

Note: The setting is not retained even if the bit is set to "1". Therefore, it is not necessary to cancel it.

(7) Address 2AE16

DA	Register	Contents		Remarks
		Status	Function	
0	SBIT0	⓪ 1	Set display start bit of scroll block: $SA = \sum_{n=0}^3 2^n (SBIT_n)$	Setting valid SA = 0 to 12 invalid SA = 13 to 15
1	SBIT1	⓪ 1		
2	SBIT2	⓪ 1		
3	SBIT3	⓪ 1		
4	SLIN0	⓪ 1	Set display start line of scroll block: $SB = \sum_{n=0}^4 2^n (SLIN_n)$	Setting valid SB = 0 to 16 invalid SB = 17 to 31
5	SLIN1	⓪ 1		
6	SLIN2	⓪ 1		
7	SLIN3	⓪ 1		
8	SLIN4	⓪ 1		
9	SST0	⓪ 1	Set start line of scroll block (last line number of the fixed block 1): $SC = \sum_{n=0}^4 2^n (SST_n)$	Setting valid SC = 0 to 15 invalid SC = 16 to 31
A	SST1	⓪ 1		
B	SST2	⓪ 1		
C	SST3	⓪ 1		
D	SST4	⓪ 1		
E	SEND0	⓪ 1	Set start line of fixed block 2 (last line number of the scroll block): $SD = \sum_{n=0}^4 2^n (SEND_n)$	When the scrolling on setting valid SD = 2 to 17 invalid SD = 18 to 31 When the scrolling off set SD = 0 SD > SC + 2
F	SEND1	⓪ 1		
10	SEND2	⓪ 1		
11	SEND3	⓪ 1		
12	SEND4	⓪ 1		
13	—	⓪ 1	Must be cleared to 0.	
14	—	⓪ 1		
15	—	⓪ 1		
16	—	⓪ 1		
17	—	⓪ 1		

Note: When the scrolling on, set the ratio which will be SC < SB < SD.

(8) Address 2AF₁₆

DA	Register	Contents		Remarks																								
		Status	Function																									
0	PTC0	⓪	Port P0 output	Select P0 pin																								
		1	YM output																									
1	PTC1	⓪	Port P1 output	Select P1 pin																								
		1	BLNK output																									
2	PTC2	⓪	Port P2 output	Select P2 pin																								
		1	B output																									
3	PTC3	⓪	Port P3 output	Select P3 pin																								
		1	G output																									
4	PTC4	⓪	Port P4 output	Select P4 pin																								
		1	R output																									
5	PTC5	⓪	Port P5 output	Select P5 pin																								
		1	CSYN output																									
6	PTD0	⓪	When port output: 0 output, when YM output: negative polarity.	Select data of P0 pin																								
		1	When port output: 1 output, when YM output: polarity.																									
7	PTD1	⓪	When port output: 0 output, when BLNK output: negative polarity.	Select data of P1 pin																								
		1	When port output: 1 output, when BLNK output: polarity.																									
8	PTD2	⓪	When port output: 0 output, when B output: negative polarity.	Select data of P2 pin																								
		1	When port output: 1 output, when B output: polarity.																									
9	PTD3	⓪	When port output: 0 output, when G output: negative polarity.	Select data of P3 pin																								
		1	When port output: 1 output, when G output: polarity.																									
A	PTD4	⓪	When port output: 0 output, when R output: negative polarity.	Select data of P4 pin																								
		1	When port output: 1 output, when R output: polarity.																									
B	PTD5	⓪	When port output: 0 output, when CSYN output: negative polarity.	Select data of P5 pin																								
		1	When port output: 1 output, when CSYN output: polarity.																									
C	SRAND0	⓪	<table border="1"> <thead> <tr> <th>SRAND</th> <th>SRAND</th> <th colspan="2">SRAND2</th> </tr> <tr> <th>1</th> <th>0</th> <th>0</th> <th>1</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Complete border = 1 dot</td> <td>Right and dot border = 1 dot</td> </tr> <tr> <td>0</td> <td>1</td> <td>Complete border = 2 dot</td> <td>Right and dot border = 2 dot</td> </tr> <tr> <td>1</td> <td>0</td> <td>Complete border = 3 dot</td> <td>Right and dot border = 3 dot</td> </tr> <tr> <td>1</td> <td>1</td> <td>Complete border = 4 dot</td> <td>Right and dot border = 4 dot</td> </tr> </tbody> </table>	SRAND	SRAND	SRAND2		1	0	0	1	0	0	Complete border = 1 dot	Right and dot border = 1 dot	0	1	Complete border = 2 dot	Right and dot border = 2 dot	1	0	Complete border = 3 dot	Right and dot border = 3 dot	1	1	Complete border = 4 dot	Right and dot border = 4 dot	Condition of border display is changeable.
		SRAND		SRAND	SRAND2																							
1	0	0	1																									
0	0	Complete border = 1 dot	Right and dot border = 1 dot																									
0	1	Complete border = 2 dot	Right and dot border = 2 dot																									
1	0	Complete border = 3 dot	Right and dot border = 3 dot																									
1	1	Complete border = 4 dot	Right and dot border = 4 dot																									
1	Vertical direction is 1 dot only.																											
F	ALL24	⓪	Blanking with all 40 characters in matrix-outline mode	Horizontal display range can be altered when all characters are in matrix-outline size. At external synchronous, set to 0. Operation of character code FF ₁₆ becomes ineffective.																								
		1	Horizontal display period fully blanked with all characters in matrix-outline size.																									
10	PC0	⓪	Display frequency f _T control $f_T = f_H \times \left\{ \sum_{n=0}^7 (2^n PC_n) + 512 \right\}$	PC7 to PC0 < 36 ₁₆ , PC7 to PC0 > C6 ₁₆ is not available.																								
11	PC1	⓪																										
12	PC2	⓪																										
13	PC3	⓪																										
14	PC4	⓪																										
15	PC5	⓪																										
16	PC6	⓪																										
17	PC7	⓪																										

Note: At EX (address 2B0₁₆) = "0" (external synchronous), setting "1" of ALL24 register is not available. Refer Fig. 2 about PTC0 to 5, PTD0 to 5.

(9) Address 2B0₁₆

DA	Register	Contents		Remarks															
		Status	Function																
0	EX	⓪	External synchronization	(Note 1)															
		1	Internal synchronization																
1	SCOR	⓪	Superimpose black and white display	Valid at only register "EX"=0 (at external synchronous) (Note 2, 3 and 4)															
		1	Superimpose coloring display																
2	SELCOR	⓪	Normal	Refer to Table 3, 4, 7 and 8.															
		1	Mode of expansion																
3	—	⓪	Must be cleared to 0.																
		1																	
4	DSPON	⓪	Digital output display OFF																
		1	Digital output display ON																
5	DSPONV	⓪	Composite video output display OFF																
		1	Composite video output display ON																
6	—	⓪	Must be cleared to 0.																
		1																	
7	BLK	⓪	Matrix outline	Only at register "DSP1xx" = 1 (xx = 00 to 16) is valid.															
		1	Matrix outline + border (border color is black)																
8	SEPV0	⓪	<table border="1"> <thead> <tr> <th>SEPV1</th> <th>SEPV0</th> <th>Composite Sync Separation Function</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Separation is performed during 1 in vertical blanking period</td> </tr> <tr> <td>0</td> <td>1</td> <td>Separation is performed during 2 in vertical blanking period</td> </tr> <tr> <td>1</td> <td>0</td> <td>Separation is performed during 3 in vertical blanking period</td> </tr> <tr> <td>1</td> <td>1</td> <td>Setting disabled</td> </tr> </tbody> </table>	SEPV1	SEPV0	Composite Sync Separation Function	0	0	Separation is performed during 1 in vertical blanking period	0	1	Separation is performed during 2 in vertical blanking period	1	0	Separation is performed during 3 in vertical blanking period	1	1	Setting disabled	Method of sync separation from composite video. Case 1 condition: vertical sync must repeat 2X within 2 or 3; indicates this area.
		SEPV1		SEPV0	Composite Sync Separation Function														
0	0	Separation is performed during 1 in vertical blanking period																	
0	1	Separation is performed during 2 in vertical blanking period																	
1	0	Separation is performed during 3 in vertical blanking period																	
1	1	Setting disabled																	
1																			
9	SEPV1	⓪																	
		1																	
A	TEST15	⓪	Test mode (Must be cleared to 0.)																
		1																	
B	TEST16	⓪																	
		1																	
C	PALH	⓪	Interlace/noninterlace normal mode	Valid at only PAL and MPAL mode.															
		1	Interlace/noninterlace expansion mode																
D	MPAL	⓪	<table border="1"> <thead> <tr> <th>PAL/NTSC</th> <th>MPAL</th> <th>Format</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>NTSC</td> </tr> <tr> <td>0</td> <td>1</td> <td>M-PAL</td> </tr> <tr> <td>1</td> <td>0</td> <td>PAL</td> </tr> <tr> <td>1</td> <td>1</td> <td>Setting disabled</td> </tr> </tbody> </table>	PAL/NTSC	MPAL	Format	0	0	NTSC	0	1	M-PAL	1	0	PAL	1	1	Setting disabled	
		PAL/NTSC		MPAL	Format														
0	0	NTSC																	
0	1	M-PAL																	
1	0	PAL																	
1	1	Setting disabled																	
1																			
E	PAL/NTSC	⓪																	
		1																	
F	INT/NON	⓪	Interlace																
		1	Noninterlace																

- Notes**
- 1: For internal synchronization, shut out (mute) the external video signal input, outside the IC. This avoids external video signal leaks inside the IC.
 - 2: For superimposed color displays, input an fsc signal which is synchronized with the color burst of the composite video signal (input to the CVIN pin) to the OSCIN pin.
 - 3: When EX (address 2B0₁₆) = "1" (internal synchronization), set the SCOR register to "0".
 - 4: When using a crystal oscillator (for the fsc input) between the OSCIN and OSCOUT pin, set the SCOR register to "0".

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

(9) Address 2B0₁₆ (cont.)

DA	Register	Contents		Remarks
		Status	Function	
10	LEVEL0	⓪	Composite video generation is off.	Refer to Table 5 and 6.
		1	Composite video generation is on.	
11	LEVEL1	⓪	Display clock is on (oscillating).	
		1	Display clock is off (not oscillating).	
12	LEVEL2	⓪	Sync separation is disabled.	
		1	Sync separation is enabled.	
13	TEST24	⓪	Test mode (Must be cleared to 0.)	
		1		
14	TEST17	⓪		
		1		
15	TEST18	⓪		
		1		
16	TEST19	⓪		
		1		
17	—	⓪	Must be cleared to 0.	
		1		

REGISTER CONSTRUCTION COMPOSITION

Table 3 Color and phase of NTSC, PAL (SELCOR = 0)

PHASE2 / LINEB	PHASE1 / LINEG	PHASE0 / LINER	Phase (rad)		Color
			NTSC	PAL	
0	0	0	—	—	Black
0	0	1	7 /16	± 7 /16	Red
0	1	0	27 /16	∓ 5 /16	Green
0	1	1	/16	± /16	Yellow
1	0	0	17 /16	∓ 15 /16	Blue
1	0	1	11 /16	± 11 /16	Magenta
1	1	0	23 /16	∓ 9 /16	Cyan
1	1	1	—	—	White

Table 4 Color and phase of NTSC, PAL (SELCOR = 1)

PHASE2 / LINEB	PHASE1 / LINEG	PHASE0 / LINER	Phase (rad)		Color
			NTSC	PAL	
0	0	0	—	—	Black
0	0	1	7 /16	± 7 /16	Red-2
0	1	0	27 /16	∓ 5 /16	Green-2
0	1	1	/16	± /16	Yellow
1	0	0	—	—	Gray
1	0	1	/16	± /16	Yellow-2
1	1	0	23 /16	∓ 9 /16	Cyan
1	1	1	—	—	White

Table 7 Video signal level (SELCOR = 0)

Color name	Phase (rad)		Luminance level (V)			Chroma amplitude (vs. color burst)		
	NTSC	PAL	Min.	Typ.	Max.	Min.	Typ.	Max.
Sync	—	—	1.3	1.5	1.7	—	—	—
Pedestal	—	—	1.9	2.1	2.3	—	—	—
Color Burst	0	±4 /16	1.9	2.1	2.3	—	1.0	—
Black	—	—	2.1	2.3	2.5	—	—	—
Red	7 /16 ± 2 /16	± 7 /16 ± 2 /16	2.3	2.5	2.7	1.5	3.0	4.5
Green	27 /16 ± 2 /16	∓ 5 /16 ± 2 /16	2.7	2.9	3.1	1.4	2.8	4.2
Yellow	/16 ± 2 /16	± /16 ± 2 /16	3.1	3.3	3.5	1.0	2.0	3.0
Blue	17 /16 ± 2 /16	∓ 15 /16 ± 2 /16	2.0	2.2	2.4	1.0	2.0	3.0
Magenta	11 /16 ± 2 /16	± 11 /16 ± 2 /16	2.5	2.7	2.9	1.4	2.8	4.2
Cyan	23 /16 ± 2 /16	∓ 9 /16 ± 2 /16	2.9	3.1	3.3	1.5	3.0	4.5
White	—	—	3.1	3.3	3.5	—	—	—

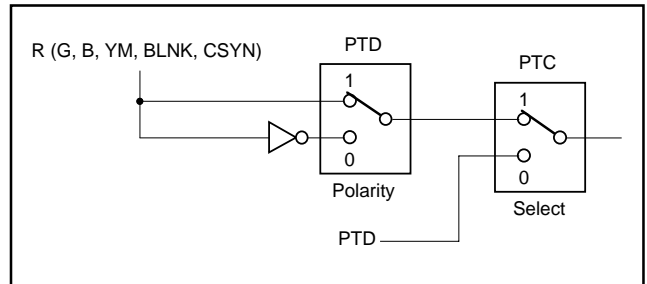


Fig. 2 Switching port output with R, G and B output

Table 5 Setting condition at LEVEL 0, 1 and 2

	At display clock operates	At display clock stops
LEVEL1	0	1
DSPON	1	0
DSPONV	1	0
CS pin	L	H

No character display at display clock

Table 6 Setting condition at LEVEL 0, 1 and 2 (at operation)

	Operation state	Stop state
LEVEL0	1	0
LEVEL1	0	1
LEVEL2	1	0

Table 8 Video signal level (SELCOR = 1)

Color name	Phase (rad)		Luminance level (V)			Chroma amplitude (vs. color burst)		
	NTSC	PAL	Min.	Typ.	Max.	Min.	Typ.	Max.
Sync	—	—	1.3	1.5	1.7	—	—	—
Pedestal	—	—	1.9	2.1	2.3	—	—	—
Color Burst	0	$\pm 4 / 16$	1.9	2.1	2.3	—	1.0	—
Black	—	—	2.1	2.3	2.5	—	—	—
Red-2	$7 / 16 \pm 2 / 16$	$\pm 7 / 16 \pm 2 / 16$	2.6	2.8	3.0	1.5	2.0	3.0
Green-2	$27 / 16 \pm 2 / 16$	$\mp 5 / 16 \pm 2 / 16$	3.1	3.3	3.5	0.5	1.0	1.5
Yellow	$/ 16 \pm 2 / 16$	$\pm / 16 \pm 2 / 16$	3.1	3.3	3.5	1.0	2.0	3.0
Gray	—	—	2.8	3.0	3.2	—	—	—
Yellow-2	$/ 16 \pm 2 / 16$	$\pm / 16 \pm 2 / 16$	3.2	3.4	3.6	0.4	0.8	1.2
Cyan	$23 / 16 \pm 2 / 16$	$\mp 9 / 16 \pm 2 / 16$	2.9	3.1	3.3	1.5	3.0	4.5
White	—	—	3.1	3.3	3.5	—	—	—

DISPLAY FORMS

1. Blanking mode

Display forms are shown in Table 9, display forms at each display mode are shown in Fig. 3.

Table 9 Display forms

Display mode	DSP1 xx (Address 2AC16)	DSP0 xx (Address 2AB16)	BLNK output
Character	0	0	Character size
Border	0	1	Border size
Matrix-outline	1	0	All blanking
Halftone	1	1	Blanking OFF

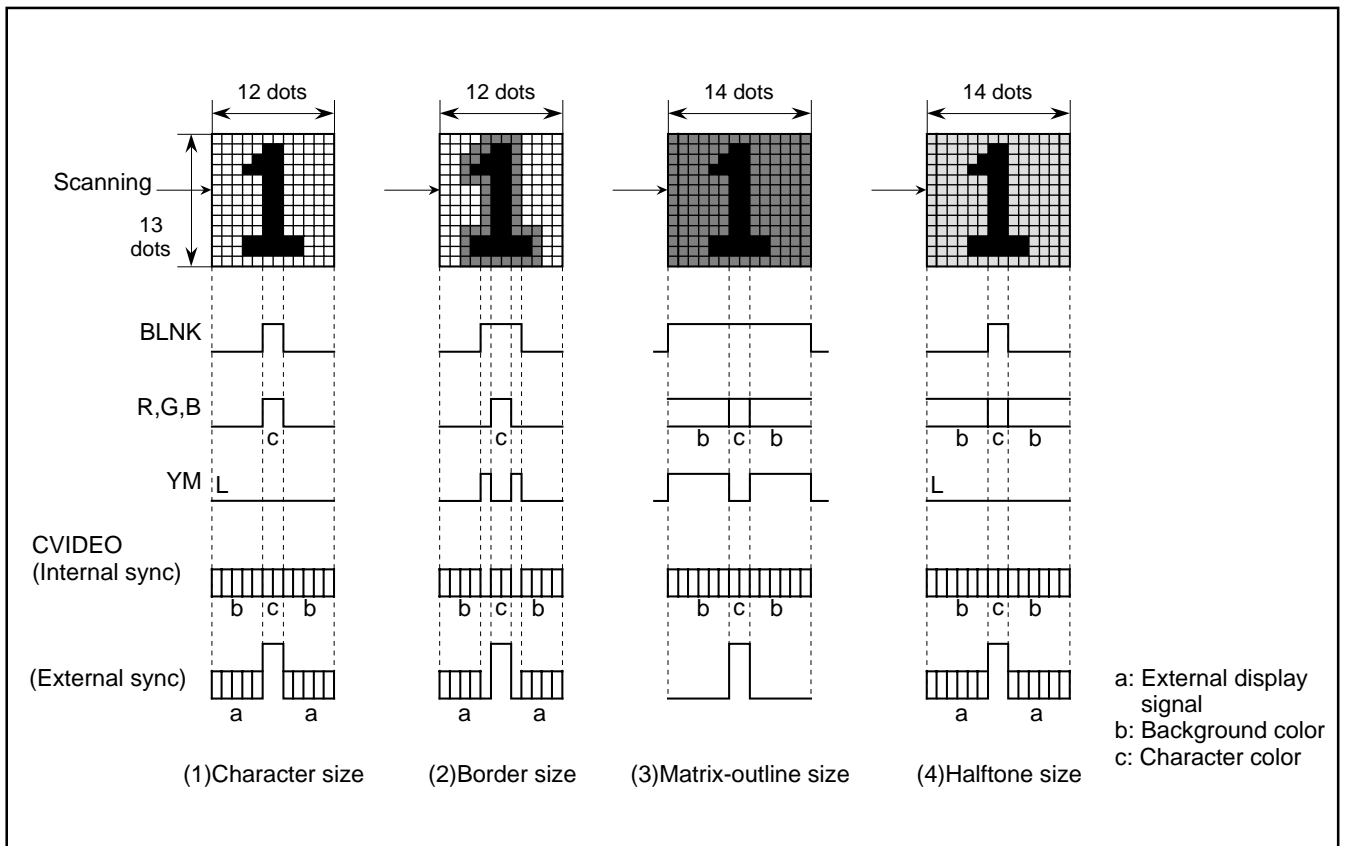


Fig. 3 Display forms at each display mode

For matrix and halftone, a character's number of dots in the horizontal direction increases to 14.

Figure 4 shows a display example for a case where adjacent characters have different background colors and for character code FF₁₆.

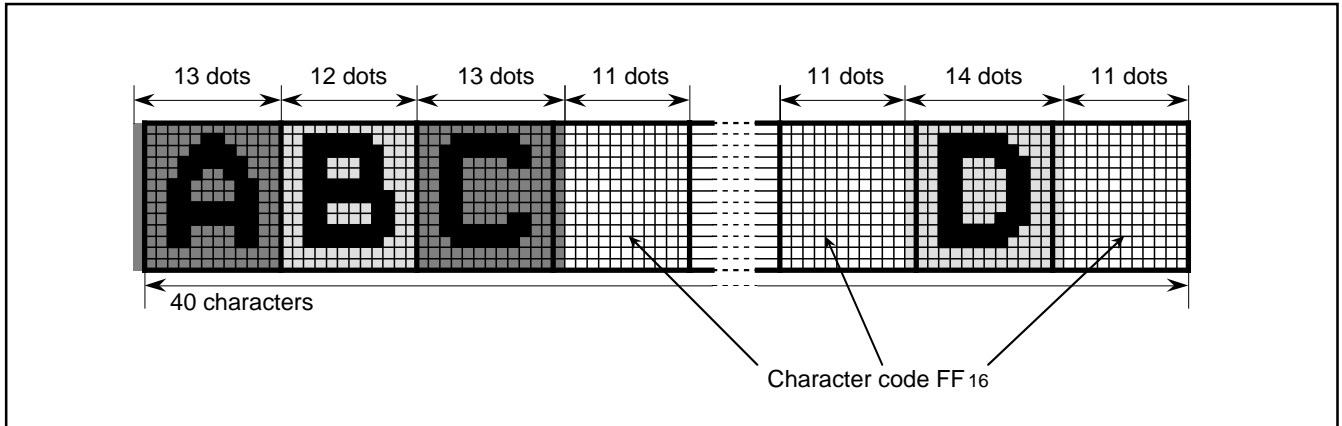
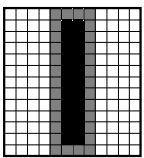
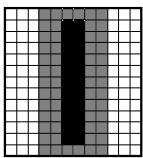
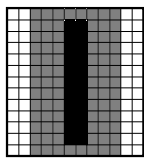
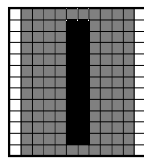
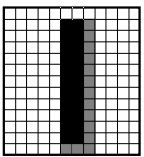
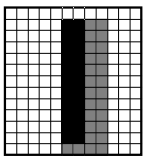
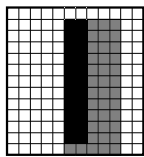
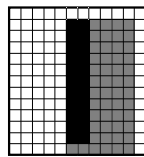


Fig. 4 Number of dots in the horizontal direction at matrix-outline or halftone

2. Border mode

In border mode, characters are displayed with borders. (Refer to Table 9.) In matrix and halftone modes also, characters are displayed with borders if the BLK register (address 2B0₁₆) is set to 1. Table 10 lists the types of borders.

Table 10 Bordering

SRAND2 (Address 2AF ₁₆) \ SRAND1, 0	00	01	10	11
0	The zero dot →  1 dot in horizontal direction	 2 dots in horizontal direction	 3 dots in horizontal direction	 4 dots in horizontal direction
1	 1 dot in horizontal direction	 2 dots in horizontal direction	 3 dots in horizontal direction	 4 dots in horizontal direction

Horizontal direction bordering is only 1 dot. When the character extends to the top line of the matrix, no border is left at the top, and when the character extends to the bottom (12th) line of the matrix, no border is left at the bottom.

3. Setting matrix outline

The ALL24 register (address 2AF16) allows you to set a matrix out-line. A matrix outline can be set for each line by using the DSP1XX register (address 2AC16) .

However, this setting is inhibited if the EX register (address 2B016) is 0 (external sync). An example of how you set a matrix outline is shown in Figure 5.

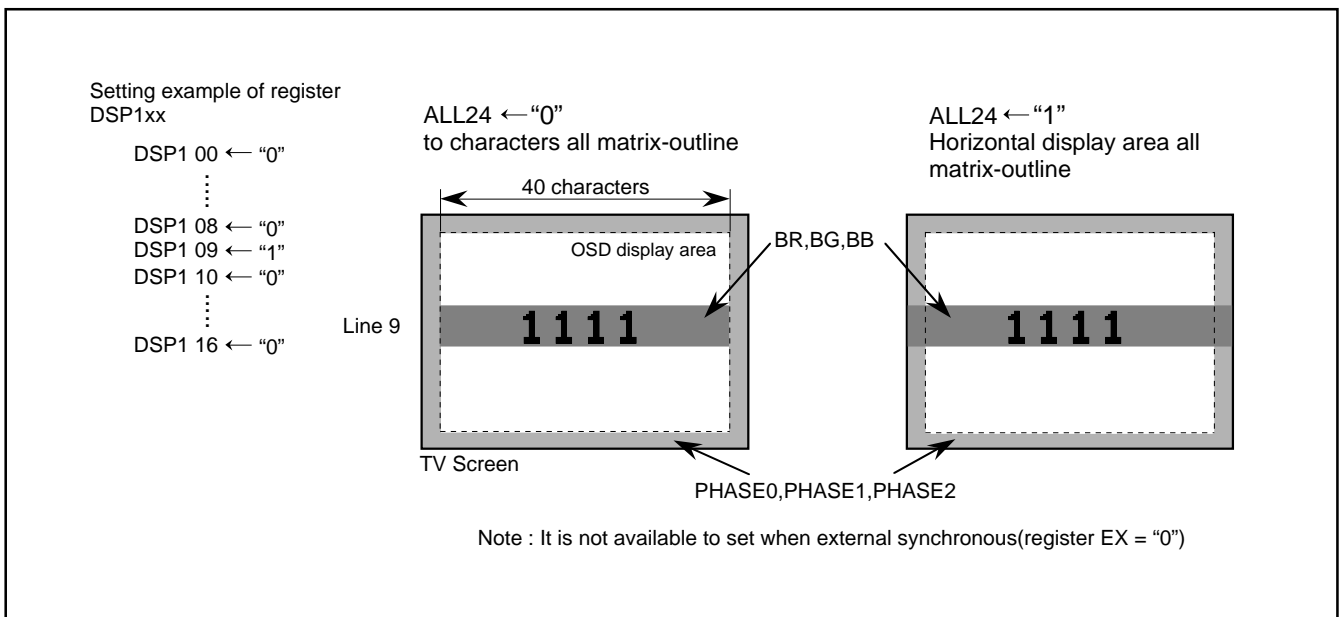


Fig. 5 Setting example all matrix-outline area

4. Blinking mode

Two patterns blinking by register BLINK3 (address 2A916) or BLINK bit of display RAM.

Blinking mode is shown in Table 11 (SYRAM do not blink).

Use registers BLINK0, 1, and 2 (address 2A916) to set the duty ratio and period that determines the blinking time. Tables 12 and 13 list the relationship between the register settings and the duty ratio and pe-riod.

Table 11 Blinking mode

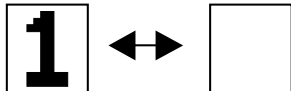

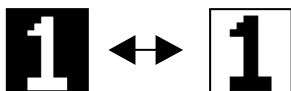

BLINK3	Blinking mode	at blinking OFF
0	Blinking 	Normal 
1	Normal character, reversed character alternation display 	Reverse 

Table 12 Setting of duty ratio

BLINK1	BLINK0	
	0	1
0	Blink OFF	Duty 25%
1	Duty 50%	Duty 75%

Table 13 Setting of cycle

BLINK2	Cycle
0	Approximately 1 second (Vertical sync divided into 1/64)
1	Approximately 0.5 second (Vertical sync divided into 1/32)

5. Scroll display mode

The scroll display mode is entered by setting registers SBIT0 to 3 (SA), SLIN0 to 4 (SB), SST0 to 4 (SC), and SEND0 to 4 (SD) (all at address 2AE16). (Scroll is turned off when SD = 0.)

The screen is scrolled in the range from the (SC)'th line to the (SD-1)'th line, and sections above and below this range are fixed. The beginning line and beginning dot of scroll are the (SA)'th dot

on the (SB)'th line.

The screen can be scrolled up or down by successively incrementing or decrementing SA and SB.

Figure 6 shows examples of how the display is scrolled. The scroll range in these examples contains 12 lines (second to the 13th lines). However, the screen can display only 11 lines at a time, and the re-maining one line is handled as a dummy line and not displayed.

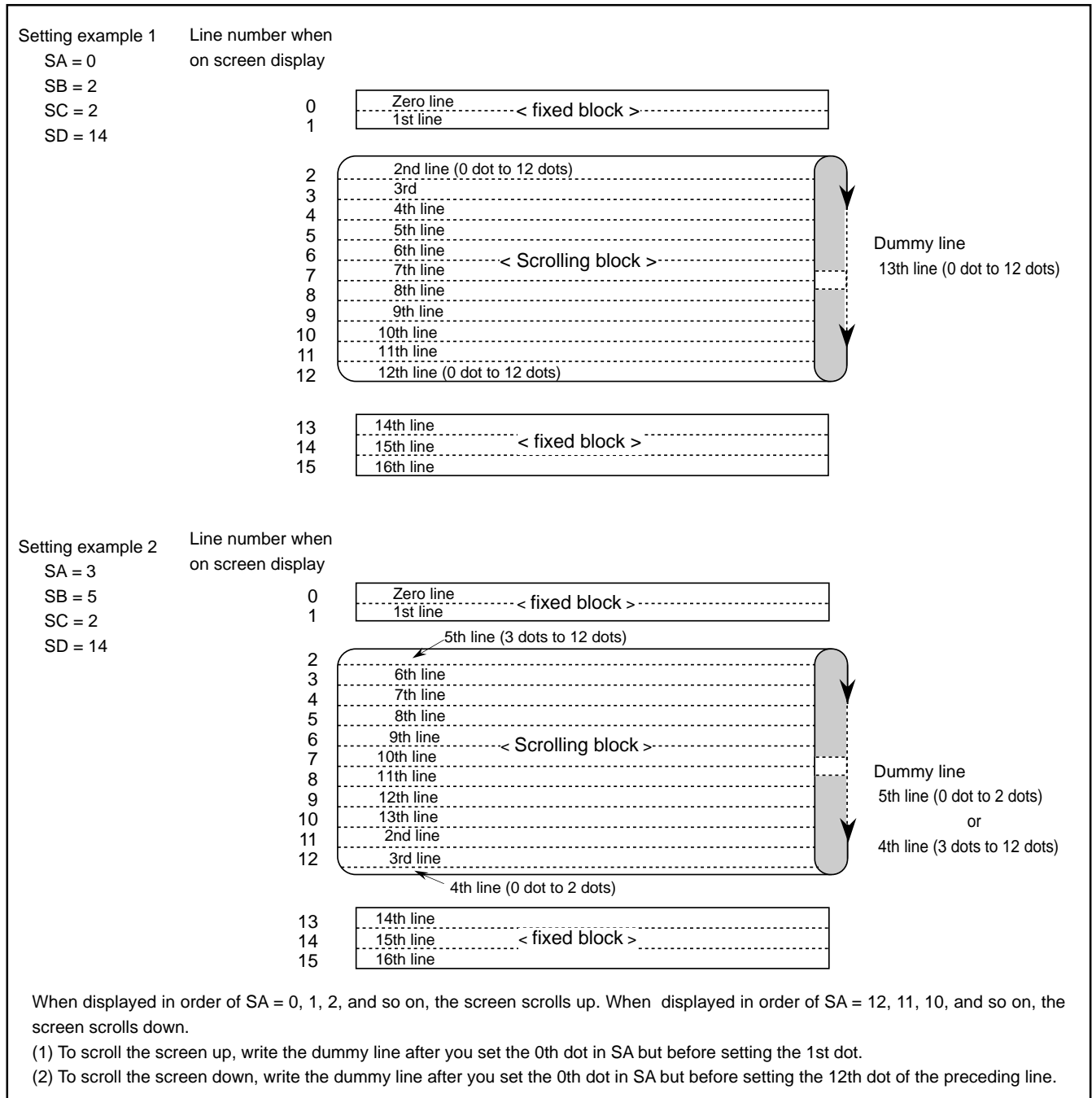


Fig. 6 Scrolling example

6. Character font

(1) Character ROM

Images are composed on a 12 X 13 dot matrix, and characters can be linked vertically and horizontally with other characters to allow the display the continuous symbols.

Character code FF16 is fixed as blank, without a background.

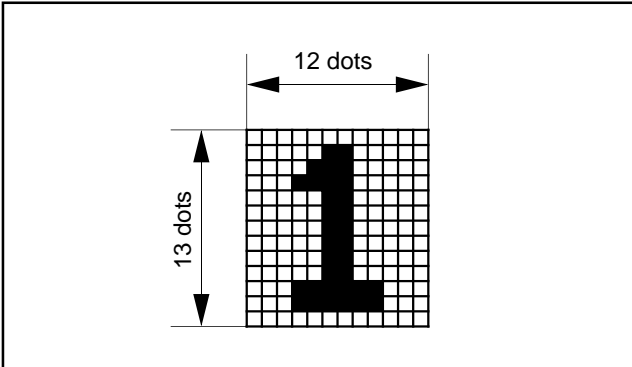


Fig. 7 Character construction

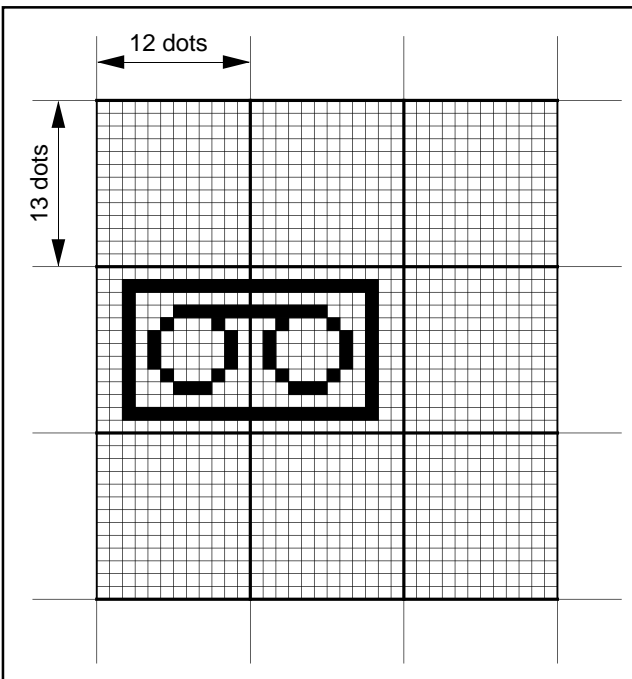


Fig. 8 Example for displaying a continuous pattern

(2) SYRAM

You can set characters for 7 letters per screen (SYRAM code 00₁₆ to 06₁₆). Figure 9 shows an example of how to set.

Use display RAM's SYC2 to 0 (00₁₆ to 06₁₆) to specify SYRAM.

Note that SYRAM code 07₁₆ is fixed to a blank, so you cannot set a character font to this code.

If you do not put SYRAM and a character together, use code 07₁₆.

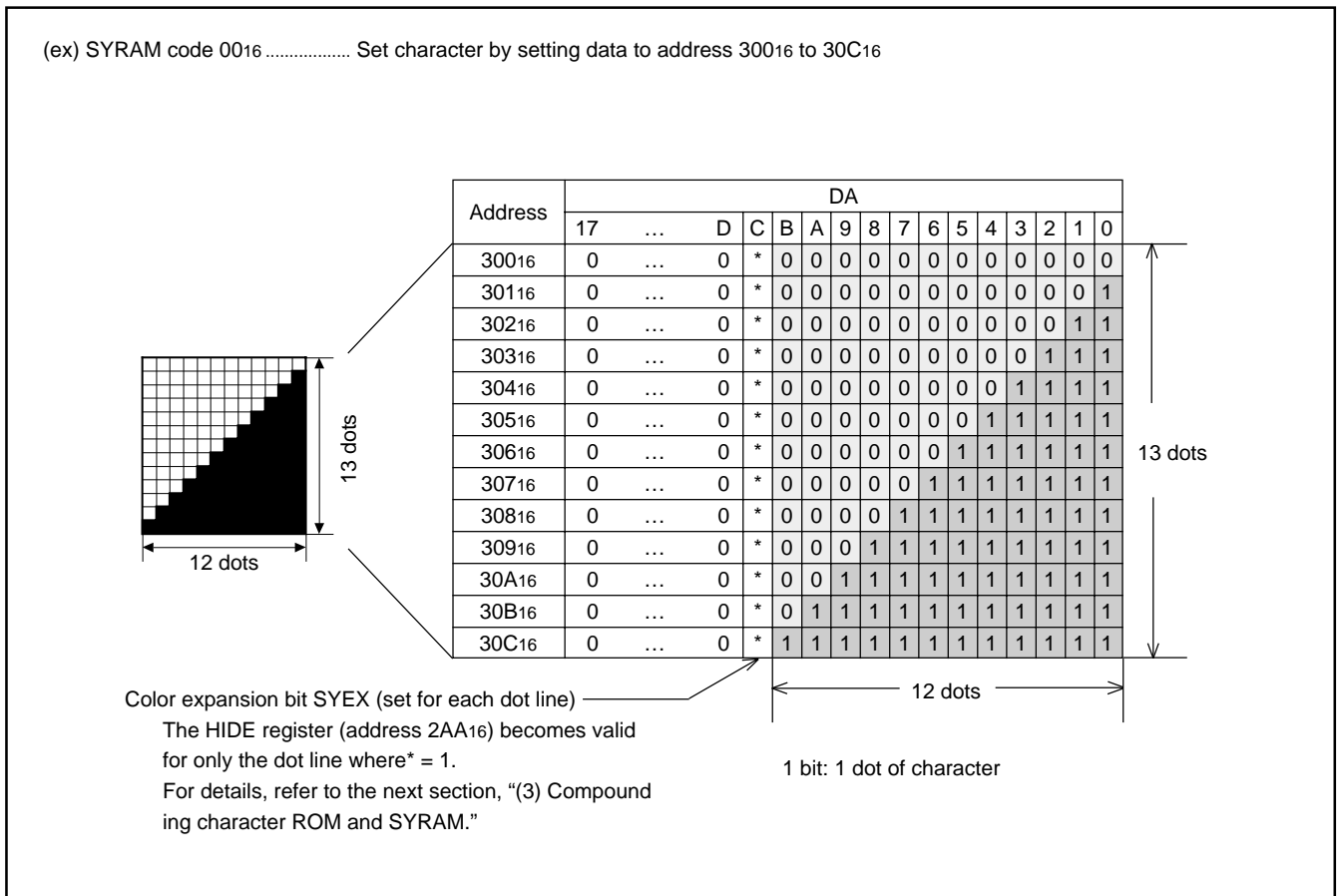


Fig. 9 Setting example of SYRAM

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

(3) Compounding character ROM and SYRAM

You can compound characters in character ROM with SYRAM. The compounding method is determined by the SYEX color expansion bit and the HIDE register (address 2AA16). For dot lines where SYEX = 0, the SYRAM color is set by the display RAM's SR, SG, and SB irrespective of the HIDE register's content. If the HIDE register's content is 0, the SYRAM color for dot lines where SYEX = 1 is set by the LINER, LINEG, and LINEB registers (address 2AC16).

If the HIDE register's content is 1, the character ROM part of the dot lines where SYEX = 1 is overwritten in HIDE mode with colors set by the LINER, LINEG, and LINEB registers irrespective of the ROM's content and color. The color of the SYRAM part is set by the display RAM's SR, SG, and SB as in the case of dot lines where SYEX = 0.

Figure 10 shows an example for each instance of compounding.

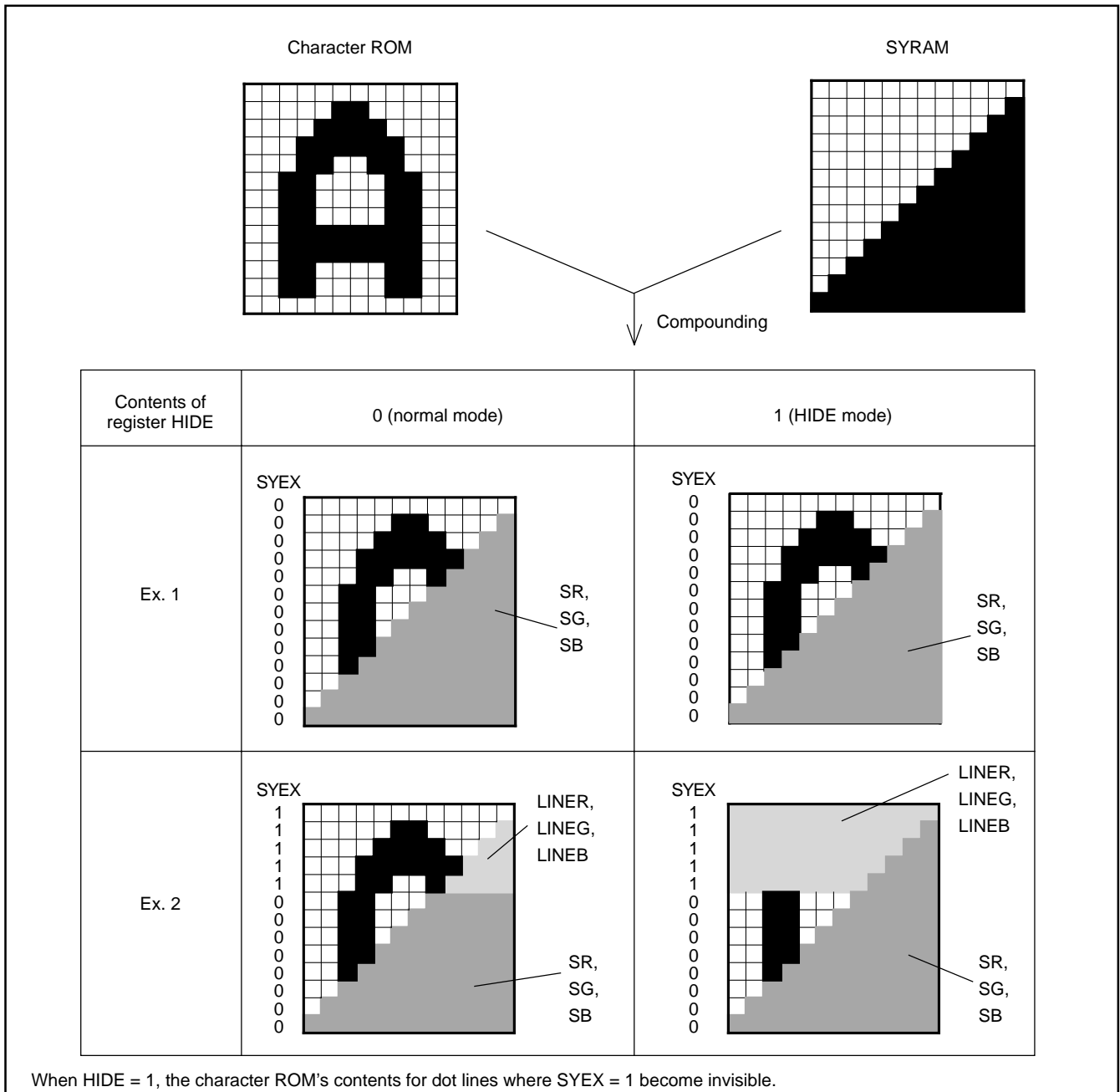


Fig. 10 Compounding example

EXAMPLE FOR DATA INPUT

Use an 8-bit parallel X 3 serial input to set data in the display RAM, display control register, and SYRAM. Table 14 lists an example of how data is set.

Table 14 Data setting

No.	Contents		DA																	
	Address/data	Remarks	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	Address (2B016)	Address setting	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
2	Data (2B016)	Display OFF	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
3	Data (30016)	Set addresses SYRAM 30016 to 36C16	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
4	Data (30116)		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
⋮	⋮		⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	
93	Data (36C16)		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
94	Address (00016)	Set address	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
95	Data (00016)	Set registers address display RAM 00016 to 2A716	SB	SG	SR	0	0	0	0	SVC	0	0	0	0	0	0	0	0	0	0
96	Data (00116)		SB	SG	SR	0	0	0	0	SVC	0	0	0	0	0	0	0	0	0	0
⋮	⋮		⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
773	Data (2A716)		SB	SG	SR	0	0	0	0	SVC	0	0	0	0	0	0	0	0	0	0
774	Data (2A816)	Set registers address 2A816 to 2AF16	0	0	0	0	0	0	0	HP8	HP7	HP6	HP5	HP4	HP3	HP2	HP1	HP0	VP7	VP6
775	Data (2A916)		0	0	0	0	0	0	0	0	HSZ	HSZ	HSZ	HSZ	HSZ	HSZ	HSZ	HSZ	HSZ	HSZ
776	Data (2AA16)		0	0	0	0	0	0	0	VSZ	VSZ	VSZ	VSZ	VSZ	VSZ	VSZ	VSZ	VSZ	VSZ	VSZ
777	Data (2AB16)		0	0	0	0	0	0	0	DSP	DSP	DSP	DSP	DSP	DSP	DSP	DSP	DSP	DSP	DSP
778	Data (2AC16)		0	0	0	0	0	0	0	LINE	LINE	LINE	LINE	LINE	LINE	LINE	LINE	LINE	LINE	LINE
779	Data (2AD16)		0	0	0	0	0	0	0	SERS	0	0	0	0	0	0	0	0	0	0
780	Data (2AE16)		0	0	0	0	0	0	0	SEND	SEND	SEND	SEND	SEND	SEND	SEND	SEND	SEND	SEND	SEND
781	Data (2AF16)		PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0	ALL24	SRAND	SRAND	PTD	PTD	PTD	PTD	PTD	PTD	PTC
782	Data (2B016)	Display ON	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0

SERIAL DATA INPUT TIMING

- (1) The address consists of 8 bits X 3.
- (2) The data consists of 8 bits X 3.
- (3) The 8 bits X 3 in the SCK after the \overline{CS} signal has fallen are the address, and for succeeding input data, the address is incremented every 24 bits (8 bits X 3). Refer to Fig.12 about detail for address increment.

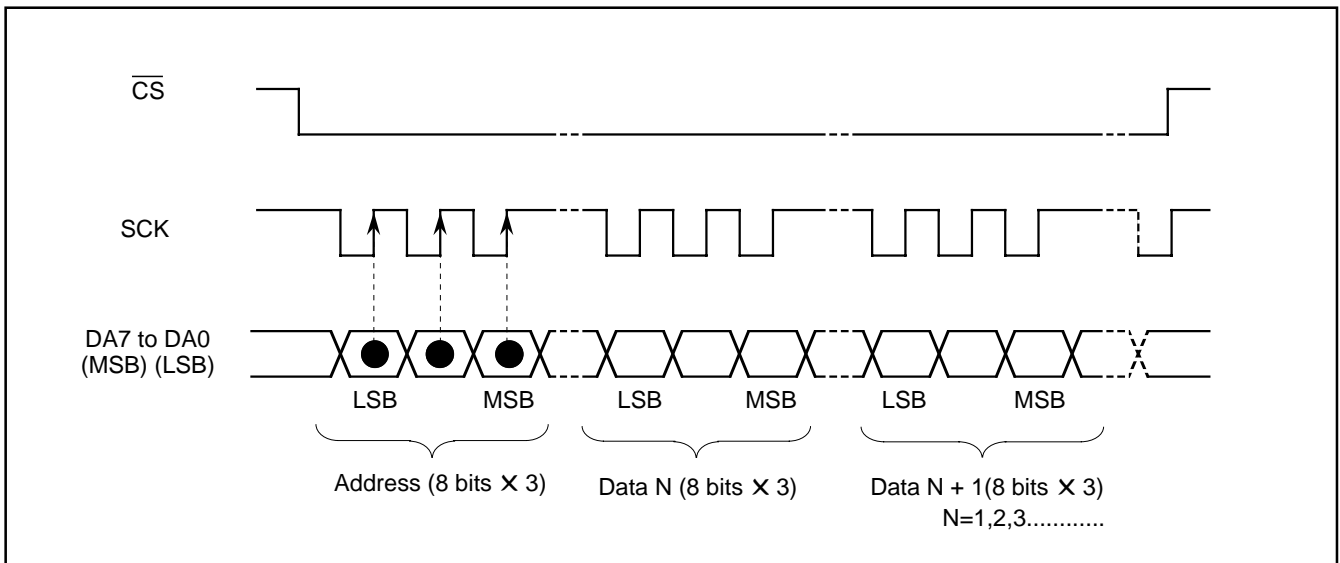


Fig. 11 Serial input timing

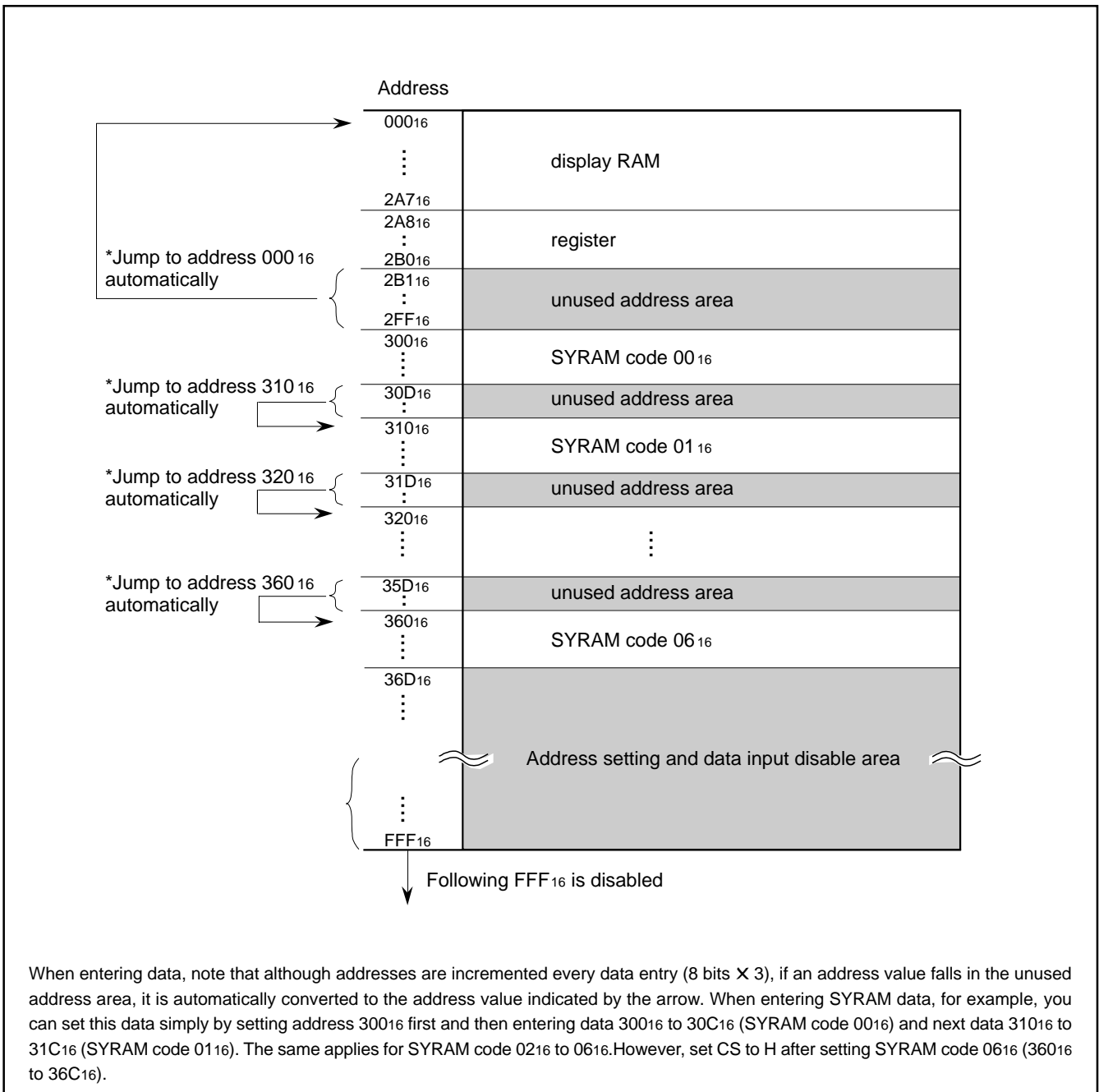


Fig. 12 Address construction

Notes on others

1. At system start-up

At system start-up, always set the \overline{AC} pin to low level before setting registers.

2. Power supply noise

When power supply noise is generated, the internal oscillator circuit does not stabilize, whereby causing horizontal jitters across the picture display. Therefore, connect a bypass capacitor between the power supply and GND.

3. At power on

When power to the M35061-XXXSP/FP is activated, characters are sometimes output without defining the internal display RAM, composite RAM and register. Also, immediately after power is turned on, up until the oscillator circuit stabilizes, data is sometimes not set correctly in the register. Therefore, use the following start-up procedure.

- (a) Activate power. (\overline{AC} pin = "L")
- (b) Engage auto clear. (\overline{AC} pin = "H")
- (c) Disable data input for a 200 m sec (time enough to allow the internal oscillator circuit to stabilize).
- (d) Set register LEVEL n.
- (e) Set register PAL/ \overline{NTSC} .
- (f) Set register PC n.
- (g) Disable data input for a 20 m sec (time enough to allow the internal oscillator circuit to stabilize).
- (h) Set other registers.
- (i) Set the SYRAM.
- (j) Set the internal display RAM.
- (k) Turn registers DSPON and DSPONV on.

4. When resuming internal oscillation from the off state

The internal oscillator circuit stops oscillating when register LEVEL 1 = 1, DSPON = 0, DSPONV = 0 and \overline{CS} pin = "H".

When resuming internal oscillation from the off state, up until the oscillator circuit stabilizes, data is sometimes not set correctly in the register. Therefore, start oscillation as follows.

- (a) \overline{CS} pin = "H" (Oscillation off)
- (b) \overline{CS} pin = "L" (Oscillation start)
- (c) Wait for a 20 m sec (time enough to allow the internal oscillator circuit to stabilize).
- (d) Set register LEVEL 1 = 0.
- (e) Set other registers, SYRAM and internal display RAM.
- (f) Turn registers DSPON and DSPONV on.

5. Other notes on oscillation

Make note of the fact that the internal oscillator circuit cannot stabilize in the below situations.

- (a) When the external composite video signal is discontinuous (when changing channels, etc.)
- (b) When register PC n setting is changed
- (c) When register LEVEL n setting is changed

Before changing settings, turn registers DSPON and DSPONV off. Also, disable data input for 20 m sec after making settings.

6. When no external composite video signal is input

Without a signal, characters cannot be displayed by external synchronization. Therefore, switch to internal synchronization.

7. When signal level of the external composite video signal is extremely poor

With a weak electric field, character display is uncontrollable by external synchronization. Therefore, switch to internal synchronization.

8. When a crystal oscillator is used as the IC's fsc input

It is possible to connect a crystal oscillator between OSCIN and OSCOUT to input the subcarrier frequency (fsc) signal to the OSCIN pin. Talk with the manufacturer of the crystal oscillator you want to use about matching it to this IC.

However, when using a crystal oscillator, it is not possible to superimpose colors. Therefore, set the SCOR register (address 2B016 in DAI register) to "0".

Crystal oscillator frequency

- NTSC system : 3.580 MHz
- PAL system : 4.434 MHz
- M-PAL system : 3.576 MHz

9. Notes on superimposed colors

(1) Register setting

The below table gives register settings for superimposed colors.

Broad-casting method \ Register	PAL/NTSC	MPAL	EX	SCOR	PHIN pin
NTSC	0	0	0	1	Connect to GND
PAL	1	0	0	1	Input control signal. Refer to (2)
M-PAL	0	1	0	1	Input control signal. Refer to (2)

(2) Signal input to PHIN (23-pin) pin

It is necessary to input a control signal for alternating color burst phase (CB1/CB2) every other scanning line. The signal is input into the PHIN (23-pin) pin.

The below figure shows timing for the signal input to the PHIN (23-pin) pin.

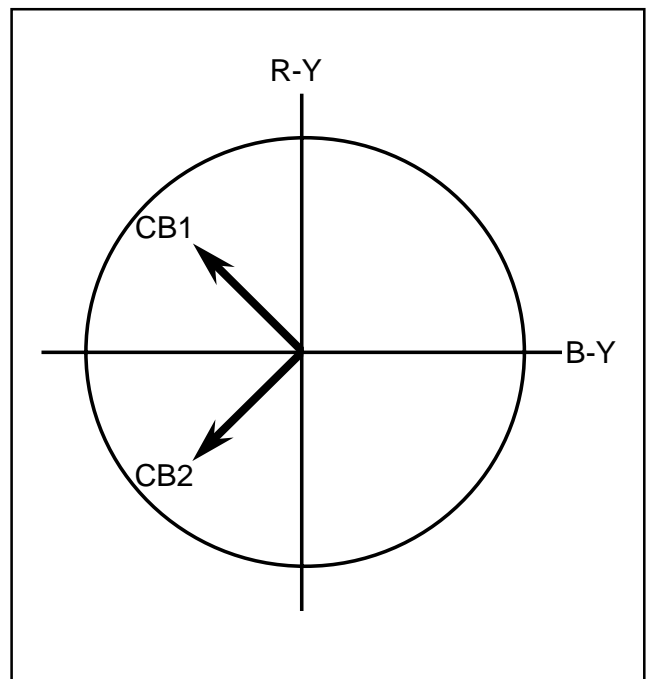


Fig. 13 Bector phase of PAL, M-PAL method

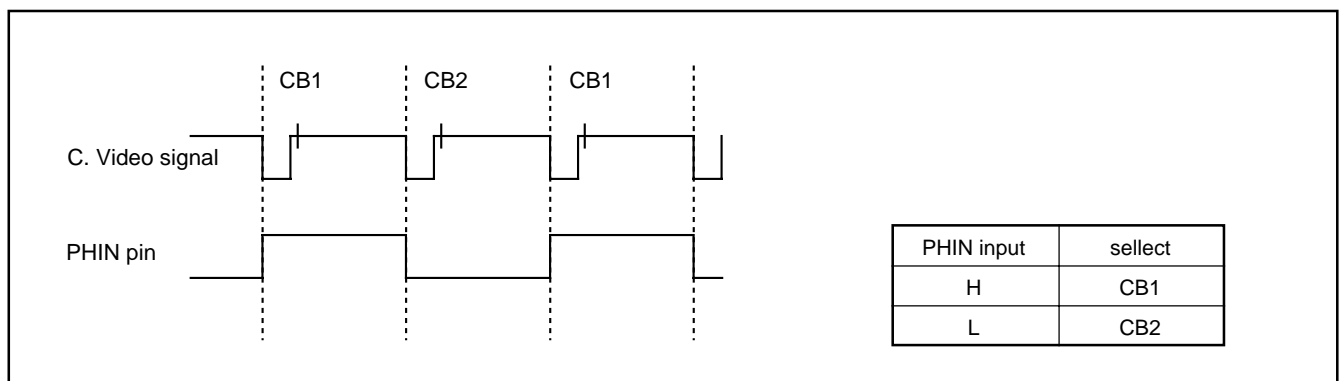


Fig. 14 Signal input timing for PHIN (23-pin) pin

10. Notes on fsc signal input

(1) This IC amplifies the subcarrier frequency (fsc) signal (NTSC system: 3.580 MHz, PAL system: 4.434 MHz, M-PAL system: 3.576 MHz) input to the OSCIN pin and generates the composite video signal internally.

The amplified fsc signal can be destabilized in the following cases.

(a) When the fsc signal is outside of recommended operating conditions

(b) When the waveform of the fsc signal is distorted

(c) When DC level in the fsc waveform fluctuates

When the amplified signal is unstable, the composite video signal generated inside the IC is also unstable in terms of synchronization with the subcarrier and phase.

Consequently, this results in color flicker and lost synchronization when the composite video signal is generated. Make note of the fact that this may prevent a stable blue background from being formed.

(2) When switching to internal synchronization from external synchronization (fsc signal is OFF), start fsc signal input 20 m sec or more before the internal oscillator circuit stabilizes.

M35061-XXXSP/FP PERIPHERAL CIRCUIT (For external fsc input)

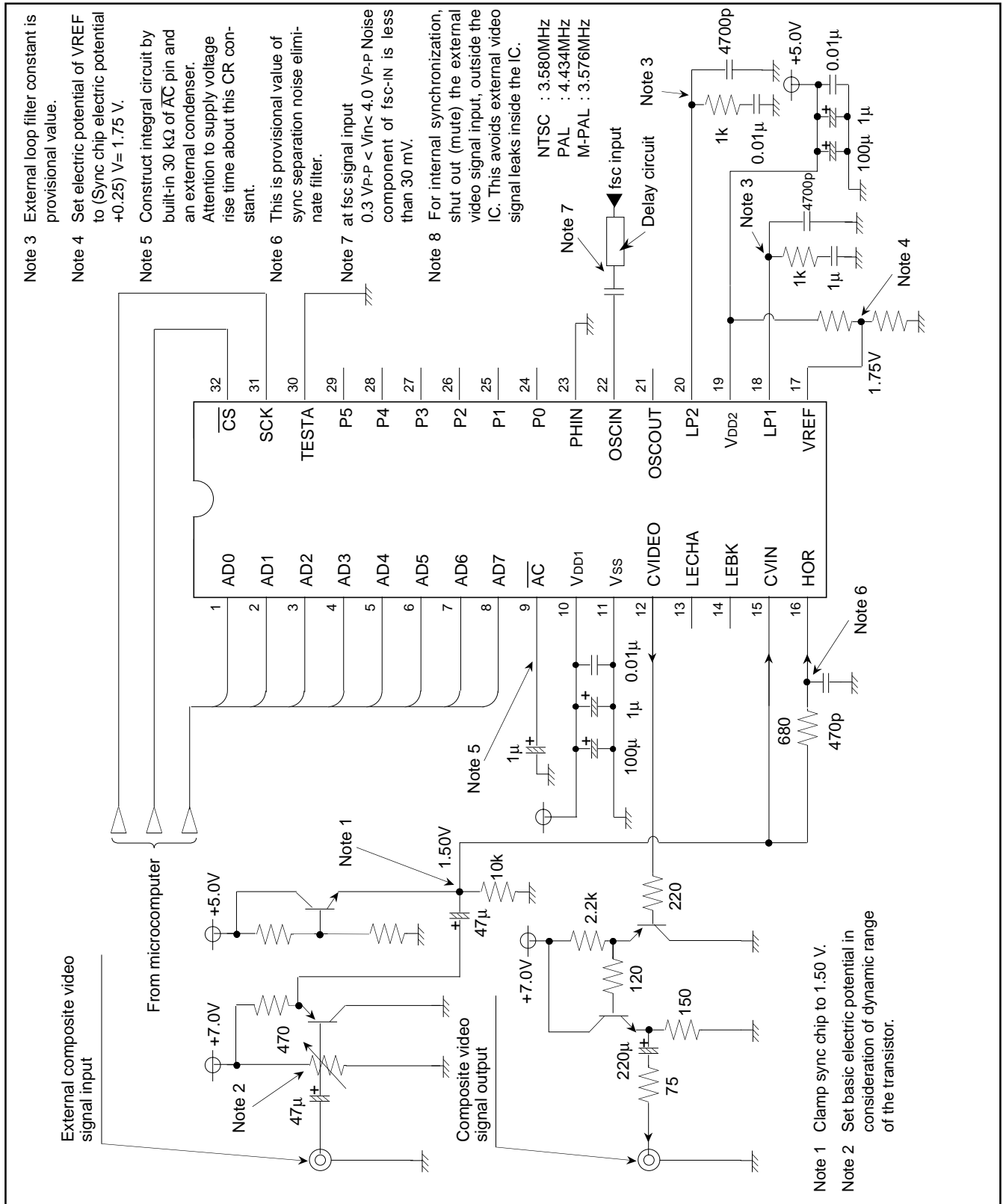


Fig.15 M35061-XXXSP/FP example of peripheral circuit

M35061-XXXSP/FP PERIPHERAL CIRCUIT (When using a crystal oscillator)

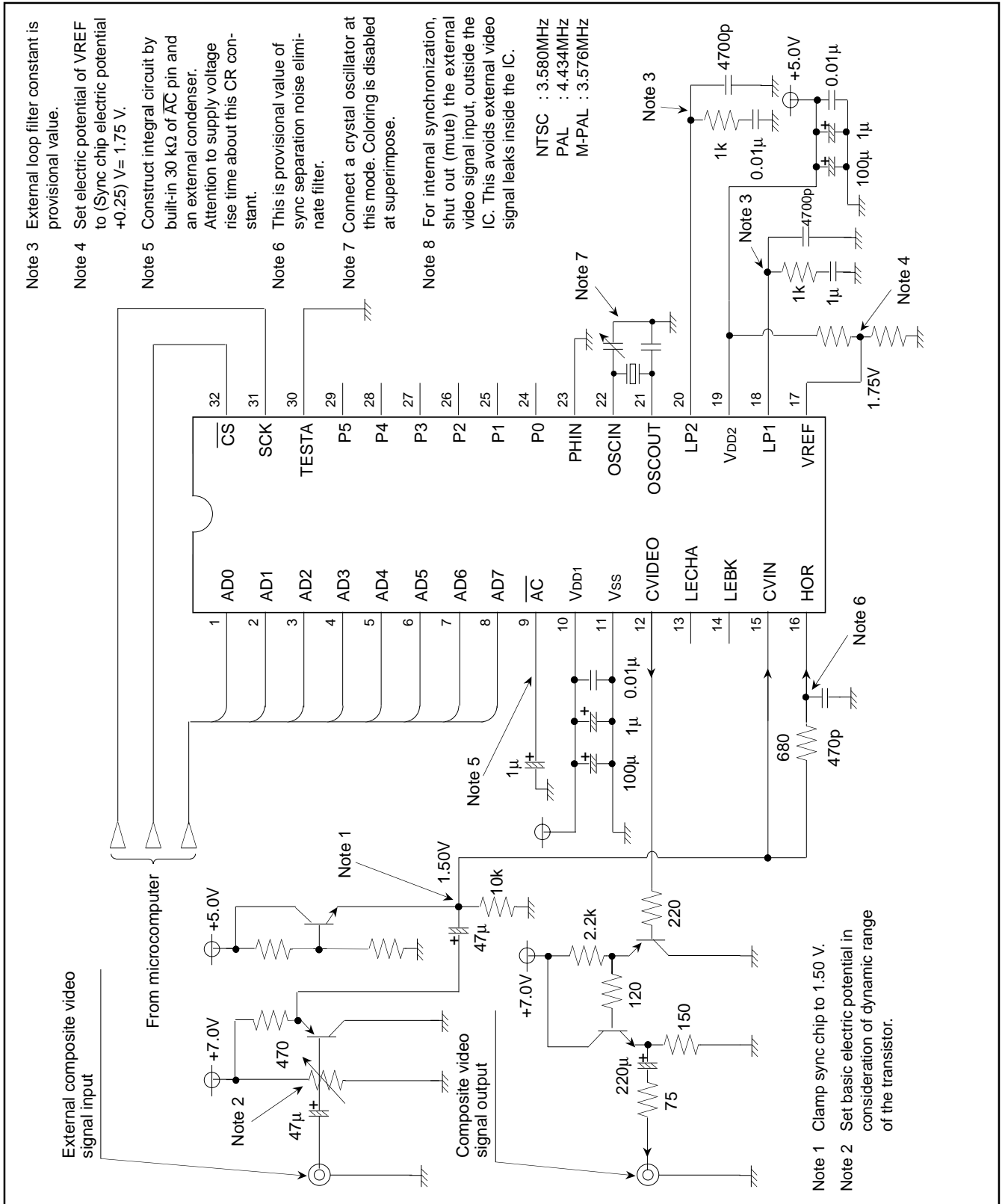


Fig.16 M35061-XXXSP/FP example of peripheral circuit

TIMING REQUIREMENTS ($T_a = -20^{\circ}\text{C}$ to $+70^{\circ}\text{C}$, $V_{DD} = 5.00 \pm 0.25\text{V}$ unless otherwise noted)

DATA INPUT

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_w(\text{SCK})$	SCK width	200	—	—	ns
$t_{su}(\overline{\text{CS}})$	$\overline{\text{CS}}$ setup time	200	—	—	ns
$t_h(\overline{\text{CS}})$	$\overline{\text{CS}}$ hold time	2	—	—	ms
$t_{su}(\text{AD})$	AD setup time	200	—	—	ns
$t_h(\text{AD})$	AD hold time	200	—	—	ns
$t_h(\text{SCK})$	1 word hold time	2	—	—	ms

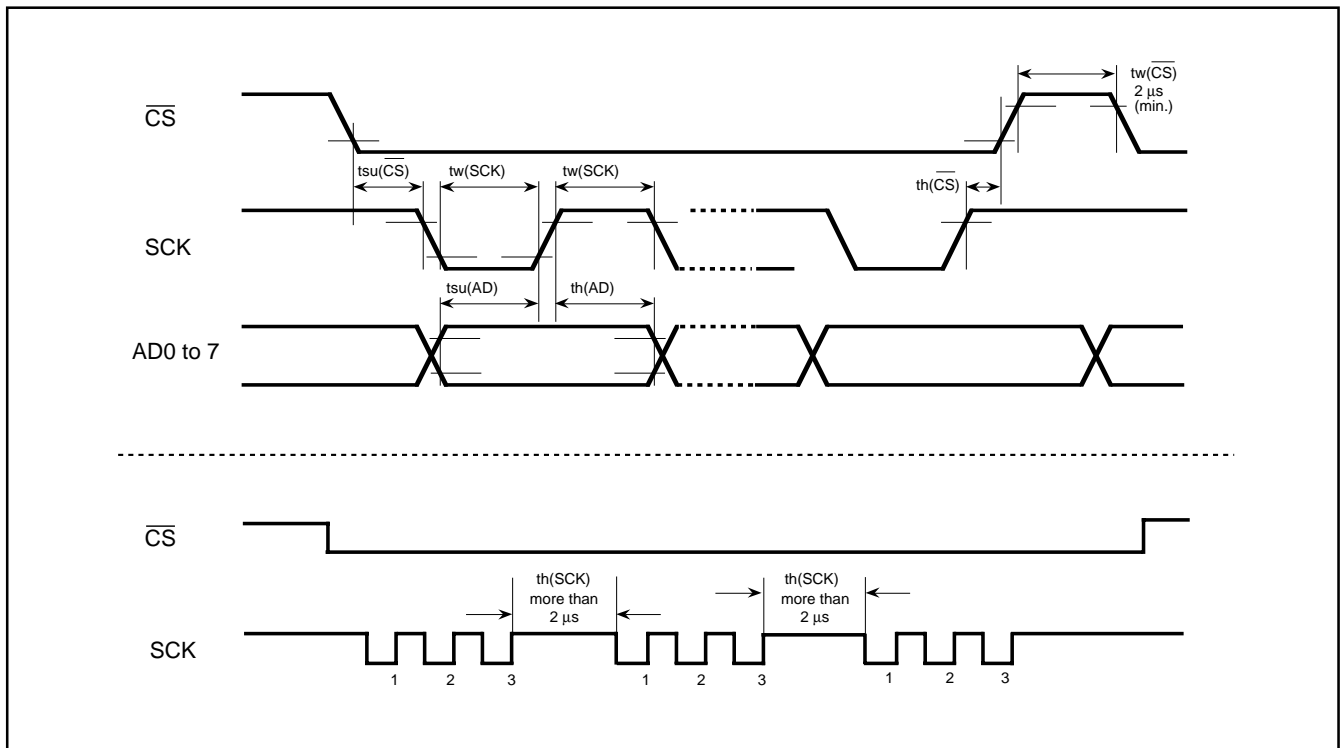


Fig. 17 Serial input timing requirements

ABSOLUTE MAXIMUM RATINGS ($V_{DD} = 5.00V$, $T_a = -20^{\circ}C$ to $+70^{\circ}C$ unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
VDD	Supply voltage	With respect to VSS.	- 0.3 to 6.0	V
Vi	Input voltage		$V_{SS} - 0.3 < V_i < V_{DD} + 0.3$	V
Vo	Output voltage		$V_{SS} < V_o < V_{DD}$	V
Pd	Power dissipation	$T_a = 25^{\circ}C$	300	mW
Topr	Operating temperature		- 20 to 70	$^{\circ}C$
Tstg	Storage temperature		- 40 to 125	$^{\circ}C$

RECOMMENDED OPERATIONAL CONDITIONS ($V_{DD} = 5.00 V$, $T_a = -20^{\circ}C$ to $+70^{\circ}C$ unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
VDD	Supply voltage	4.75	5.00	5.25	V
V _{IH}	"H" level input voltage \overline{AC} , CS, SCK, AD0 to AD7	$0.8 \times V_{DD}$	VDD	VDD	V
V _{IL}	"L" level input voltage \overline{AC} , CS, SCK, AD0 to AD7	0	0	$0.2 \times V_{DD}$	V
V _{CVIN}	Composite video input voltage CVIN	—	2 V _{P-P}	—	V
V _{OSCIN}	Input voltage OSCIN	0.3 V _{P-P}	—	4.0 V _{P-P}	V
f _{OSCIN}	Oscillation frequency for synchronous signal (Duty 40~60%)	—	3.580 4.434 3.576	—	MHz

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
VDD	Supply voltage	$T_a = -20^{\circ}C$ to $+70^{\circ}C$	4.75	5.00	5.25	V
I _{DD}	Supply current	$V_{DD} = 5.00 V$	—	25	50	mV
V _{OH}	"H" level output voltage P0 to P5	$V_{DD} = 4.75$, I _{OH} = - 0.2 mA	3.75	—	—	V
V _{OL}	"L" level output voltage P0 to P5	$V_{DD} = 4.75$, I _{OL} = 0.2 mA	—	—	0.4	V
R _I	Pull-up resistance \overline{AC}	$V_{DD} = 5.00 V$	10	30	100	k Ω

VIDEO SIGNAL INPUT CONDITIONS ($V_{DD} = 5.00 V$, $T_a = -20^{\circ}C$ to $+70^{\circ}C$)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V _{IN-CU}	Composite video signal input clamp voltage	Sync-chip voltage	—	1.5	—	V

NOTE FOR SUPPLYING POWER

(1) Timing of power supplying to \overline{AC} pin

The internal circuit of M35061-XXXSP/FP is reset when the level of the auto clear input pin \overline{AC} is "L".

This pin is hysteresis input with the pull-up resistor. The timing about power supplying of \overline{AC} pin is shown in Figure 18.

After supplying the power (V_{DD} and V_{SS}) to M35061-XXXSP/FP, the t_W time must be reserved for 1 ms or more.

Before starting input from the microcomputer, the waiting time (t_S) must be reserved for 200 ms after the supply voltage to the \overline{AC} pin becomes $0.8 \times V_{DD}$ or more.

(2) Timing of power supplying to V_{DD1} pin and V_{DD2} pin

The power need to supply to V_{DD1} and V_{DD2} at a time, though it is separated perfectly between the V_{DD1} as the digital line and the V_{DD2} as the analog line.

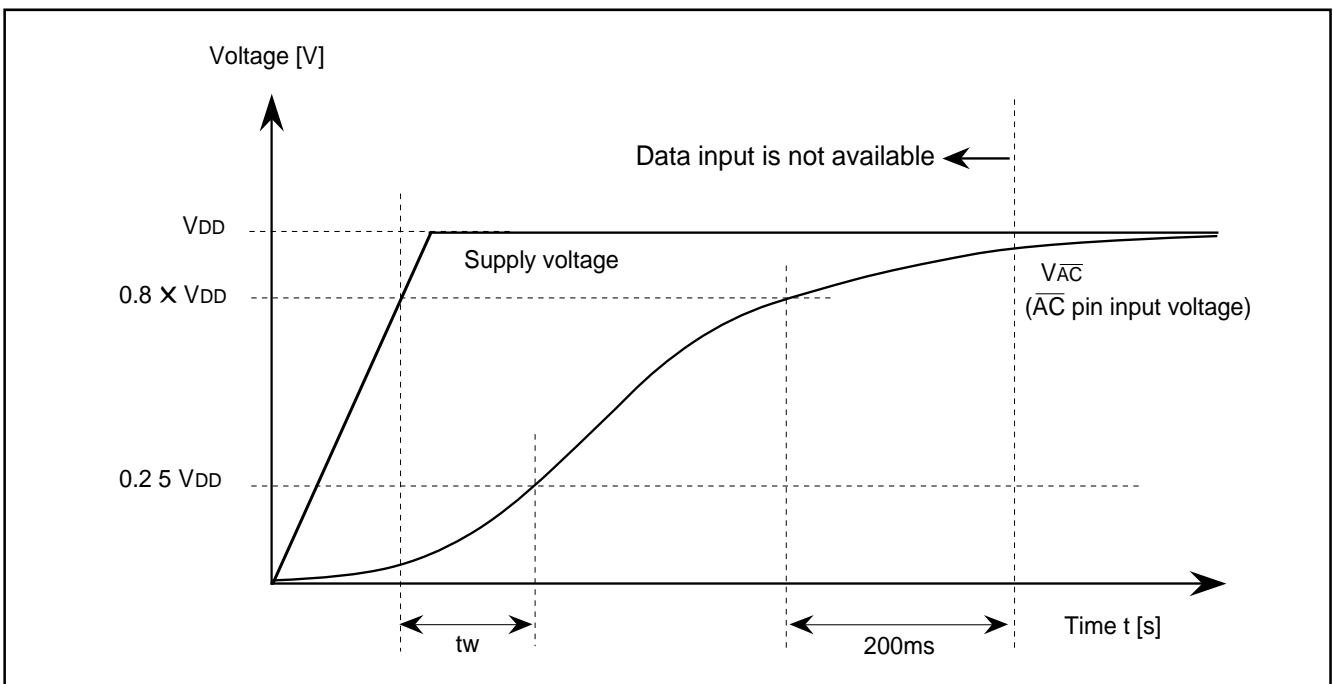


Fig. 18 Timing of power supplying to \overline{AC} pin

PRECAUTION FOR USE

Notes on noise and latch-up

In order to avoid noise and latch-up, connect a bypass capacitor (0.1 μ F) directly between the V_{DD1} pin and V_{SS} pin, and the V_{DD2} pin and V_{SS} pin using a heavy wire.

DATA REQUIRED FOR MASK ROM ORDERING

Please send the following data for mask orders.

- (1) M35061-XXXSP/FP mask ROM order confirmation form
- (2) 32P2W-A, 32P4B mask specification form
- (3) ROM data (EPROM 3 sets)
- (4) Floppy disks containing the character font generating program +character data

M35061-XXXSP/FP

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

STANDARD ROM TYPE: M35061-002SP/FP

M35061-002SP/FP is a standard ROM type of M35061-XXXSP/FP.

Character patterns are fixed to the contents of Figure 19 to 20.

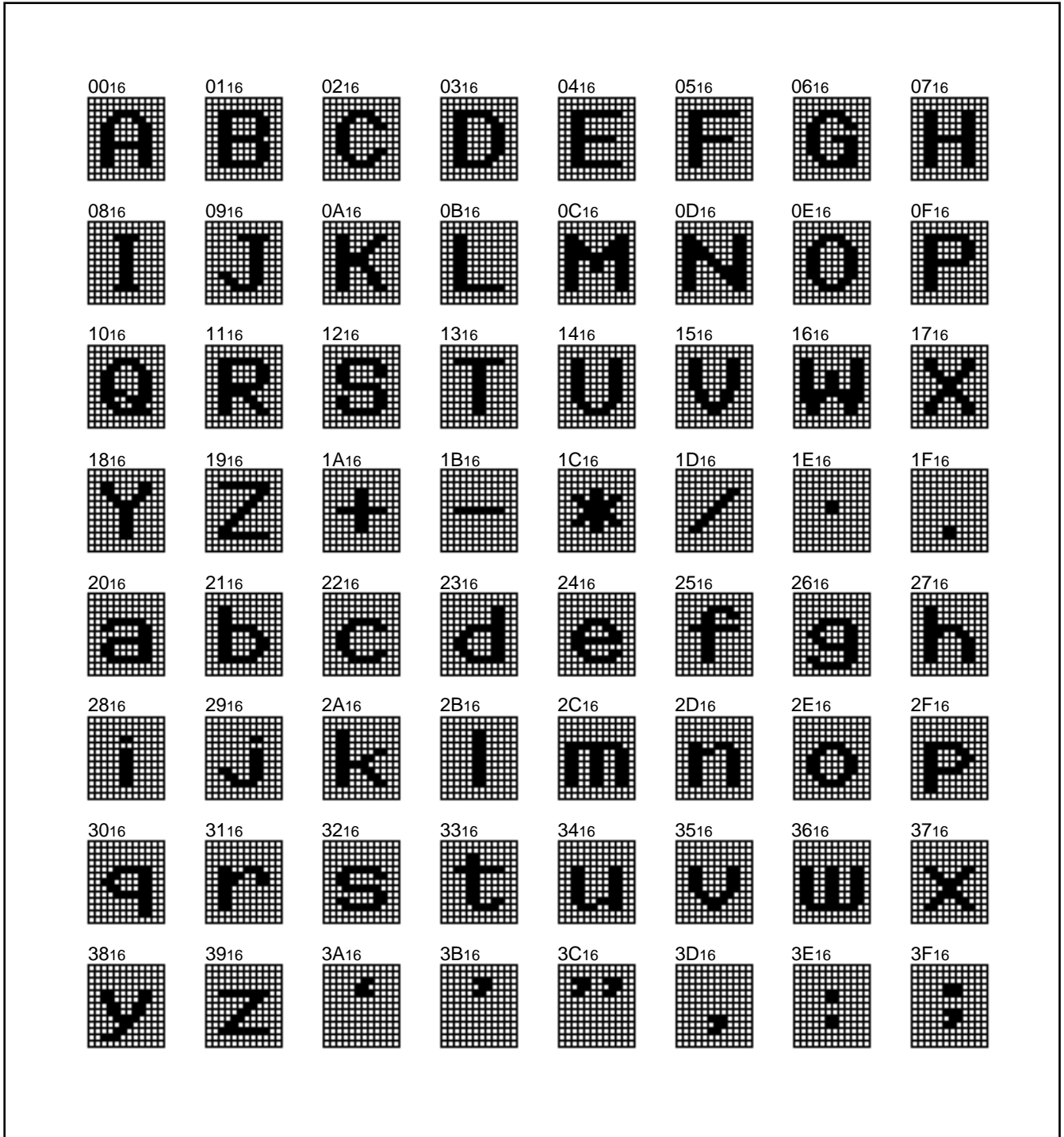


Fig. 19 M35061-002SP/FP Character patterns (1)

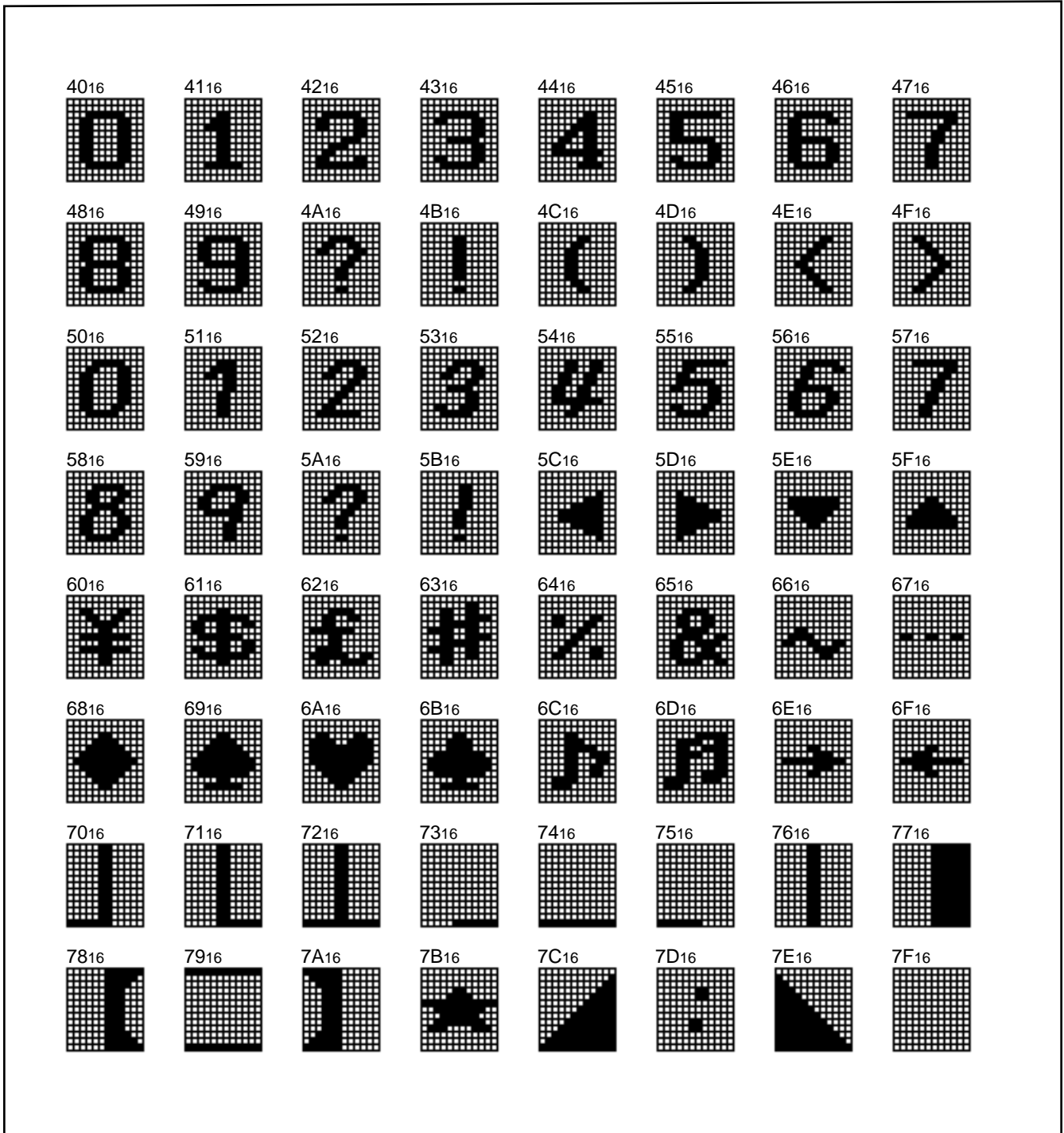


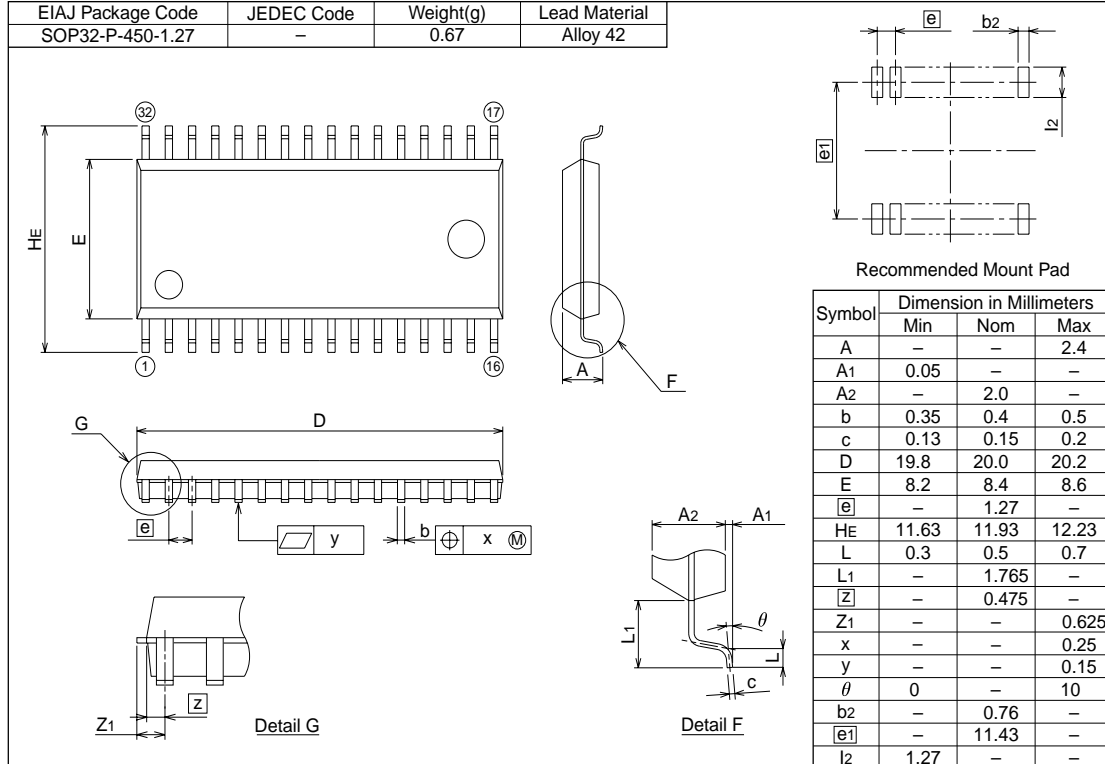
Fig. 20 M35061-002SP/FP Character patterns (2)

PACKAGE OUTLINE

32P2W-A

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
SOP32-P-450-1.27	-	0.67	Alloy 42

Plastic 32pin 450mil SOP

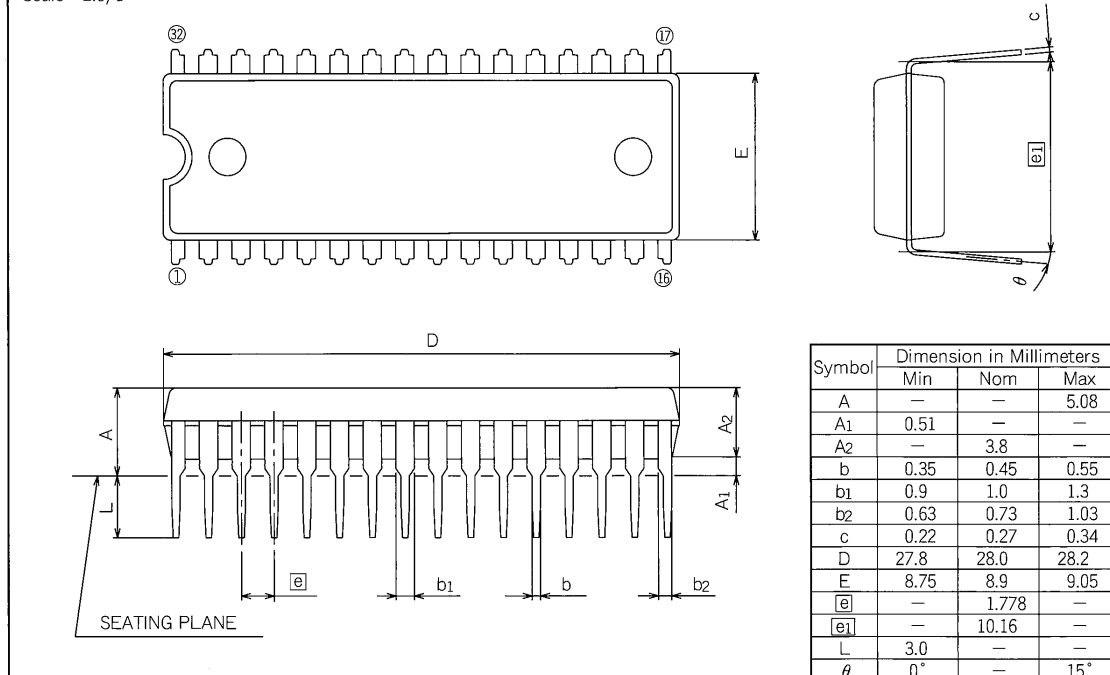


32P4B

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
SDIP32-P-400-1.78	-	2.2	Alloy 42/Cu Alloy

Plastic 32pin 400mil SDIP

Scale : 2.5/1



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REVISION DESCRIPTION LIST

M35061-XXXSP/FP DATA SHEET

Rev. No.	Revision Description	Rev. date
1.0	First Edition	9804
1.1	<ul style="list-style-type: none"> • Deletes some Japanese font and create pdf file (some pages) • P37, P38 and P39 MARK SPECIFICATION FORM and PACKAGE OUTLINE are added 	0007
1.2	Delete MARK SPECIFICATION FORM	0008
1.3	P35 Fig 19 M35061-002SP/FP character patterns(1) Address 00 ₁₆ , 01 ₁₆ 3E ₁₆ , 3F ₁₆ are added P36 Fig 20 M35061-002SP/FP character patterns(2) Address 40 ₁₆ , 41 ₁₆ 7E ₁₆ , 7F ₁₆ are added	0110