FSP34063

■ FEATURES

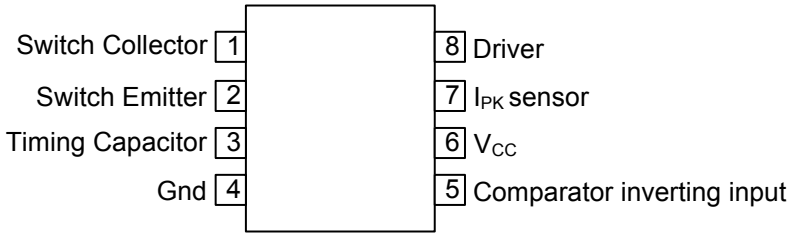
- Operation from 3.0V to 40V Input
- Low Standby Current
- Current Limiting
- Output Switch Current to 1.6A
- Output Voltage Adjustable
- Frequency Operation to 100kHz
- Precision 2% Reference
- SOP8L and PDIP8L Packages

■ GENERAL DESCRIPTION

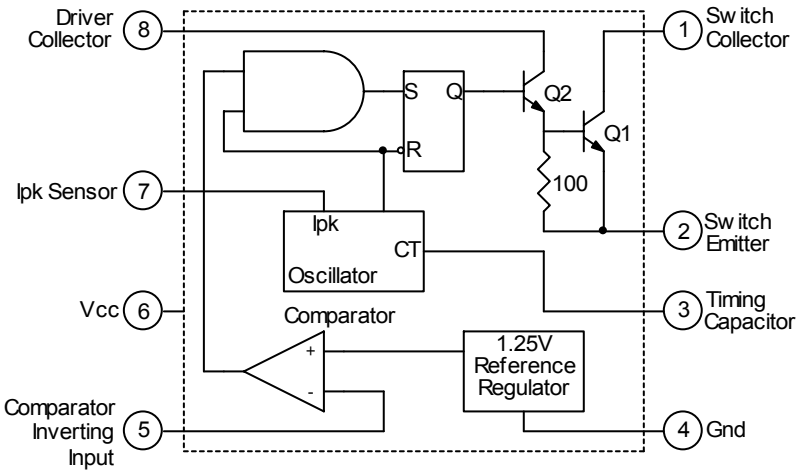
The FSP34063 Series is a monolithic control circuit containing the primary functions required for DC-to-DC converters. These devices consists of an internal temperature compensated reference, comparator, controlled duty cycle oscillator with an active current limit circuit, driver and high current output switch. This series is specifically designed for incorporating in Step-Down and Step-Up and Voltage-Inverting applications with a minimum number of external components.

■ PIN CONFIGURATION

(Top View)



■ REPRESENTATIVE SCHEMATIC DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Rating	Unit
V_{CC}	Power Supply Voltage		40	V
V_{IR}	Comparator Input Voltage Range		-0.3~+40	V
$V_{C(switch)}$	Switch Collector Voltage		40	V
$V_{E(switch)}$	Switch Emitter Voltage(VPin1=40V)		40	V
$V_{CE(switch)}$	Switch Collector to Emitter Voltage		40	V
$V_{C(driver)}$	Driver Collector Voltage		40	V
$I_{C(driver)}$	Driver Collector Current(Note1)		100	mA
I_{SW}	Switch Current		1.6	A
P_D	Power Dissipation and Thermal Characteristics	SOP8L: T_A=25℃	600	mW
θ_{JA}		Thermal Resistance	160	℃/W
P_D		PDIP8L: T_A=25℃	1.25	W
θ_{JA}		Thermal Resistance	100	℃/W
T_J	Operating Junction Temperature		+150	℃
T_A	Operating Ambient Temperature Range		0~+70 -40~+85	℃
Tstg	Storage Temperature Range		-65~+150	℃

Notes: 1.Maximum package power dissipation limits must be observed.
2.ESD data available upon request.

■ ELECTRICAL CHARACTERISTICS(V_{CC}=5V, UNLESS OTHERWISE NOTED)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Oscillator section						
fosc	Frequency	VPin 5=0V, C_T=1.0nF, T_A=25℃	24	33	42	kHz
Ichg	Charge Current	V_{CC}=5.0V to 40V, T_A=25℃	24	30	42	μA
Idischg	Discharge Current	V_{CC}=5.0V to 40V, T_A=25℃	140	200	260	μA
Idischg/Ichg	Discharge to Charge Current Ratio	Pin7 to Vcc, T_A=25℃	5.2	6.5	7.5	
Vipk(sense)	Current Limit Sense Voltage	Ichg=Idischg, T_A=25℃	300	400	450	mV
Output switch section						
$V_{CE(sat)}$	Saturation Voltage, Darlington Connection	I_{SW}=1.0A, Pins 1,8 connected		1.0	1.3	V
$V_{CE(sat)}$	Saturation Voltage, Darlington Connection	I_{SW}=1.0A, I_D=50mA, Forced β120		0.45	0.7	V
hFE	DC Current Gain	I_{SW}=1.0A, V_{CE}=5.0V, T_A=25℃	50	75		
$I_{C(off)}$	Collector Off-State Current	V_{CE}=40V		0.01	100	μA
Comparator section						
Vth	Threshold Voltage	T_A=25℃ T=0℃~75℃	1.225 1.21	1.25	1.275 1.29	V
Reg(line)	Threshold Voltage Line Regulation	V_{CC}=3.0V to 40V		1.4	6.0	mV
Total device						
I_{CC}	Supply Current	V_{CC}=5.0V to 40V, C_T=1.0nF, Pin7=V_{CC}, VPin5＞Vth, Pin2=Gnd, remaining pins open			3.5	mA

Note: 3.Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient temperature as possible.
4.If the output switch is driven into hard saturation(non-Darlington configuration) at low switch currents(≤300mA) and high driver currents(≥30mA), it may take up to 2.0μs for it to come out of saturation. This condition will shorten the off time at frequencies≥30kHz, and is magnified at high temperatures. This condition does not occur with a Darlington configuration, since the output switch cannot saturate. If a non-Darlington configuration is

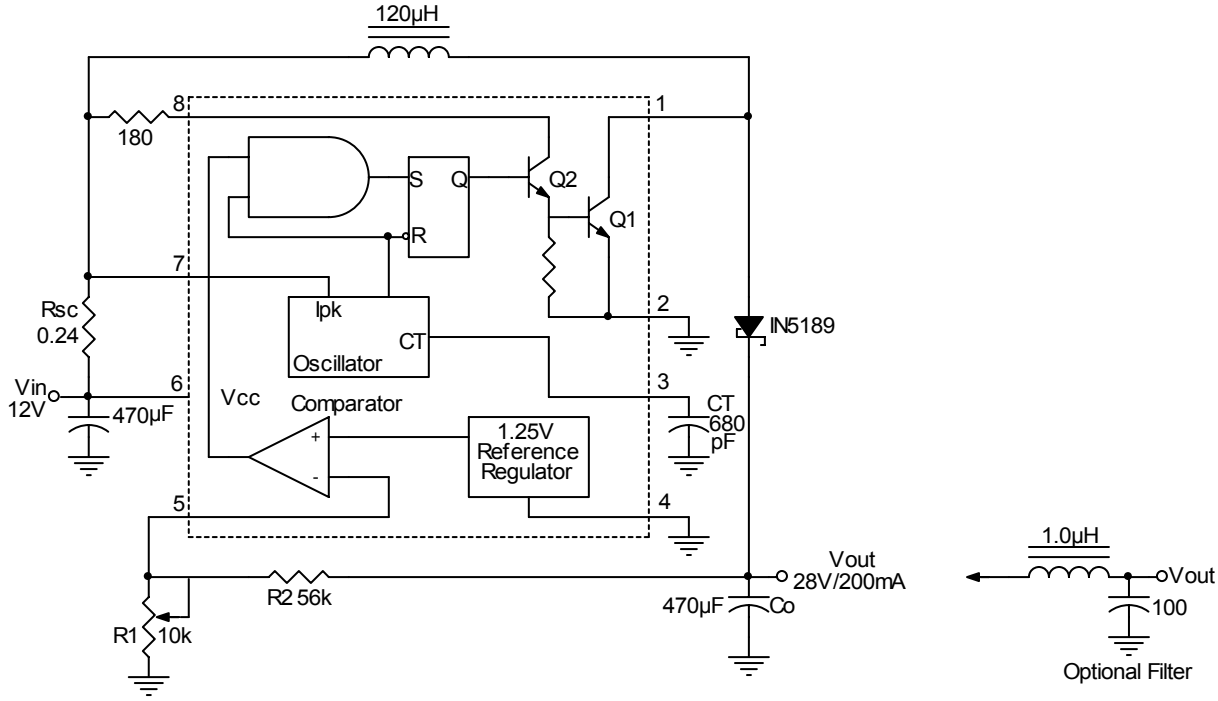
used, the following output drive condition is recommended:

Forced β of output switch: $\frac{I_C output}{I_C driver - 7.0mA^*} \geq 10$

*The 100Ω resistor in the emitter of the driver device requires about 7.0mA before the output switch conducts.

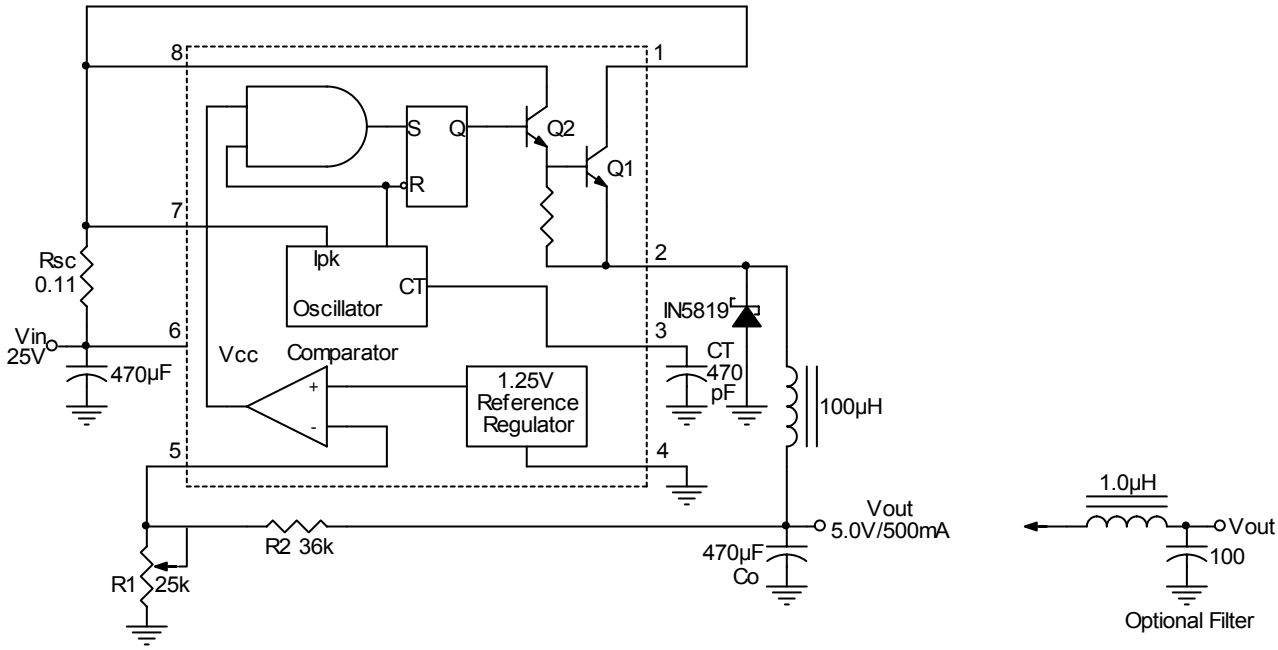
■ APPLICATION CIRCUITS

(1) Step-Up Converter



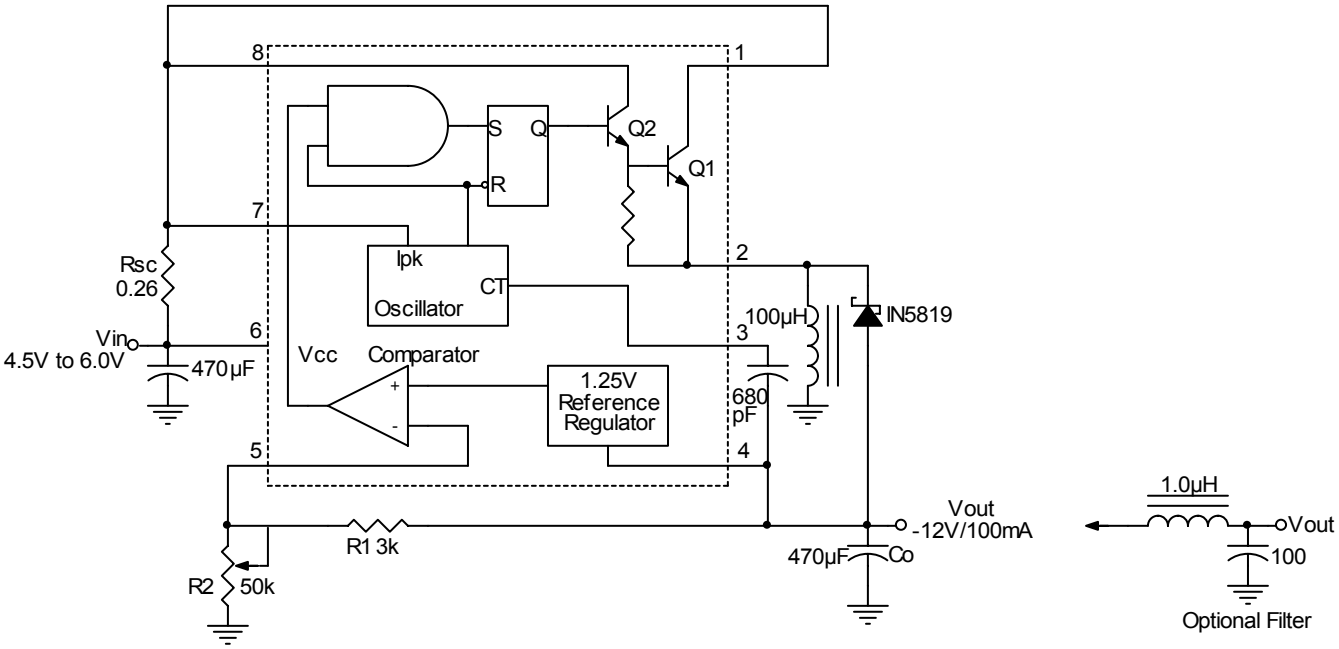
Test	Conditions	Results
Line Regulation	Vin=9V to 12V, I_O=200mA	20mV=0.035%
Load Regulation	Vin=12V, I_O=50mA to 200mA	15mV=0.035%
Output Ripple	Vin=12V, I_O=200mA	500mVPP
Efficiency	Vin=12V, I_O=200mA	80%

(2) Step-Down Converter



Test	Conditions	Results
Line Regulation	Vin=12V to 24V, I_O=500mA	20mV=0.2%
Load Regulation	Vin=24V, I_O=50mA to 500mA	5mV=0.05%
Output Ripple	Vin=24V, I_O=500mA	160mVPP
Efficiency	Vin=24V, I_O=500mA	82%

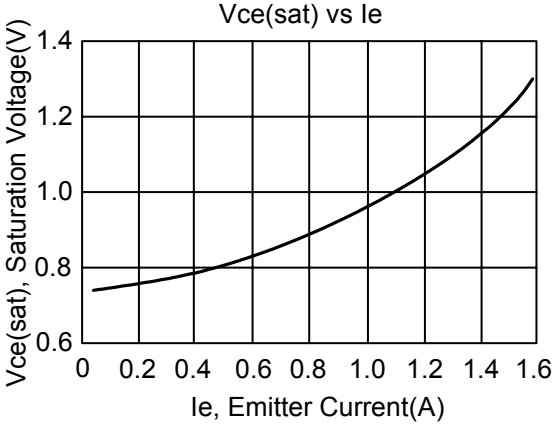
(3) Voltage Inverting Converter



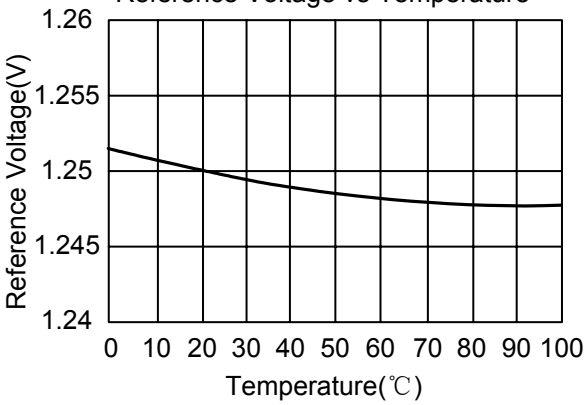
Test	Conditions	Results
Line Regulation	Vin=4.5V to 6.0V, I_O=100mA	20mV=0.08%
Load Regulation	Vin=5.0V, I_O=20mA to 100mA	30mV=0.12%
Output Ripple	Vin=5.0V, I_O=100mA	500mVPP
Efficiency	Vin=5.0V, I_O=100mA	60%

■ TYPICAL CHARACTERISTICS

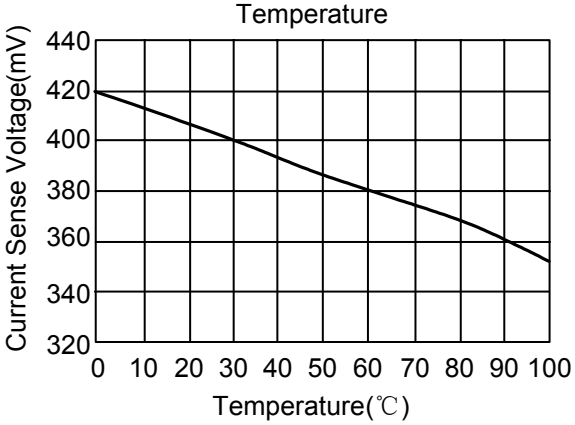
Vce(sat) vs Ie



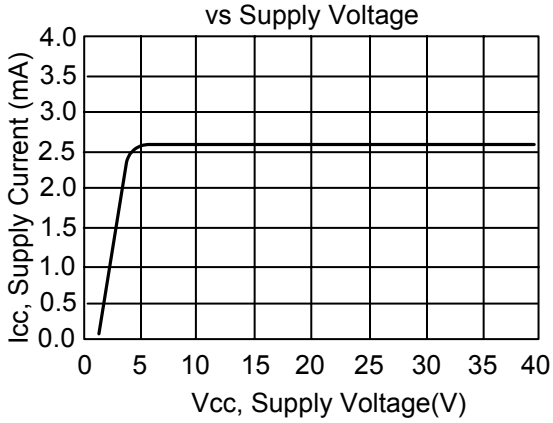
Reference Voltage vs Temperature



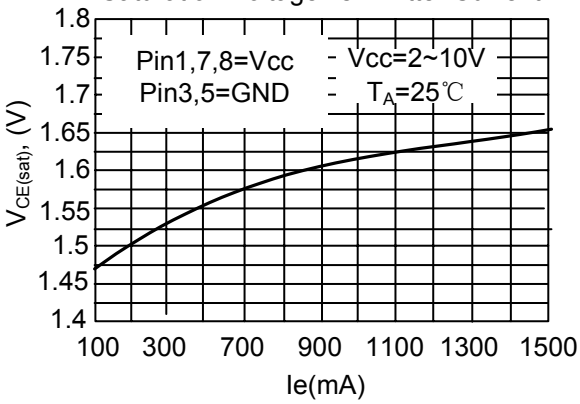
Current Sense Voltage vs Temperature



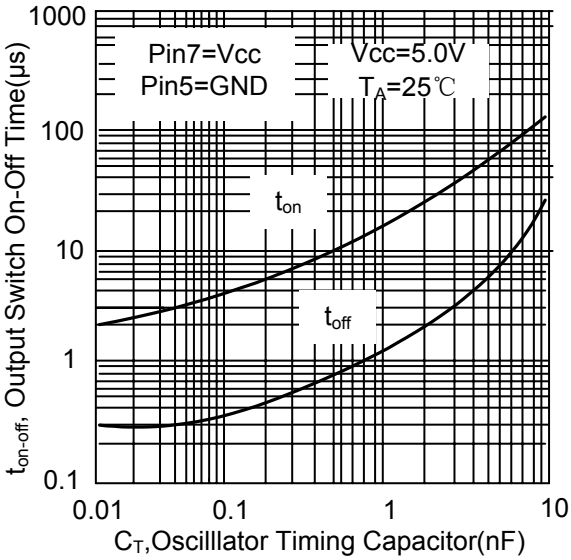
Standby Supply Current vs Supply Voltage



Emitter Follower Configuration Output Saturation Voltage vs Emitter Current



Output Switch On-Off Time vs Oscillator Timing Capacitor



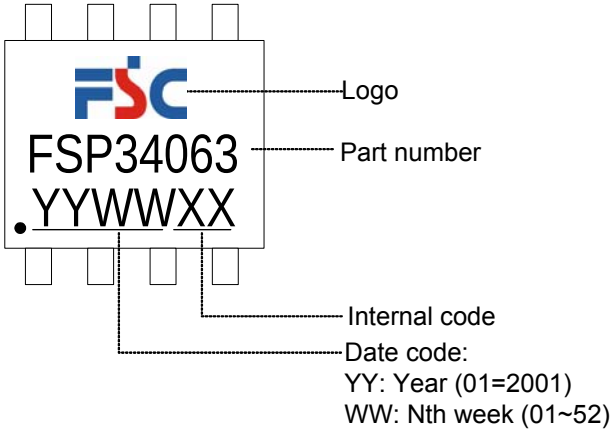
■ ORDERING INFORMATION

FSP34063XXX

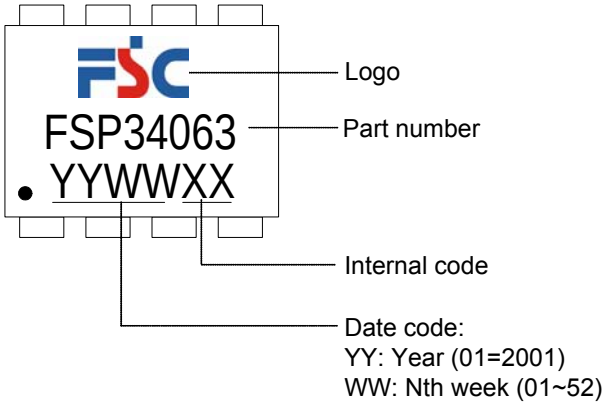
Package:	Packing:	Temperature Grade:
S: SOP8L	Blank: Tube or Bulk	Blank: 0~70℃
N: PDIP8L	A: Tape & Reel	D:-40~85℃

■ MARKING INFORMATION

(1) SOP8L

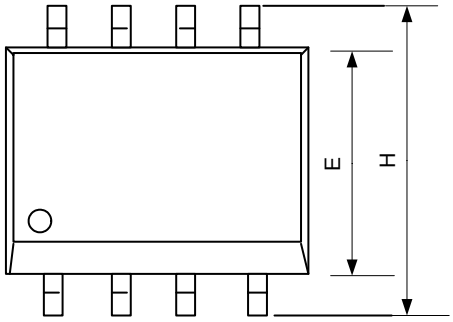


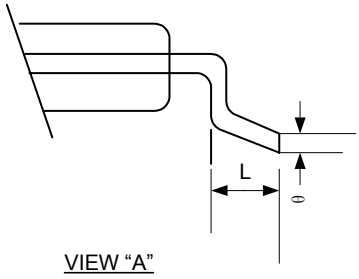
(2) PDIP8L

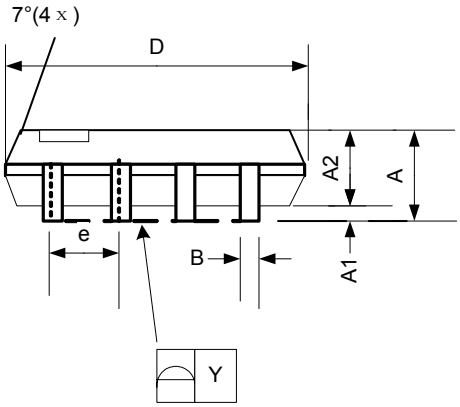


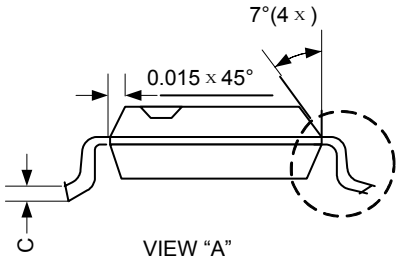
■ PACKAGE INFORMATION

(1) SOP8L



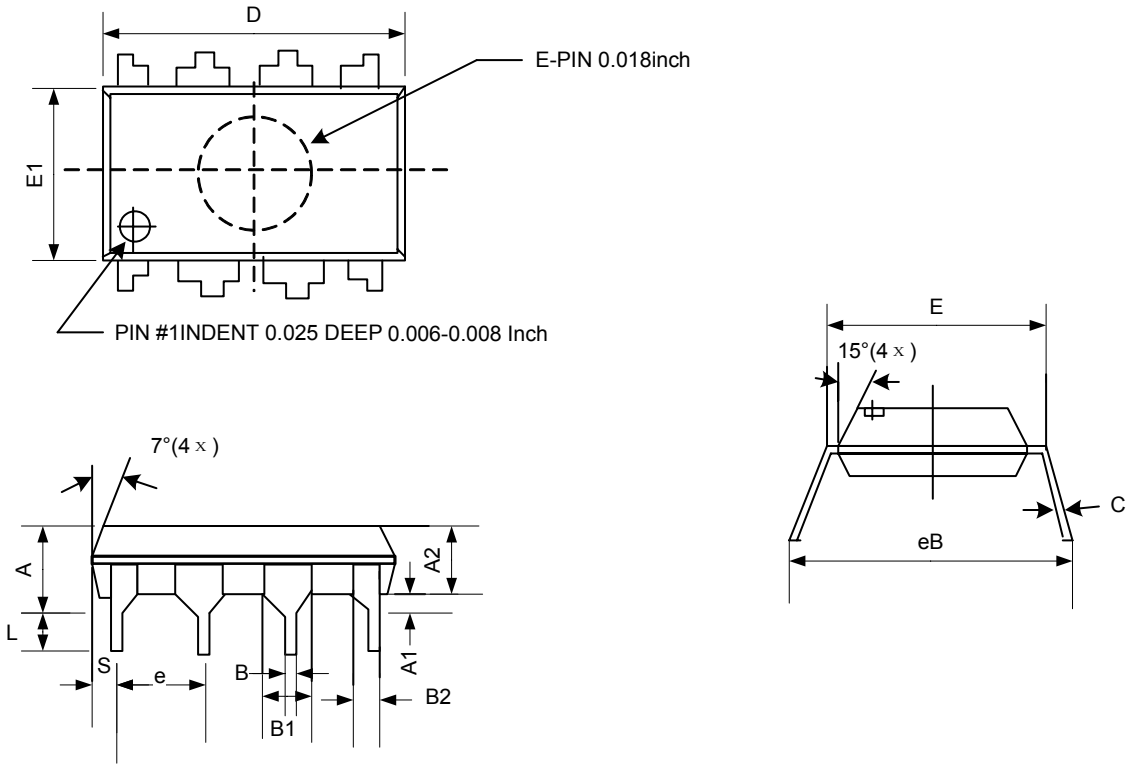






Symbol	Dimensions In Millimeters			Dimensions In Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	1.40	1.60	1.75	0.055	0.063	0.069
A1	0.10		0.25	0..004		0.010
A2	1.30	1.45	1.50	0.051	0.057	0.059
B	0.33	0.41	0.51	0.013	0.016	0.020
C	0.19	0.20	0.25	0.0075	0.008	0.010
D	4.80	5.05	5.30	0.189	0.199	0.209
E	3.70	3.90	4.10	0.146	0.154	0.161
e		1.27			0.050	
H	5.79	5.99	6.20	0.228	0.236	0.244
L	0.38	0.71	1.27	0.015	0.028	0.050
Y			0.10			0.004
θ	0°		8°	0°		8°

(2) PDIP8L



Symbol	Dimensions In Millimeters			Dimensions In Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A			5.33			0.210
A1	0.38			0.015		
A2	3.1	3.30	3.5	0.122	0.130	0.138
B	0.36	0.46	0.56	0.014	0.018	0.022
B1	1.4	1.52	1.65	0.055	0.060	0.065
B2	0.81	0.99	1.14	0.032	0.039	0.045
C	0.20	0.25	0.36	0.008	0.010	0.014
D	9.02	9.27	9.53	0.335	0.365	0.375
E	7.62	7.94	8.26	0.300	0.313	0.325
E1	6.15	6.35	6.55	0.242	0.250	0.258
e		2.54			0.100	
L	2.92	3.3	3.81	0.115	0.130	0.150
eB	8.38	8.89	9.40	0.330	0.350	0.370
S	0.71	0.84	0.97	0.028	0.033	0.038

■ DESIGN FORMULA TABLE

Calculation	Step-Up	Step-Down	Voltage-Inverting
t_{on}/t_{off}	$\frac{V_{OUT}+V_F-V_{in(\min)}}{V_{in(\min)}-V_{sat}}$	$\frac{V_{OUT}+V_F}{V_{in(\min)}-V_{sat}-V_{OUT}}$	$\frac{\lvert V_{OUT}\rvert+V_F}{V_{in}-V_{sat}}$
$(t_{on}+t_{off})$	1/f	1/f	1/f
t_{off}	$\frac{t_{on}+t_{off}}{\frac{t_{on}}{t_{off}}+1}$	$\frac{t_{on}+t_{off}}{\frac{t_{on}}{t_{off}}+1}$	$\frac{t_{on}+t_{off}}{\frac{t_{on}}{t_{off}}+1}$
t_{on}	$(t_{on}+t_{off})-t_{off}$	$(t_{on}+t_{off})-t_{off}$	$(t_{on}+t_{off})-t_{off}$
C_T	$4.0\times10^{-5}t_{on}$	$4.0\times10^{-5}t_{on}$	$4.0\times10^{-5}t_{on}$
$I_{PK(switch)}$	$2I_{out(\max)}(t_{on}/t_{off}+1)$	$2I_{out(\max)}$	$2I_{out(\max)}(t_{on}/t_{off}+1)$
R_{SC}	$0.3/I_{PK(switch)}$	$0.3/I_{PK(switch)}$	$0.3/I_{PK(switch)}$
$L_{(min)}$	$\frac{V_{in(\min)}-V_{sat}}{I_{pk(switch)}}t_{on(\max)}$	$\frac{V_{in(\min)}-V_{sat}-V_{out}}{I_{pk(switch)}}t_{on(\max)}$	$\frac{V_{in(\min)}-V_{sat}}{I_{pk(switch)}}t_{on(\max)}$
Co	$9\frac{I_{out}t_{on}}{V_{ripple(pp)}}$	$\frac{I_{pk(switch)}(t_{off}+t_{on})}{8V_{ripple(pp)}}$	$9\frac{I_{out}t_{on}}{V_{ripple(pp)}}$

Vsat=Saturation voltage of the output switch.
VF=Forward voltage drop of the output rectifier.

The following power supply characteristics must be chosen:
Vin-Norminal input voltage
Vout-Desired output voltage, |vout|=1.25(1+ R2/R1)
Iout-Desired output current
fmin-Minimum desired output switching frequency at the selected values of Vin and Io
Vripple(pp)-Desired peak-to-peak output ripple voltage, In practice, the calculated capacitor value will need to be increased due to its equivalent series resistance and board layout. The ripple voltage should be kept to a low value since it will directly affect the line and load regulation.