



## FSUSB22 — Low-Power, 2-Port, High-Speed USB 2.0 (480Mbps) Switch

### Features

- -40dB Off Isolation at 250MHz
- -40dB Non-adjacent Channel Crosstalk at 250MHz
- On Resistance: 4.5Ω Typical (R<sub>ON</sub>)
- -3dB Bandwidth: 750MHz
- Low-Power Consumption: 1μA Maximum
- Control Input: TTL Compatible
- Bi-directional Operation
- USB High-Speed and Full-Speed Signaling Capability

### Description


FSUSB22 is a low-power, high-bandwidth switch specially designed for applications switching high-speed USB 2.0 signals in handset and consumer applications; such as cell phone, digital camera, and notebook with hubs or controllers of limited USB I/O. The wide bandwidth (750MHz) allows signals to pass with minimum edge and phase distortion. Superior channel-to-channel crosstalk results in minimal interference. It is compatible with the USB2.0 Hi-Speed standard.

### Applications

- Cell Phones, PDAs, Digital Cameras, Notebook Computers

### Ordering Information

Part Number	Operating Temperature Range	Package	Packing Method
FSUSB22BQX	-40 to +85°C	16-Terminal Depopulated Quad Very-Thin Flat Pack No Leads (DQFN), JEDEC MO-241, 2.5 x 3.5mm	Tape and Reel
FSUSB22QSC	-40 to +85°C	16-Lead Quarter Size Outline Package (QSOP), JEDEC MO-137, 0.150-inch Wide	Tube
FSUSB22QSCX	-40 to +85°C	16-Lead Quarter Size Outline Package (QSOP), JEDEC MO-137, 0.150-inch Wide	Tape and Reel
FSUSB22MTC	-40 to +85°C	16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide	Tube
FSUSB22MTCX	-40 to +85°C	16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide	Tape and Reel

 All packages are lead free per JEDEC: J-STD-020B standard.

### Logic Diagram

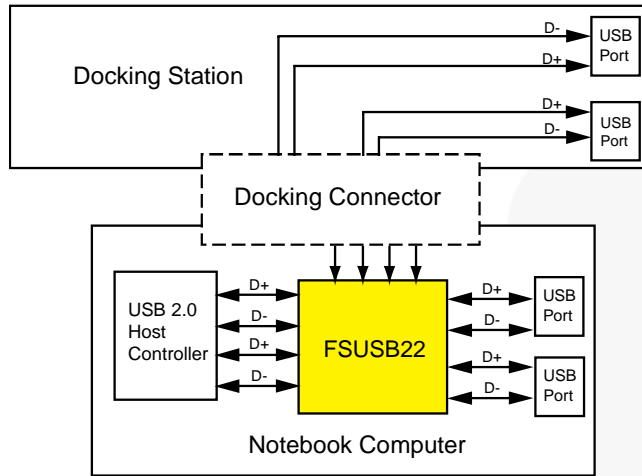


Figure 1. Logic Diagram

### Analog Symbol

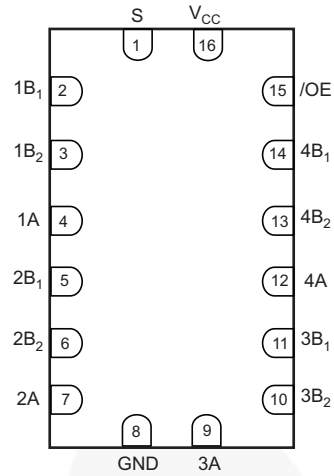


Figure 2. Analog Symbol

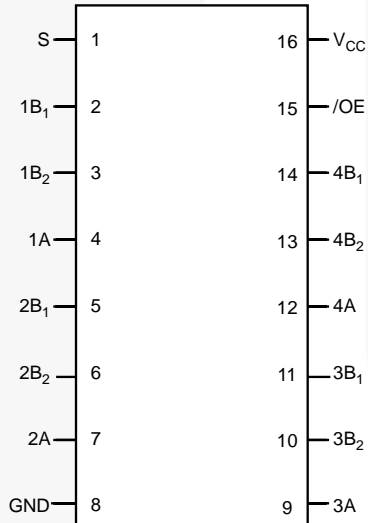


Figure 3. QSOPT and TSSOP Pin Configuration

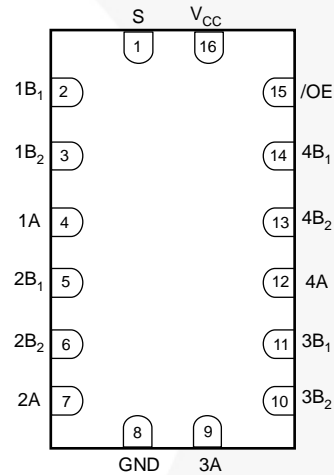


Figure 4. Pad Assignment for DQFN

### Pin Descriptions

Pin #	Pin Names	Description
1	S	Select Input
2,3,5,6,10,11,13,14	1B <sub>1</sub> ,1B <sub>2</sub> , 2B <sub>1</sub> ,2B <sub>2</sub> ,3B <sub>2</sub> ,3B <sub>1</sub> ,4B <sub>2</sub> ,4B <sub>1</sub>	Bus B
8	GND	Ground
4,7,9,12	1A,2A,3A,4A	Bus A
15	/OE	Bus Switch Enable
16	V <sub>CC</sub>	Supply Voltage

### Truth Table

S	OE	Function
Don't Care	HIGH	Disconnect
LOW	LOW	A=B <sub>1</sub>
HIGH	LOW	A=B <sub>2</sub>

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min.	Max.	Unit
$V_{CC}$	Supply Voltage	-0.5	4.6	V
$V_S$	DC Switch Voltage	-0.5	$V_{CC} + 0.05$	V
$V_{IN}$	DC Input Voltage <sup>(1)</sup>	-0.5	4.6	V
$I_{IK}$	DC Input Diode Current, $V_{IN} < 0V$		-50	mA
$I_{OUT}$	DC Output Sink Current		128	mA
$I_{CC} / I_{GND}$	DC $V_{CC}$ / GND Current		$\pm 100$	mA
$T_{STG}$	Storage Temperature Range	-65	+150	°C
ESD	Human Body Model, JESD22-A114		4	kV

### Note:

- The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

## Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter		Min.	Max.	Unit
$V_{CC}$	Power Supply Operating		3.0	3.6	V
$V_{IN}$	Input Voltage		0	$V_{CC}$	V
$V_{OUT}$	Output Voltage		0	$V_{CC}$	V
$t_r, t_f$	Input Rise and Fall Time	Switch Control Input <sup>(2)</sup>	0	5	ns/V
		Switch I/O	0	DC	
$T_A$	Operating Temperature, Free Air		-40	+85	°C

### Note:

- Unused control inputs must be held HIGH or LOW. They may not float.

## DC Electrical Characteristics

Typical values are at  $V_{CC} = 3.0V$  and  $T_A = 25^\circ C$ .

Symbol	Parameter	Conditions	$V_{CC}$ (V)	$T_A = -40$ to $+85^\circ C$			Units
				Min.	Typ.	Max.	
$V_{IK}$	Clamp Diode Voltage	$I_{IN} = -18mA$	3.0			-1.2	V
$V_{IH}$	High-Level Input Voltage		3.0 to 3.6	2.0			V
$V_{IL}$	Low-Level Input Voltage		3.0 to 3.6			0.8	V
$I_{IN}$	Input Leakage Current	$0 \leq V_{IN} \leq 3.6V$	3.6			$\pm 1.0$	$\mu A$
$I_{OFF}$	Off-state Leakage Current	$0 \leq A, B \leq V_{CC}$	3.6			$\pm 1.0$	$\mu A$
$R_{ON}$	Switch On Resistance <sup>(3)</sup>	$V_{IN} = 0.8V, I_{ON} = 8mA$	3.0		5	7	$\Omega$
		$V_{IN} = 3.0V, I_{ON} = 8mA$	3.0		4.5	6.5	
$\Delta R_{ON}$	Delta $R_{ON}$	$V_{IN} = 0.8V, V_{IN} = 0V - 1.5, I_{ON} = 8mA$	3.0		0.3		$\Omega$
$R_{FLAT(ON)}$	On Resistance Flatness <sup>(4)</sup>	$I_{OUT} = 8mA$	3.0		1		$\Omega$
$I_{CC}$	Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND, $I_{OUT} = 0$	3.6			1	$\mu A$

### Notes:

- Measured by the voltage drop between the A and B pins at the indicated current through the switch. On resistance is determined by the lower of the voltages on the A or B pins.
- Flatness is defines as the difference between the maximum and the minimum value on resistance over the specified range of conditions.

## AC Electrical Characteristics

Typical values are at  $V_{CC} = 3.0V$  and  $T_A = 25^\circ C$ .

Symbol	Parameter	Conditions	$V_{CC}(V)$	Min.	Typ.	Max.	Units	Figure
$t_{ON}$	Turn-on Time S-to-Bus B		3.0 to 3.6		4.5	6.0	ns	Figure 9 Figure 10
$t_{OFF}$	Turn-off Time S-to-Bus B		3.0 to 3.6		2.5	4.0	ns	Figure 9 Figure 10
$t_{PD}$	Propagation Delay	$C_L = 10pF$	3.0 to 3.6		0.25		ns	Figure 14
$O_{IRR}$	Non-Adjacent Off Isolation	$f = 250MHz,$ $R_L = 50\Omega$	3.0 to 3.6		-30		dB	Figure 11
$X_{TALK}$	Non-Adjacent Channel Crosstalk	$f = 250MHz,$ $R_L = 50\Omega$	3.0 to 3.6		-38		dB	Figure 12
BW	-3dB Bandwidth	$R_L = 50\Omega$	3.0 to 3.6		750		MHz	Figure 13

## USB Related AC Electrical Characteristics

Typical values are at  $V_{CC} = 3.0V$  and  $T_A = 25^\circ C$ .

Symbol	Parameter	Conditions	$V_{CC} (V)$	Min.	Typ.	Max.	Units	Figure
$t_{SK(O)}$	Channel-to Channels Skew	$C_L = 10pF$	3.0 to 3.6		0.051		pF	Figure 14 Figure 16
$t_{SK(P)}$	Skew of Opposite Transition of the Same Output	$C_L = 10pF$	3.0 to 3.6		0.020		pF	Figure 14 Figure 16
$T_J$	Total Jitter	$R_L = 50\Omega,$ $C_L = 10pF$ $t_R = t_F = 750ps$ at 480MPs	3.0 to 3.6		0.210			

## Capacitance

Typical values are at  $V_{CC} = 3.0V$  and  $T_A = 25^\circ C$ .

Symbol	Parameter	Conditions	Typ.	Units
$C_{IN}$	Control Pin Input Capacitance	$V_{CC} = 0V$	2.5	pF
$C_{ON}$	A/B On Capacitance	$V_{CC} = 3.3V, /OE = 0V$	12	pF
$C_{OFF}$	Port B Off Capacitance	$V_{CC}$ and $/OE = 3.3V$	4.5	pF

## Performance Characteristics

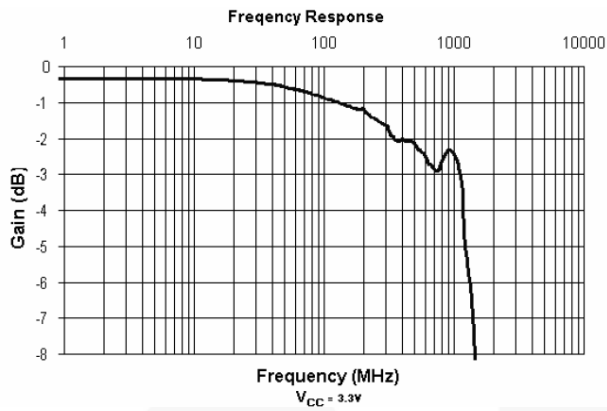


Figure 5. Gain vs. Frequency

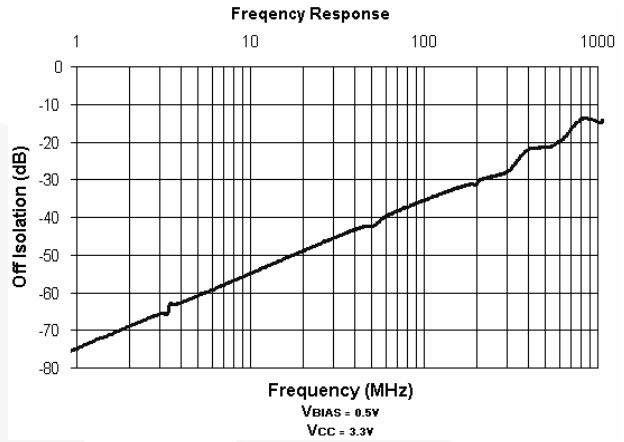


Figure 6. Off Isolation

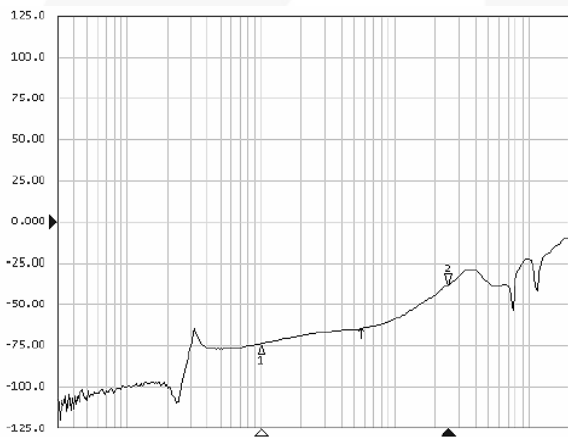


Figure 7. Crosstalk

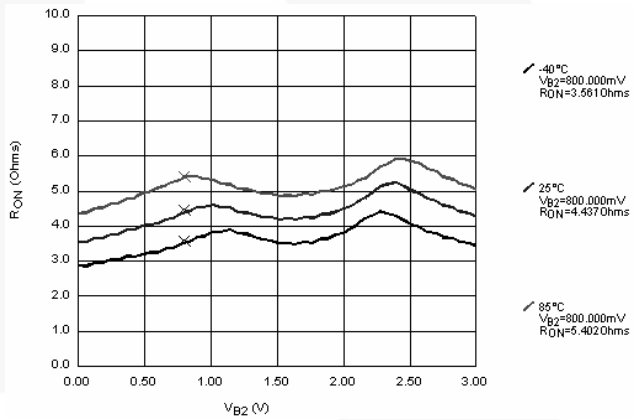
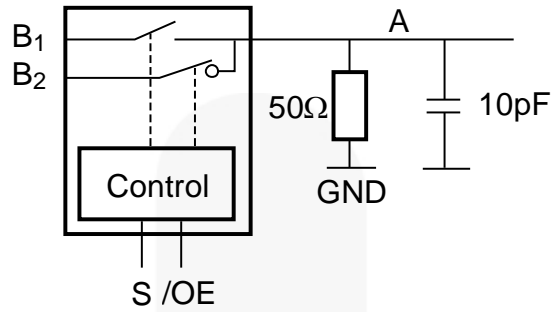


Figure 8. RON

## AC Loadings and Waveforms



Notes: Input driven by 50Ω source terminated in 50Ω.  
 CL includes load and stray capacitance.  
 Input PRR-1.0MHz,  $t_w = 500\text{ns}$ .

Figure 9. AC Test Circuit

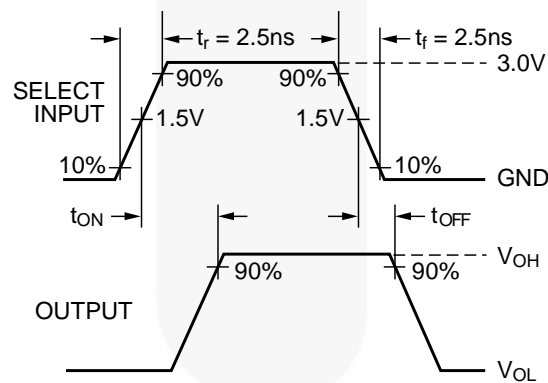


Figure 10. AC Waveforms

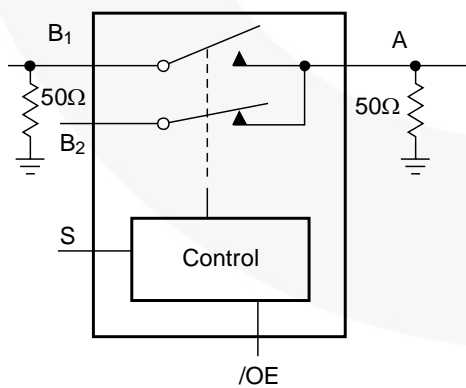


Figure 11. Off Isolation Test

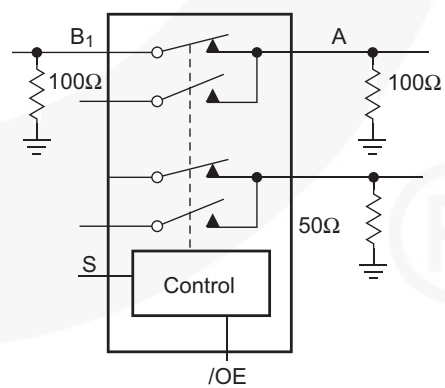


Figure 12. Crosstalk Test

AC Loadings and Waveforms

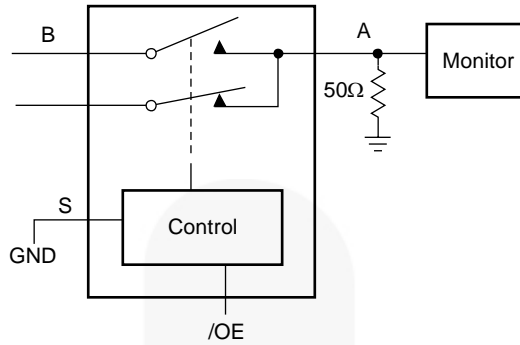


Figure 13. Bandwidth Test

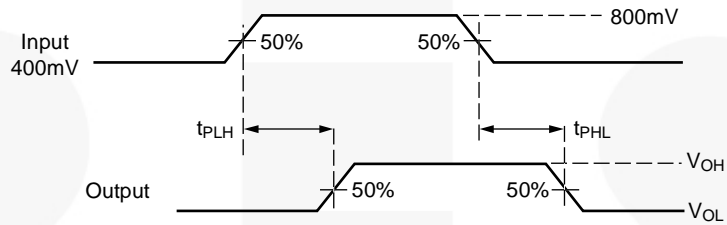


Figure 14. Propagation Delay

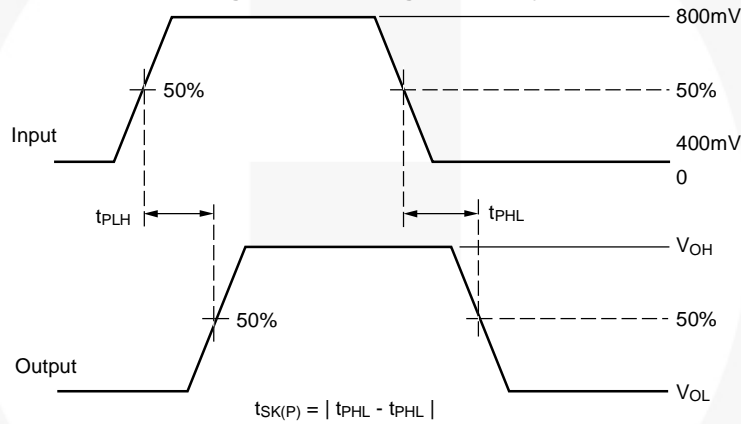


Figure 15. Pulse Skew  $t_{SK(P)}$

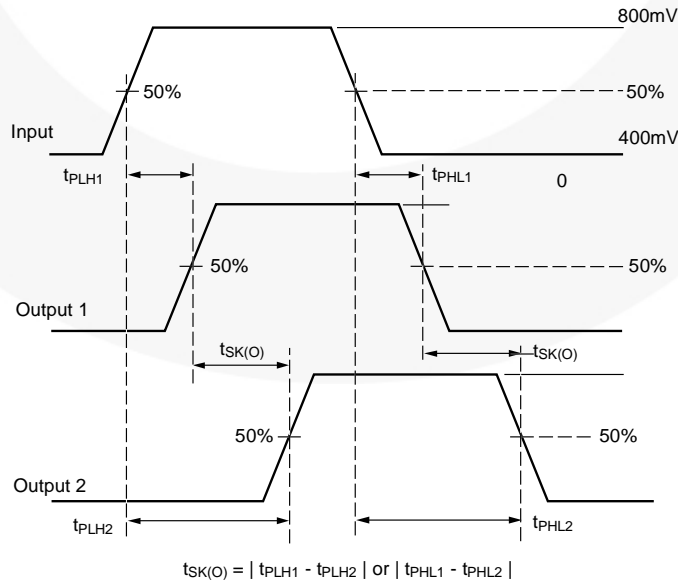
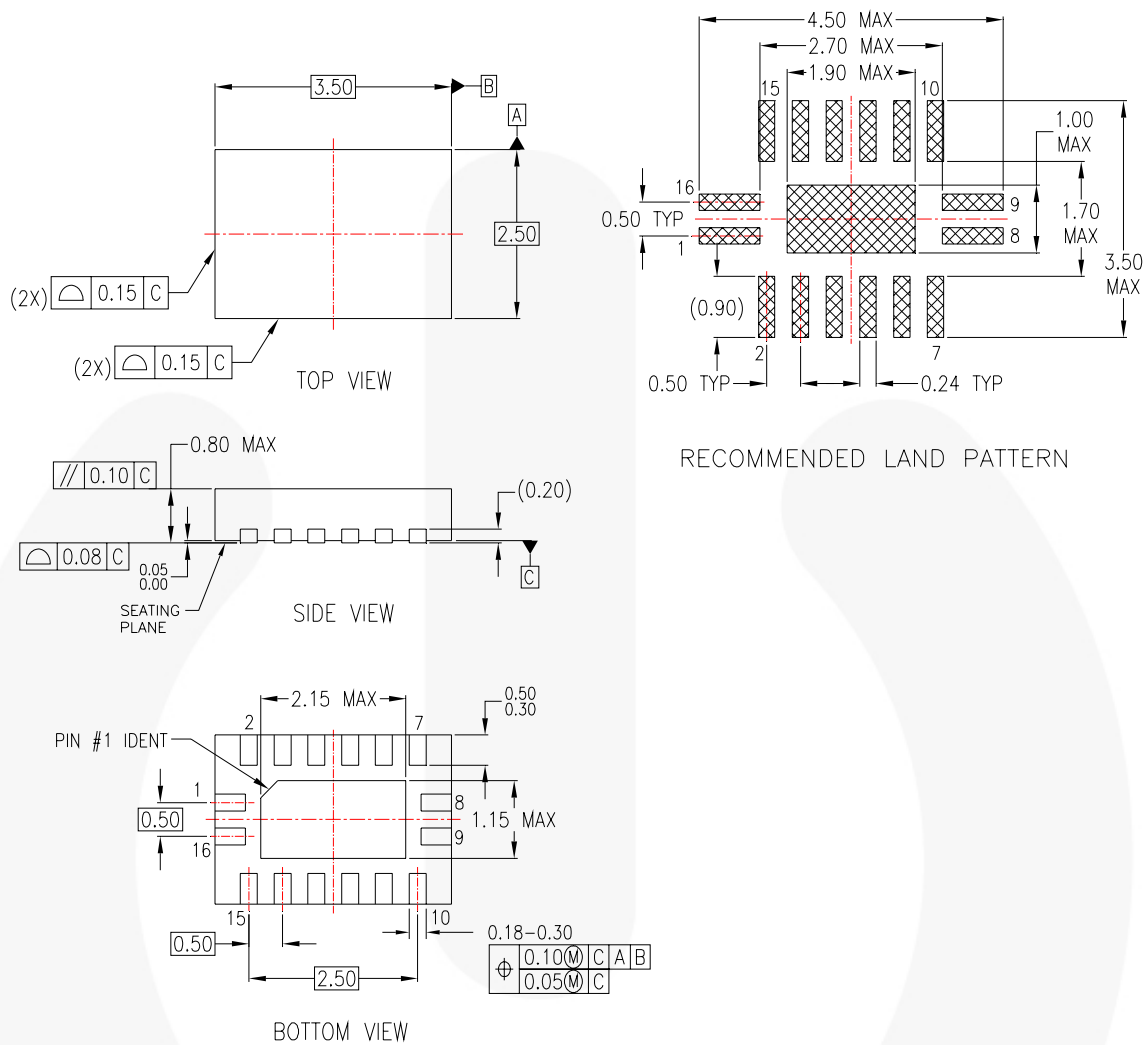


Figure 16. Output Skew  $t_{SK(O)}$



## Physical Dimensions



### NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MO-241, VARIATION AB
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994

MLP16ErevA

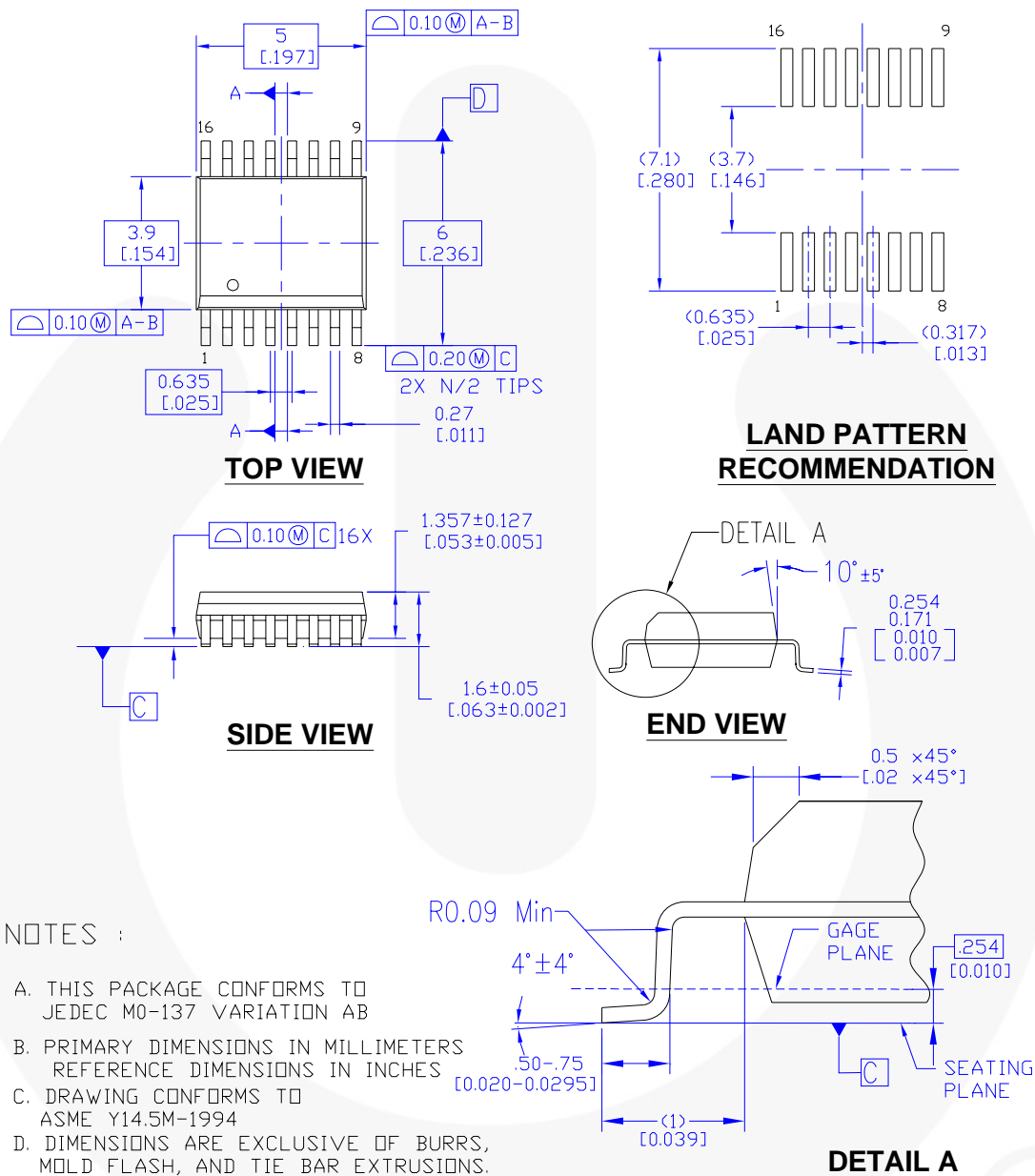
Figure 17. 16-Terminal Depopulated Quad Very-Thin Flat Pack No Leads (DQFN), JEDEC MO-241, 2.5 x 3.5mm

**Note:** [click here for tape and reel specifications, available at:](http://www.fairchildsemi.com/products/analog/pdf/MLP16_25x35_TNR.pdf)  
[http://www.fairchildsemi.com/products/analog/pdf/MLP16\\_25x35\\_TNR.pdf](http://www.fairchildsemi.com/products/analog/pdf/MLP16_25x35_TNR.pdf)

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## Physical Dimensions



NOTES :

- A. THIS PACKAGE CONFORMS TO JEDEC MO-137 VARIATION AB
- B. PRIMARY DIMENSIONS IN MILLIMETERS  
REFERENCE DIMENSIONS IN INCHES
- C. DRAWING CONFORMS TO ASME Y14.5M-1994
- D. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

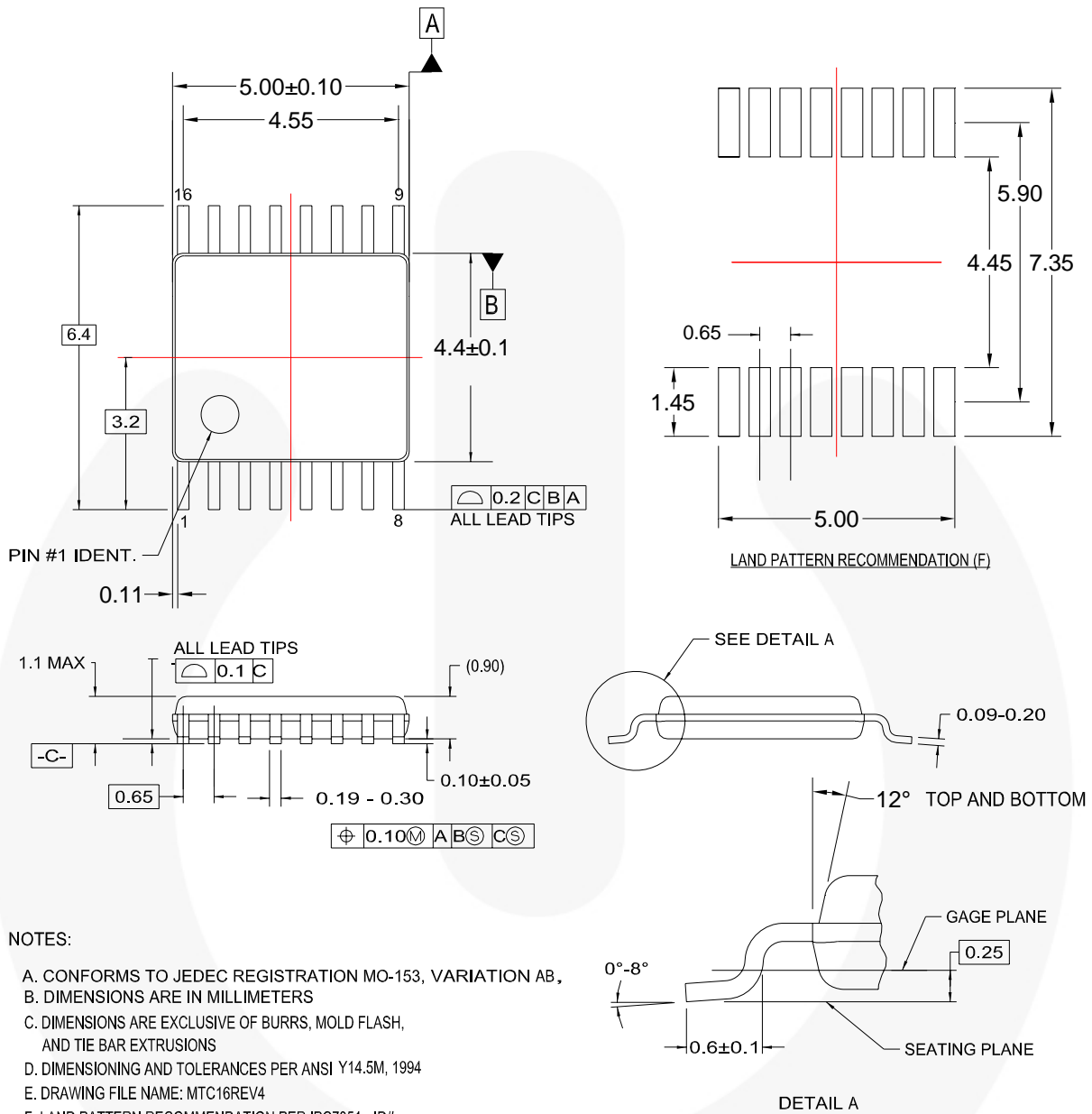
MQA16AREVB

**Figure 18. 16-Lead Quarter Size Outline Package (QSOP), JEDEC MO-137, 0.150-inch Wide**

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Physical Dimensions



NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB,
- B. DIMENSIONS ARE IN MILLIMETERS
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS
- D. DIMENSIONING AND TOLERANCES PER ANSI Y14.5M, 1994
- E. DRAWING FILE NAME: MTC16REV4
- F. LAND PATTERN RECOMMENDATION PER IPC7351 - ID# TSOP65P640X110-16N

MTC16rev4

Figure 19. 16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

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| FACT <sup>®</sup>   | Motion-SPM <sup>™</sup>                       | SuperSOT <sup>™</sup> -6  | VisualMax <sup>™</sup>  |
| FAST <sup>®</sup>   | OPTOLOGIC <sup>®</sup>                        | SuperSOT <sup>™</sup> -8  |   |
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No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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