



STLS2E02

Loongson 2E: 700MHz 64-bit superscalar MIPS® based microprocessor

Data Brief

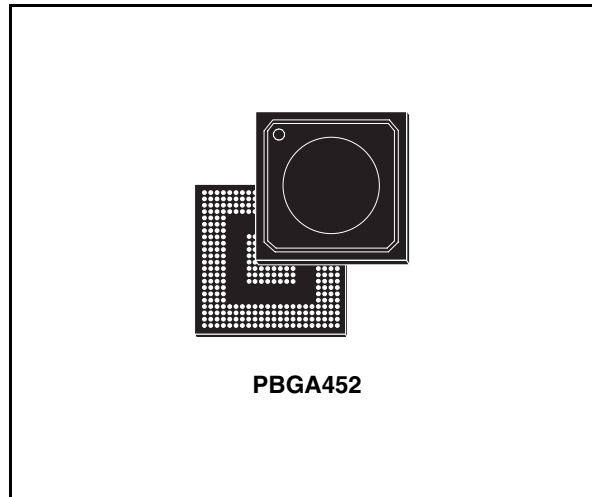
Features

- 64 bit superscalar architecture
- 700MHz clock frequency (typical conditions)
- Single/double precision floating-point units
- New Streaming Multimedia instruction set support (SIMD)
- 64KB instruction cache, 64KB data cache, on-chip 512KB unified L2 cache
- On-chip DDR-333 controller
- Thermal Design Power (TDP)
 - 4W @ 700MHz
- Leading edge 90nm process technology
- 35x35 BGA package
- MIPS based
- MIPS bus interface (Sysad)

Description

The STLS2E02, is a MIPS based 64-bit superscalar microprocessor, able to issue four instructions per clock cycle among six functional units: two integer, two single/double-precision floating-point, one 64bit SIMD and one load/store unit.

The microarchitecture is organized with nine stages of pipeline and support of dynamic branch prediction.



The memory hierarchy is composed by the first level of 64KB 4-way set associative cache for instructions and data, the second level of 512KB unified 4-ways set associative cache and the Memory Management Unit with Table Lookside Buffer.

The Loongson microprocessor family is the outcome of a successful collaboration started in 2004 between STMicroelectronics and the Institute of Computing Technology, part of the Chinese Academy of Science. Loongson microprocessors were co-developed by STMicroelectronics and the Institute of Computing Technology to address all the applications requiring high level of performance and low power dissipation.

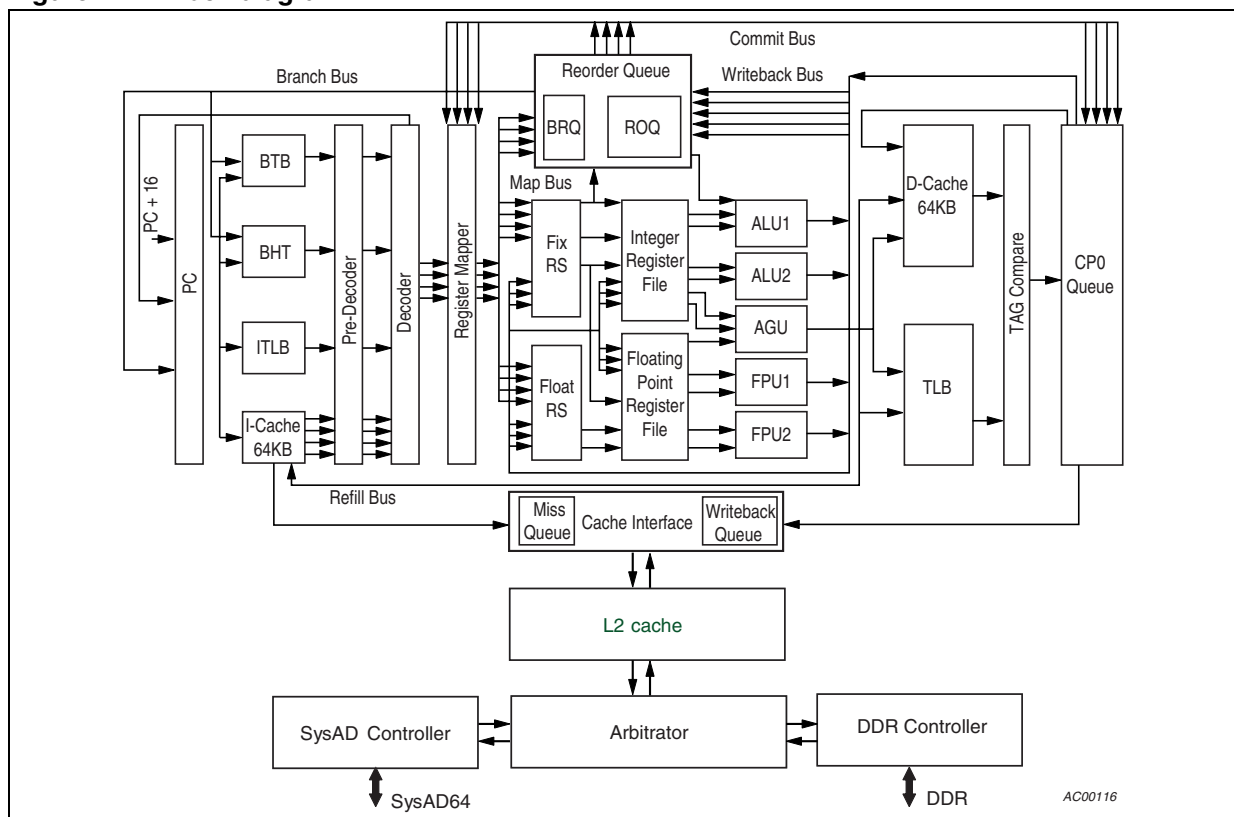
Table 1. Device summary

Part numbers	Package	Packing
STLS2E02	PBGA452 (35x35x2.33mm)	Tray

1 Architectural features and block diagram

- CPU
 - Out-of-order superscalar 64bit architecture
 - MIPS based
 - 9 stage pipeline organized in fetch, pre-decode, decode, reg-map, dispatch, issue, reg-read, execution and commit
 - Up to 64 instructions executed out-of-order with four issue mechanism
 - 64bit register file (32 fix+32 float)
 - Register renaming unit composed by 64-entry physical register files
 - Branch prediction unit
 - Six functional units: two integer, two float, one SIMD unit, one load/store unit
- Memory Hierarchy
 - 64KB + 64KB four-ways set-associative first level instruction and data cache
 - 512KB four-ways set associative unified second level cache
 - Up to 24 non-blocking accesses with on-the-fly Memory Disambiguation
 - Load speculation through value return from previous pending stores
 - Miss word first access for cache miss access
 - Instruction 16-entry TLB (Table Lookside Buffer) and unified 64-entry TLB with page size from 4KB to 4MB

Figure 1. Block diagram

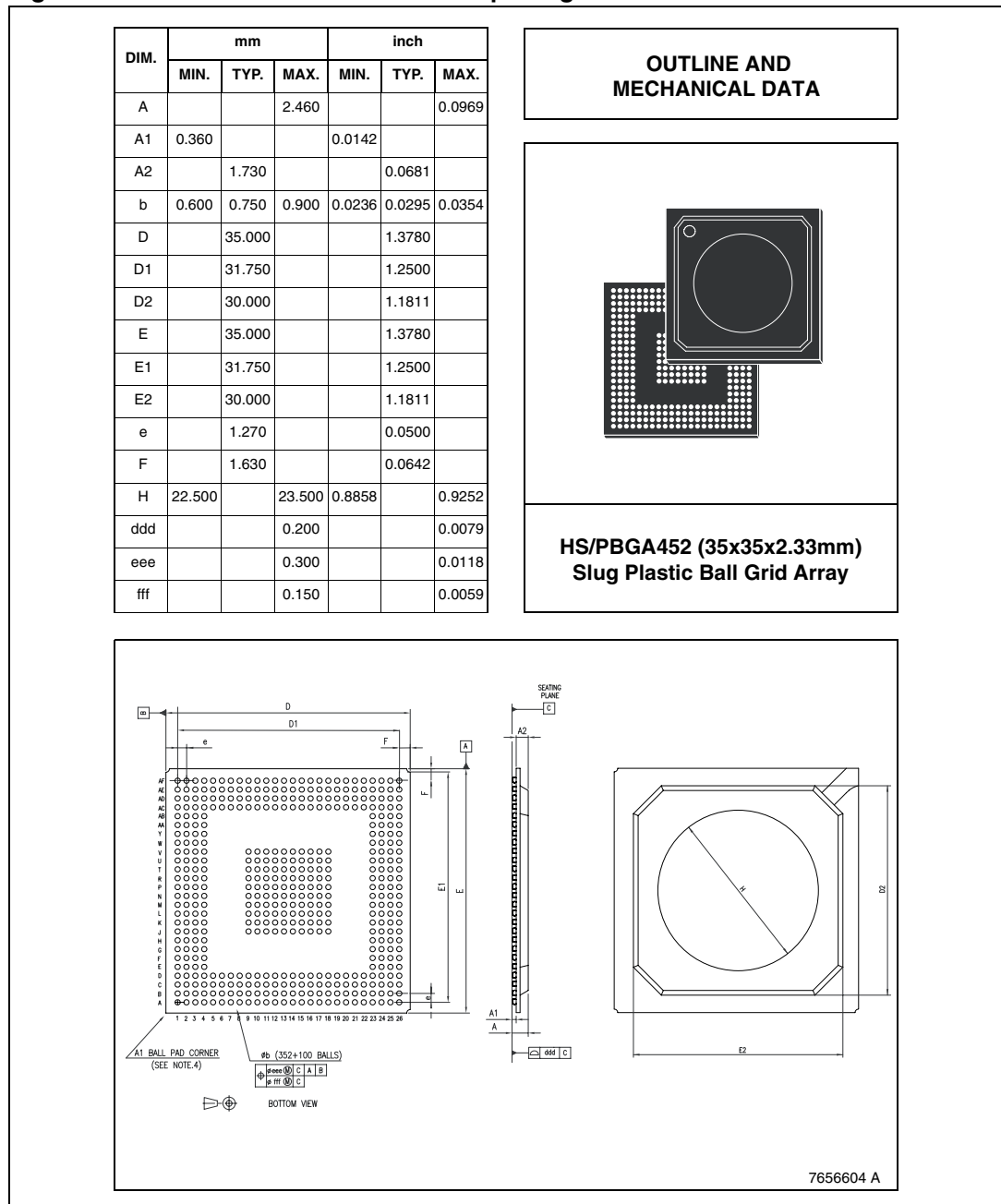


2 Package information

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label.

ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Figure 2. PBGA452 mechanical data & package dimensions



3 Revision history

Table 2. Document revision history

Date	Revision	Changes
23-Mar-2007	1	Initial release.
26-Apr-2007	2	Text modifications.

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