



Dual Per-Pin Parametric Measurement Units

MAX9951/MAX9952

General Description

The MAX9951/MAX9952 dual parametric measurement units (PMUs) feature a small package size, wide force and measurement range, and high accuracy, making the devices ideal for automatic test equipment (ATE) and other instrumentation that requires a PMU per pin or per site.

The MAX9951/MAX9952 force or measure voltages in the -2V to +7V through -7V to +13V ranges, dependent upon the supply voltage (V_{CC} and V_{EE}). The devices handle supply voltages of up to +30V (V_{CC} to V_{EE}) and a 20V device-under-test (DUT) voltage swing at full current. The MAX9951/MAX9952 also force or measure currents up to $\pm 64\text{mA}$ with a lowest full-scale range of $\pm 2\mu\text{A}$. Integrated support circuitry facilitates use of an external buffer amplifier for current ranges greater than $\pm 64\text{mA}$.

A voltage proportional to the measured output voltage or current is provided at the MSR_{-} output. Integrated comparators, with externally set voltage thresholds, provide detection for both voltage and current levels. The MSR_{-} and comparator outputs can be placed in a high-impedance state. Separate FORCE and SENSE connections are short-circuit protected for voltages from ($V_{EE} - 0.3\text{V}$) to ($V_{CC} + 0.3\text{V}$). The FORCE output also features a low-leakage, high-impedance state.

Integrated voltage clamps limit the force output to levels set externally. The force-current or the measure-current voltage can be offset -0.2V to +4.4V (IOS). This feature allows for the centering of the control or measured signal within the external DAC or ADC range.

The MAX9951D/MAX9952D feature an integrated $10\text{k}\Omega$ force-sense resistor between $FORCE_{-}$ and $SENSE_{-}$. The MAX9951F/MAX9952F have no internal force-sense resistor. These devices are available in a 64-pin, 10mm x 10mm, 0.5mm pitch TQFP package with an exposed 8mm x 8mm die pad on the top (MAX9951) or the bottom (MAX9952) of the package for efficient heat removal. The exposed pad is internally connected to V_{EE} . The MAX9951/MAX9952 are specified over the commercial 0°C to $+70^{\circ}\text{C}$ temperature range.

Applications

Memory Testers
VLSI Testers
System-on-a-Chip Testers
Structural Testers

Features

- ◆ Force Voltage/Measure Current (FVMI)
- ◆ Force Current/Measure Voltage (FIMV)
- ◆ Force Voltage/Measure Voltage (FVMV)
- ◆ Force Current/Measure Current (FIMI)
- ◆ Force Nothing/Measure Voltage (FNMV)
- ◆ Force Nothing/Measure Current (FNMI, Range E Only)
- ◆ Termination/Measure Current
- ◆ Termination/Measure Voltage
- ◆ Five Programmable Current Ranges
 - $\pm 2\mu\text{A}$
 - $\pm 20\mu\text{A}$
 - $\pm 200\mu\text{A}$
 - $\pm 2\text{mA}$
 - $\pm 64\text{mA}$
- ◆ -2V to +7V Through -7V to +13V Input-Voltage Range
- ◆ Force-Current/Measure-Current Adjustable-Voltage Offset (IOS)
- ◆ Programmable Voltage Clamps at Force Output
- ◆ Low-Leakage, High-Impedance Measure, and Force States
- ◆ 3-Wire Serial Interface
- ◆ Low 6mA (max) Quiescent Current per PMU

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX9951DCCB	0°C to $+70^{\circ}\text{C}$	64 TQFP-EPR
MAX9951FCCB*	0°C to $+70^{\circ}\text{C}$	64 TQFP-EPR
MAX9952DCCB	0°C to $+70^{\circ}\text{C}$	64 TQFP-EP
MAX9952FCCB*	0°C to $+70^{\circ}\text{C}$	64 TQFP-EP

*Future product—contact factory for availability.

Selector Guide

PART	DESCRIPTION
MAX9951DCCB	Internal $10\text{k}\Omega$ force-sense resistor
MAX9951FCCB	External force-sense resistor
MAX9952DCCB	Internal $10\text{k}\Omega$ force-sense resistor
MAX9952FCCB	External force-sense resistor

Pin Configurations appear at end of data sheet.



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For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

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ABSOLUTE MAXIMUM RATINGS

V _{CC} to AGND	+20V
V _{EE} to AGND	-15V
V _{CC} to V _{EE}	+32V
V _L to AGND	+6V
AGND to DGND	-0.5V to +0.5V
Digital Inputs/Outputs	-0.3V to (V _L + 0.3V)
All Other Pins to AGND	(V _{EE} - 0.3V) to (V _{CC} + 0.3V)
Continuous Power Dissipation (T _A = +70°C)	
MAX9951_CCB (derate 43.5mW/°C above +70°C)	3478mW
MAX9952_CCB (derate 125mW/°C above +70°C)	10,000mW

θ _{JA} MAX9951_CCB	+8°C/W
θ _{JC} MAX9951_CCB	+2°C/W
θ _{JA} MAX9952_CCB	+23°C/W
θ _{JC} MAX9952_CCB	+8°C/W
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range (commercial)	0°C to +70°C
Lead Temperature (soldering 10s)	+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +12V, V_{EE} = -7V, V_L = +3.3V, T_A = +25°C, unless otherwise noted. Specifications at T_A = T_{MIN} and T_A = T_{MAX} are guaranteed by design and characterization. Typical values are at T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
FORCE VOLTAGE						
Force Input Voltage Range	V _{IN0_} , V _{IN1_}		V _{EE} + 2.5		V _{CC} - 2.5	V
Forced Voltage	V _{DUT}	DUT current at full scale	V _{CC} = +12V, V _{EE} = -7V	-2	+7	V
			V _{CC} = +18V, V _{EE} = -12V	-7	+13	
		DUT current = 0	V _{EE} + 2.5		V _{CC} - 2.5	
Input Bias Current				±1		µA
Forced-Voltage Offset	V _{FOS}		-25		+25	mV
Forced-Voltage-Offset Temperature Coefficient				±100		µV/°C
Forced-Voltage Gain Error	V _{FGE}	Nominal gain of +1	-1	0.005	+1	%
Forced-Voltage-Gain Temperature Coefficient				±10		ppm/°C
Forced-Voltage Linearity Error	V _{FLE}	Gain and offset errors calibrated out (Notes 2, 3)	-0.02		+0.02	%FSR
MEASURE CURRENT						
Measure-Current Offset	I _{MOS}	(Note 2)	-1		+1	%FSR
Measure-Current-Offset Temperature Coefficient				±20		ppm/°C
Measure-Current Gain Error	I _{MGE}	(Note 4)	-1		+1	%
Measure-Current-Gain Temperature Coefficient				±20		ppm/°C
Linearity Error	I _{MLER}	Gain and offset errors calibrated out (Notes 2, 3, 5)	-0.02		+0.02	%FSR

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DC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +12V, V_{EE} = -7V, V_L = +3.3V, T_A = +25°C, unless otherwise noted. Specifications at T_A = T_{MIN} and T_A = T_{MAX} are guaranteed by design and characterization. Typical values are at T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Measure-Output-Voltage Range Over Full-Current Range	V _{MSR}	V _{IOS_} = V _{DUTGND}	-4		+4	V
		V _{IOS_} = 4V + V _{DUTGND}	0		+8	
Current-Sense Amp Offset-Voltage Input	V _{IOS}	Relative to V _{DUTGND}	-0.2		+4.4	V
Rejection of Output-Measure Error Due to Common-Mode Sense Voltage	CMV _R LER	(Notes 4 and 6)		+0.001	+0.007	%FSR/V
Measure-Current Range		Range E, R _E = 500kΩ	-2		+2	μA
		Range D, R _D = 50kΩ	-20		+20	
		Range C, R _C = 5kΩ	-200		+200	
		Range B, R _B = 500Ω	-2		+2	mA
		Range A, R _A = 15.6Ω	-64		+64	
FORCE CURRENT						
Input Voltage Range for Setting Forced Current Over Full Range	V _{IN0_} , V _{IN1_}	V _{IOS_} = V _{DUTGND}	-4		+4	V
		V _{IOS_} = 4V + V _{DUTGND}	0		+8	
Current-Sense Amp Offset-Voltage Input	V _{IOS}	Relative to V _{DUTGND}	-0.2		+4.4	V
IOS_ Input Bias Current				±1		μA
Forced-Current Offset		(Note 2)	-1		+1	%FSR
Forced-Current-Offset Temperature Coefficient				±20		ppm/°C
Forced-Current Gain Error		(Note 4)	-1		+1	%
Forced-Current-Gain Temperature Coefficient				±20		ppm/°C
Forced-Current Linearity Error	I _F LER	Gain and offset errors calibrated out (Notes 2, 3, 5)	-0.02		+0.02	%FSR
Rejection of Output Error Due to Common-Mode Load Voltage	CMR _I OER	(Notes 4 and 6)		+0.001	+0.007	%FSR/V
Forced-Current Range		Range E, R _E = 500kΩ	-2		+2	μA
		Range D, R _D = 50kΩ	-20		+20	
		Range C, R _C = 5kΩ	-200		+200	
		Range B, R _B = 500Ω	-2		+2	mA
		Range A, R _A = 15.6Ω	-64		+64	

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DC ELECTRICAL CHARACTERISTICS (continued)

($V_{CC} = +12V$, $V_{EE} = -7V$, $V_L = +3.3V$, $T_A = +25^\circ C$, unless otherwise noted. Specifications at $T_A = T_{MIN}$ and $T_A = T_{MAX}$ are guaranteed by design and characterization. Typical values are at $T_A = +25^\circ C$, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
MEASURE VOLTAGE						
Measure-Voltage-Offset	V_{MOS}		-25		+25	mV
Measure-Voltage-Offset Temperature Coefficient				± 100		$\mu V/^\circ C$
Gain Error	V_{MGER}	Nominal gain of +1	-1	± 0.005	+1	%
Measure-Voltage-Gain Temperature Coefficient				± 10		ppm/ $^\circ C$
Measure-Voltage Linearity Error	V_{MLER}	Gain and offset errors calibrated out (Notes 2, 3, 5)	-0.02		+0.02	%FSR
Measure-Output-Voltage Range Over Full DUT Voltage	V_{MSR}	DUT current at full scale	$V_{CC} = +12V$, $V_{EE} = -7V$	-2	+7	V
			$V_{CC} = +18V$, $V_{EE} = -12V$	-7	+13	
		DUT current = 0	$V_{EE} + 2.5$		$V_{CC} - 2.5$	
FORCE OUTPUT						
Off-State Leakage Current			-1		+1	nA
Short-Circuit Current Limit	I_{LIM-}		-92		-65	mA
	I_{LIM+}		+65		+92	
Force-to-Sense Resistor	R_{FS}	D option only	8	10	12	k Ω
SENSE INPUT						
Input Voltage Range			$V_{EE} + 2.5$		$V_{CC} - 2.5$	V
Leakage Current		F option only	-1		+1	nA
COMPARATOR INPUTS						
Input Voltage Range			$V_{EE} + 2.5$		$V_{CC} - 2.5$	V
Offset Voltage			-25		+25	mV
Input Bias Current				± 1		μA
VOLTAGE CLAMPS						
Input Control Voltage	$V_{CLLO_}$, $V_{CLHI_}$		$V_{EE} + 2.4$		$V_{CC} - 2.4$	V
Clamp Voltage Accuracy		(Note 7)	-100		+100	mV
DIGITAL INPUTS						
Input High Voltage (Note 8)	V_{IH}	$V_L = 5V$	+3.5			V
		$V_L = 3.3V$	+2.0			
		$V_L = 2.5V$	+1.7			
Input Low Voltage (Note 8)	V_{IL}	$V_L = 5V$ or $3.3V$			+0.8	V
		$V_L = 2.5V$			+0.7	
Input Current	I_{IN}			± 1		μA
Input Capacitance	C_{IN}			3.0		pF

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DC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +12V, V_{EE} = -7V, V_L = +3.3V, T_A = +25°C, unless otherwise noted. Specifications at T_A = T_{MIN} and T_A = T_{MAX} are guaranteed by design and characterization. Typical values are at T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
COMPARATOR OUTPUTS						
Output High Voltage	V _{OH}	V _L = +2.375V to +5.5V, R _{PUP} = 1kΩ	V _L - 0.2			V
Output Low Voltage	V _{OL}	V _L = +2.375V to +5.5V, R _{PUP} = 1kΩ	+0.4			V
High-Impedance-State Leakage Current			±1			μA
High-Impedance-State Output Capacitance			6.0			pF
DIGITAL OUTPUTS						
Output High Voltage	V _{OH}	I _{OUT} = 1mA, V _L = +2.375V to +5.5V, relative to DGND	V _L - 0.25			V
Output Low Voltage	V _{OL}	I _{OUT} = -1mA, V _L = +2.375V to +5.5V, relative to DGND	+0.2			V
POWER SUPPLY						
Positive Supply	V _{CC}	(Note 1)	+10	+12	+18	V
Negative Supply	V _{EE}	(Note 1)	-15	-7	-5	V
Total Supply Voltage	V _{CC} - V _{EE}	(Note 9)	+30			V
Logic Supply	V _L		+2.375	+5.5		V
Positive Supply Current	I _{CC}	No load, clamps enabled	10.0			mA
Negative Supply Current	I _{EE}	No load, clamps enabled	10.0			mA
Logic Supply Current	I _L	No load, all digital inputs at rails	1.2			mA
Analog Ground Current	I _{AGND}	No load, clamps enabled	0.9			mA
Digital Ground Current	I _{DGND}	No load, all digital inputs at rails	1.4			mA
Power-Supply Rejection Ratio	PSRR	1MHz, measured at force output	20			dB
		60Hz, measured at force output	85			

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AC ELECTRICAL CHARACTERISTICS

($V_{CC} = +12V$, $V_{EE} = -7V$, $V_L = +3.3V$, $C_{CM} = 120pF$, $C_L = 100pF$, $T_A = +25^\circ C$, unless otherwise noted. Specifications at $T_A = T_{MIN}$ and $T_A = T_{MAX}$ are guaranteed by design and characterization. Typical values are at $T_A = +25^\circ C$, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
FORCE VOLTAGE (Notes 10, 11)						
Settling Time		Range E, $R_E = 500k\Omega$		150		μs
		Range D, $R_D = 50k\Omega$		50		
		Range C, $R_C = 5k\Omega$		20	30	
		Range B, $R_B = 500\Omega$		20		
		Range A, $R_A = 15.6\Omega$		25		
FORCE VOLTAGE/MEASURE CURRENT (Notes 10, 11)						
Settling Time		Range E, $R_E = 500k\Omega$		500		μs
		Range D, $R_D = 50k\Omega$		100		
		Range C, $R_C = 5k\Omega$		30	55	
		Range B, $R_B = 500\Omega$		25		
		Range A, $R_A = 15.6\Omega$		25		
Range Change Switching		In addition to force-voltage and measure-current settling times, range A to range B, $R_A = 15.6\Omega$, $R_B = 500\Omega$		12		μs
FORCE CURRENT/MEASURE VOLTAGE (Notes 10, 11)						
Settling Time		Range E, $R_E = 500k\Omega$		2500		μs
		Range D, $R_D = 50k\Omega$		350		
		Range C, $R_C = 5k\Omega$		30	60	
		Range B, $R_B = 500\Omega$		25		
		Range A, $R_A = 15.6\Omega$		25		
Range Change Switching		In addition to force-current and measure-voltage settling times, range A to range B, $R_A = 15.6\Omega$, $R_B = 500\Omega$		12		μs
SENSE INPUT TO MEASURE OUTPUT PATH						
Propagation Delay		$C_{LMSR} = 100pF$		0.2		μs
MEASURE OUTPUT						
Maximum Stable Load Capacitance				1000		pF
COMPARATORS ($C_{LCOMP} = 20pF$, $R_{PUP} = 1k\Omega$)						
Propagation Delay		50mV overdrive, 1Vp-p, measured from input-threshold zero crossing to 50% of output voltage (Note 12)		75		ns
Rise Time		20% to 80%		60		ns
Fall Time		80% to 20%		5		ns
SERIAL PORT ($V_L = +3.3V$, $C_{DOUT} = 10pF$)						
Serial Clock Frequency	fSCLK	(Note 13)			20	MHz
SCLK Pulse-Width High	tCH			12		ns
SCLK Pulse-Width Low	tCL			12		ns

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AC ELECTRICAL CHARACTERISTICS (continued)

($V_{CC} = +12V$, $V_{EE} = -7V$, $V_L = +3.3V$, $C_{CM} = 120pF$, $C_L = 100pF$, $T_A = +25^\circ C$, unless otherwise noted. Specifications at $T_A = T_{MIN}$ and $T_A = T_{MAX}$ are guaranteed by design and characterization. Typical values are at $T_A = +25^\circ C$, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCLK Fall to DOUT Valid	t _{DO}				22	ns
\overline{CS} Low to SCLK High Setup	t _{CSS0}		10			ns
SCLK High to \overline{CS} High Hold	t _{CSH1}		22			ns
SCLK High to \overline{CS} Low Hold	t _{CSH0}		0			ns
\overline{CS} High to SCLK High Setup	t _{CSS1}		5			ns
DIN to SCLK High Setup	t _{DS}		10			ns
DIN to SCLK High Hold	t _{DH}	(Note 12)	0			ns
\overline{CS} Pulse-Width High	t _{CSWH}		10			ns
\overline{CS} Pulse-Width Low	t _{CSWL}		10			ns
\overline{LOAD} Pulse-Width Low	t _{LDW}		20			ns
V _{DD} High to \overline{CS} Low (Power-Up)		(Note 12)			500	ns

Note 1: The device operates properly with different supply voltages with equally different voltage swings.

Note 2: Interpret errors expressed in terms of %FSR (percent of full-scale range) as a percentage of the end-point-to-end-point range, i.e., for the $\pm 64mA$ range, the full-scale range = 128mA, and a 1% error = 1.28mA.

Note 3: Case must be maintained $\pm 5^\circ C$ for linearity specifications.

Note 4: Tested in range C.

Note 5: Current linearity specifications are maintained to within 700mV of the clamp voltages when the clamps are enabled.

Note 6: Specified as the percent of full-scale range change at the output per volt change in the DUT voltage.

Note 7: $V_{CLLO_}$ and $V_{CLHI_}$ should differ by at least 700mV.

Note 8: The digital interface accepts +5V, +3.3V, and +2.5V CMOS logic levels. The voltage at V_L adjusts the threshold.

Note 9: Guaranteed by design.

Note 10: Settling times are to 0.1% of FSR. $C_{x_} = 60pF$.

Note 11: All settling times are specified using a single compensation capacitor ($C_{x_}$) across all current-sense resistors. Use an individual capacitor across each sense resistor for better performance across all current ranges, particularly the lower ranges.

Note 12: The propagation delay time is only guaranteed over the force-voltage output range. Propagation delay is measured by holding $V_{SENSE_}$ steady and transitioning $THMAX_$ or $THMIN_$.

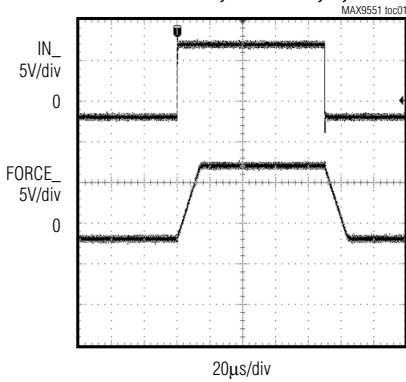
Note 13: Maximum serial clock frequency may diminish at $V_L < +3.3V$.

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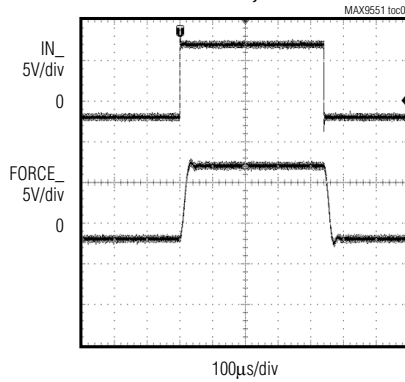
Typical Operating Characteristics

($V_{CC} = +12V$, $V_{EE} = -7V$, $C_L = 100pF$, $C_{CM_} = 120pF$, $C_{CX_} = 60pF$, R_L to $+2.5V$, range A: $R_{A_} = 15.6\Omega$, $R_L = 70.3\Omega$; range B: $R_{B_} = 500\Omega$, $R_L = 2.25k\Omega$; range C: $R_{C_} = 5k\Omega$, $R_L = 22.5k\Omega$; range D: $R_{D_} = 50k\Omega$, $R_L = 225k\Omega$; range E: $R_{E_} = 500k\Omega$, $R_L = 2.25M\Omega$, $T_A = +25^\circ C$.)

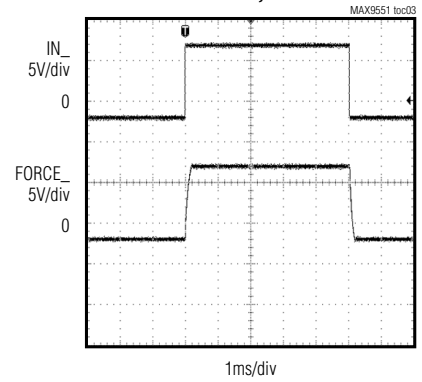
**TRANSIENT RESPONSE
FVMI MODE, RANGES A, B, C**



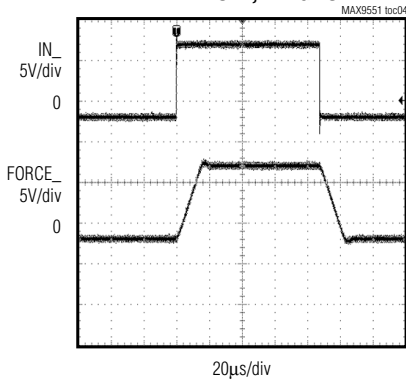
**TRANSIENT RESPONSE
FVMI MODE, RANGE D**



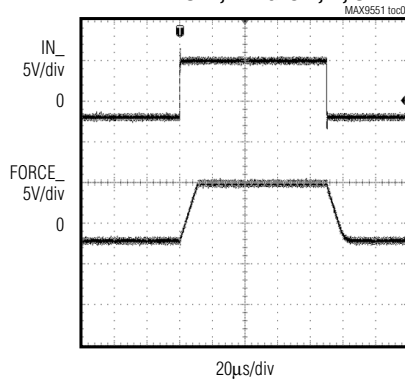
**TRANSIENT RESPONSE
FVMI MODE, RANGE E**



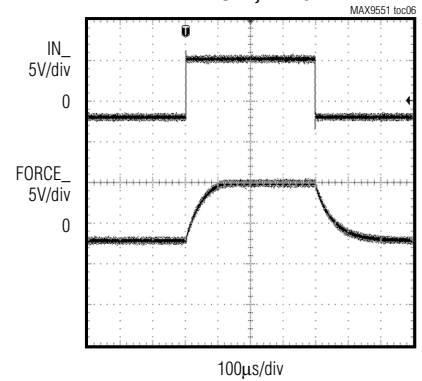
**TRANSIENT RESPONSE
FVMV MODE, RANGE C**



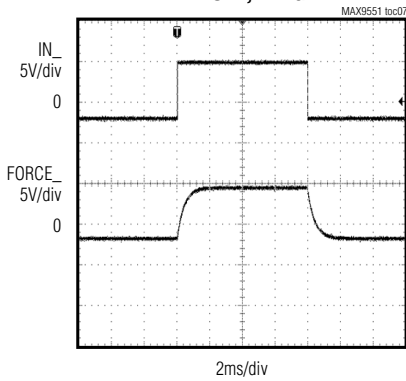
**TRANSIENT RESPONSE
FIMI MODE, RANGES A, B, C**



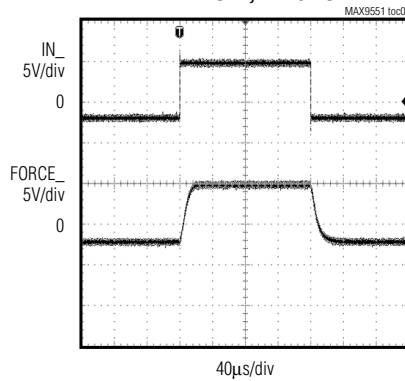
**TRANSIENT RESPONSE
FIMI MODE, RANGE D**



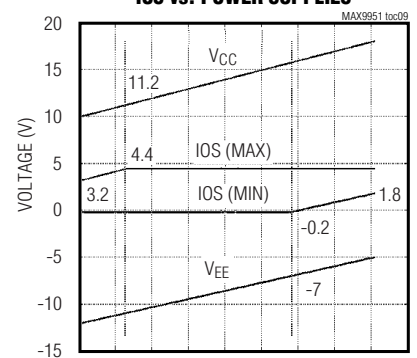
**TRANSIENT RESPONSE
FIMI MODE, RANGE E**



**TRANSIENT RESPONSE
FIMI MODE, RANGE C**



IOS vs. POWER SUPPLIES



Dual Per-Pin Parametric Measurement Units

Pin Description

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PIN		NAME	FUNCTION
MAX9951	MAX9952		
1	48	SENSEA	PMU-A Sense Input. A Kelvin connection to the DUT. Provides the feedback signal in FVMI mode and the measured signal in FIMV mode for PMU-A.
2	47	FORCEA	PMU-A Driver Output. Forces a current or voltage to the DUT for PMU-A.
3	46	CCA	PMU-A Compensation Capacitor Connection. Provides compensation for the PMU-A main amplifier. Connect a 120pF capacitor from CCA to CCOMA.
5, 15, 34, 44	5, 15, 34, 44	V _{EE}	Negative Analog-Supply Input
4, 14, 35, 45	4, 14, 35, 45	V _{CC}	Positive Analog-Supply Input
6	43	CCOMA	Common Connection of CMA and CXA for PMU-A
7	42	RAAS	PMU-A Range Setting Resistor-Sense Connection
8	41	RAA	PMU-A Range A Setting Resistor Connection
9	40	RAB	PMU-A Range B Setting Resistor Connection
10	39	RAC	PMU-A Range C Setting Resistor Connection
11	38	RAD	PMU-A Range D Setting Resistor Connection
12	37	RAE	PMU-A Range E Setting Resistor Connection
13	36	RAX	PMU-A Current-Range Sense-Resistor Connection. Connects to the external current range sense resistor for PMU-A.
16	33	EXTSELA	PMU-A External Current-Range Selector. Selects the external current range for PMU-A.
17	32	$\overline{\text{DUTLA}}$	PMU-A Window Comparator Lower Comparator Output. A high output indicates that the sensed voltage at the window comparator is above V _{THMINA} . $\overline{\text{DUTLA}}$ is an open-drain output.
18	31	$\overline{\text{DUTHA}}$	PMU-A Window Comparator Higher Comparator Output. A high output indicates that the sensed voltage at the window comparator is below V _{THMAXA} . $\overline{\text{DUTHA}}$ is an open-drain output.
19	30	$\overline{\text{HI-ZA}}$	MSRA Tri-State Control Input. A logic-low places MSRA in a high-impedance state.
20	29	INSELA	Input Select PMU-A. INSELA is a logic input that selects between IN0A and IN1A. Force INSELA low to select IN0A. INSELA is NANDed with control register bit INMODEA.
21	28	TEMP	Temperature Output. V _{TEMP} = 10mV/°C. T _{DIE} (°C) = (100)V _{TEMP} - 273.
22	27	DGND	Digital Ground
23	26	V _L	Logic-Supply Voltage Input. The voltage applied at V _L sets the upper logic-voltage level.
24	25	DOUT	Serial-Data Output. A standard SPI™-compatible output. Data appears at DOUT MSB first.
25	24	DIN	Serial-Data Input. Load data into DIN MSB first.
26	23	$\overline{\text{LOAD}}$	Serial-Port Load Input. A logic-low asynchronously loads data from the input registers into the PMU registers.

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Dual Per-Pin Parametric Measurement Units

Pin Description (continued)

PIN		NAME	FUNCTION
MAX9951	MAX9952		
27	22	SCLK	Serial-Clock Input. SCLK accepts external clock frequencies up to 20MHz.
28	21	$\overline{\text{CS}}$	Chip-Select Input. Force $\overline{\text{CS}}$ low to enable the serial interface.
29	20	INSELB	Input Select PMU-B. INSELB is a logic input that selects between IN0B and IN1B. Force INSELB low to select IN0B. INSELB is NANDed with control register bit INMODEB.
30	19	$\overline{\text{HI-ZB}}$	MSRB Tri-State Control Input. A logic-low places MSRB in a high-impedance state.
31	18	$\overline{\text{DUTHB}}$	PMU-B Window Comparator Higher Comparator Output. A high output indicates that the sensed voltage at the window comparator is below V_{THMAXB} . DUTHB is an open-drain output.
32	17	$\overline{\text{DUTLB}}$	PMU-B Window Comparator Lower Comparator Output. A high output indicates that the sensed voltage at the window comparator is above V_{THMINB} . DUTLB is an open-drain output.
33	16	EXTSELB	PMU-B External Current-Range Selector. Selects the external current range for PMU-B.
36	13	RBX	PMU-B Current-Range Sense-Resistor Connection. Connects to the external current-range sense resistor for PMU-B.
37	12	RBE	PMU-B Range E Setting Resistor Connection
38	11	RBD	PMU-B Range D Setting Resistor Connection
39	10	RBC	PMU-B Range C Setting Resistor Connection
40	9	RBB	PMU-B Range B Setting Resistor Connection
41	8	RBA	PMU-B Range A Setting Resistor Connection
42	7	RBAS	PMU-B Range A Setting Resistor-Sense Connection
43	6	CCOMB	Common Connection of CMB and CXB for PMU-B
46	3	CCB	PMU-B Compensation Capacitor Connection. Provides compensation for the PMU-B main amplifier. Connect a 120pF capacitor from CCB to CCOMB.
47	2	FORCEB	PMU-B Driver Output. Forces a current or voltage to the DUT for PMU-B.
48	1	SENSEB	PMU-B Sense Input. A Kelvin connection to the DUT. Provides the feedback signal in FVMI mode and the measured signal in FIMV mode for PMU-B.
49	64	THMAXB	PMU-B Window Comparator Upper Threshold Voltage Input. Sets the upper voltage threshold for the PMU-B window comparator.
50	63	THMINB	PMU-B Window Comparator Lower Threshold Voltage Input. Sets the lower voltage threshold for the PMU-B window comparator.
51	62	CLHIB	PMU-B Upper-Clamp Voltage Input. Sets the upper-clamp voltage level.
52	61	CLLOB	PMU-B Lower-Clamp Voltage Input. Sets the lower-clamp voltage level.
53	60	IN0B	Force-Threshold Current Input for PMU-B. Sets the forced voltage in FV mode or the forced current in FI mode.
54	59	IN1B	Force-Threshold Voltage Input for PMU-B. Sets the forced voltage in FV mode or the forced current in FI mode

Dual Per-Pin Parametric Measurement Units

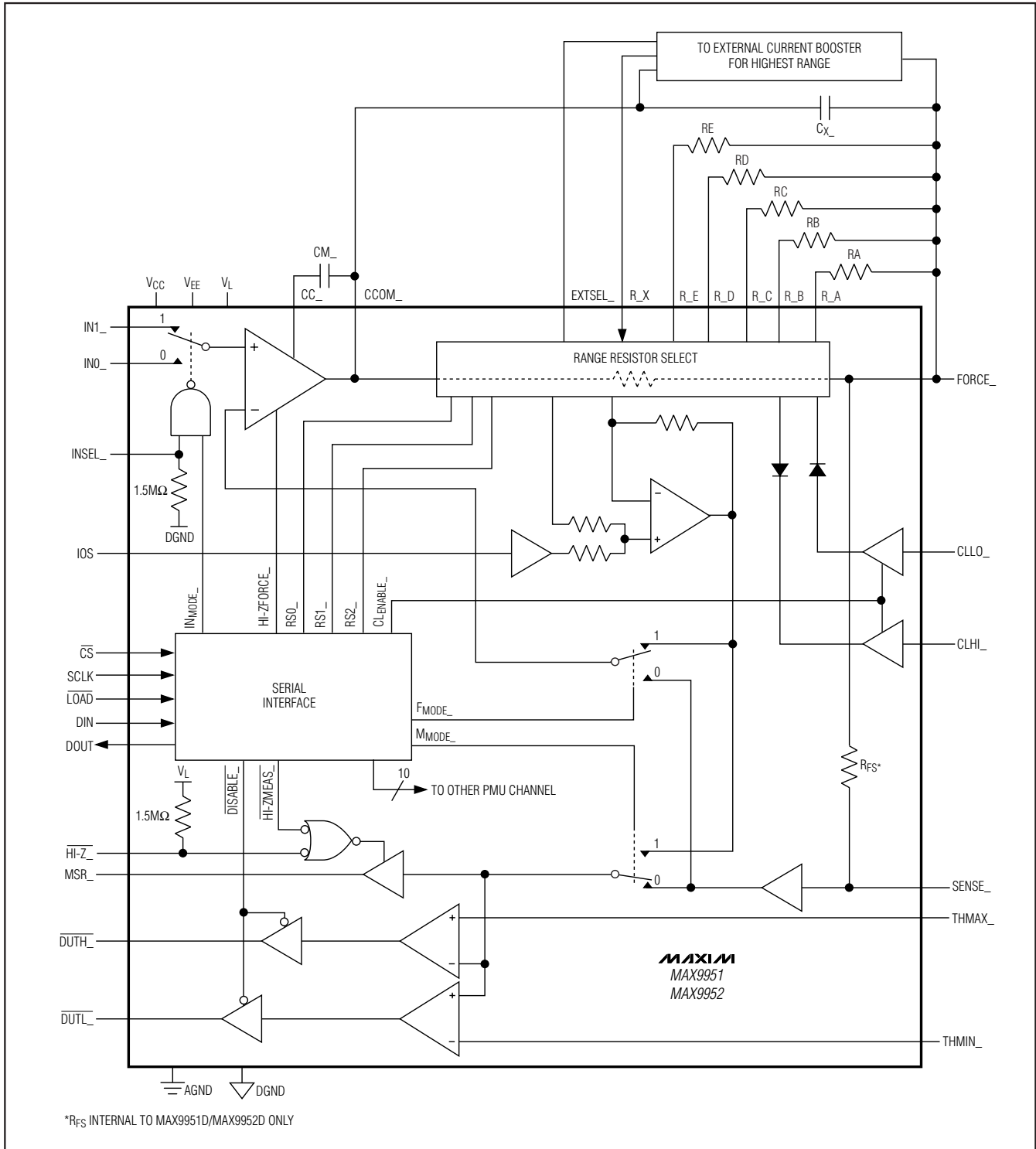
Pin Description (continued)

PIN		NAME	FUNCTION
MAX9951	MAX9952		
55	58	MSRB	PMU-B Measurement Output. Provides a voltage equal to the SENSE voltage in FIMV mode, and provides a voltage proportional to the DUT current in FVMI mode for PMU-B. Force HI-ZB low to place MSRB in a high-impedance state.
56	57	AGND	Analog Ground
57	56	IOS	Offset-Voltage Input. Sets an offset voltage for the internal current-sense amplifiers of both channels.
58	55	MSRA	PMU-A Measurement Output. Provides a voltage equal to the SENSE voltage in FIMV mode, and provides a voltage proportional to the DUT current in FVMI mode for PMU-A. Force HI-ZA low to place MSRA in a high-impedance state.
59	54	IN1A	Force-Threshold Voltage Input for PMU-A. Sets the forced voltage in FV mode or the forced current in FI mode.
60	53	IN0A	Force-Threshold Current Input for PMU-A. Sets the forced voltage in FV mode or the forced current in FI mode.
61	52	CLLOA	PMU-A Lower-Clamp Voltage Input. Sets the lower-clamp voltage level.
62	51	CLHIA	PMU-A Upper-Clamp Voltage Input. Sets the upper-clamp voltage level.
63	50	THMINA	PMU-A Window Comparator Lower Threshold Voltage Input. Sets the lower voltage threshold for the PMU-A window comparator.
64	49	THMAXA	PMU-A Window Comparator Upper Threshold Voltage Input. Sets the upper voltage threshold for the PMU-A window comparator.

MAX9951/MAX9952

Dual Per-Pin Parametric Measurement Units

Functional Diagram



Dual Per-Pin Parametric Measurement Units

Detailed Description

The MAX9951/MAX9952 force or measure voltages in the -2V to +7V through -7V to +13V ranges, dependent upon the supply voltage range (VCC and VEE). These devices also force or measure currents up to ±64mA, with a lowest full-scale range of ±2μA. Use an external buffer amplifier for current ranges greater than ±64mA.

MSR_ presents a voltage proportional to the measured voltage or current. Place MSR_ in a low-leakage, high-impedance state by forcing HI-Z_ low. Integrated comparators with externally programmable voltage thresholds provide “too low” (DUTL_) and “too high” (DUTH_) voltage-monitoring outputs. Each comparator output features a selectable high-impedance state. The devices feature separate FORCE_ and SENSE_ connections and are fully protected against short circuits. The FORCE_ output has two voltage clamps, negative (CLLO_) and positive (CLHI_), to limit the voltage to externally provided levels. Two control-voltage inputs, selected independently of the PMU mode, allow for greater flexibility.

Serial Interface

The MAX9951/MAX9952 use a standard 3-wire SPI/QSPI™/MICROWIRE™-compatible serial port. Once the input data register fills, the data becomes available at DOUT MSB first. This data output allows for daisy-chaining multiple devices. Figures 1, 2, and 3 show the serial interface timing diagrams.

Serial Port Operation

The serial interface has two ranks (Figure 4). Each PMU has an input register that loads from the serial port shift register. Each PMU also has a PMU register that loads from the input register. Data does not affect the PMU until it reaches the PMU register. This register configuration permits loading of the PMU data into the input register at one time and then latching the input register data into the PMU register later, at which time the PMU function changes accordingly. The register configuration also provides the ability to change the state of the PMU asynchronously, with respect to the loading of that PMU's data into the serial port. Thus, the PMU easily updates simultaneously with other PMUs or other devices.

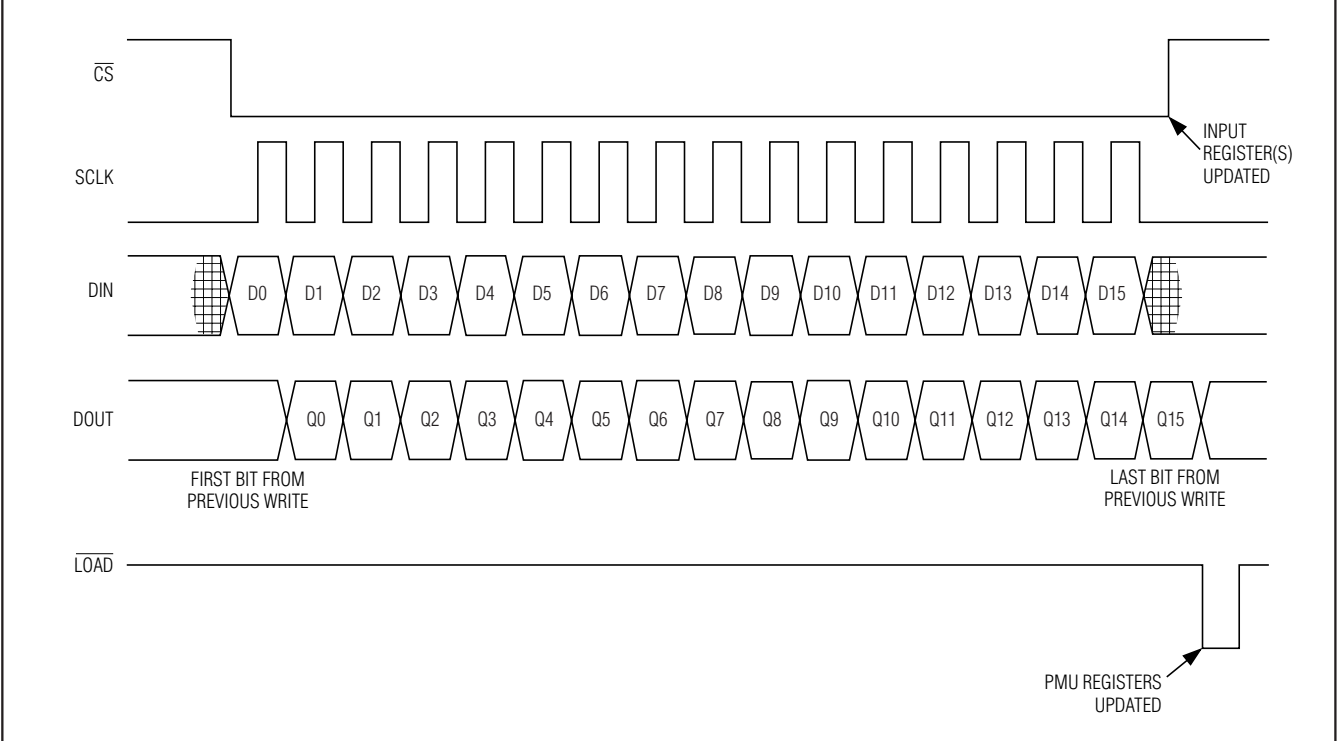


Figure 1. Serial Port Timing with Asynchronous Load

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Dual Per-Pin Parametric Measurement Units

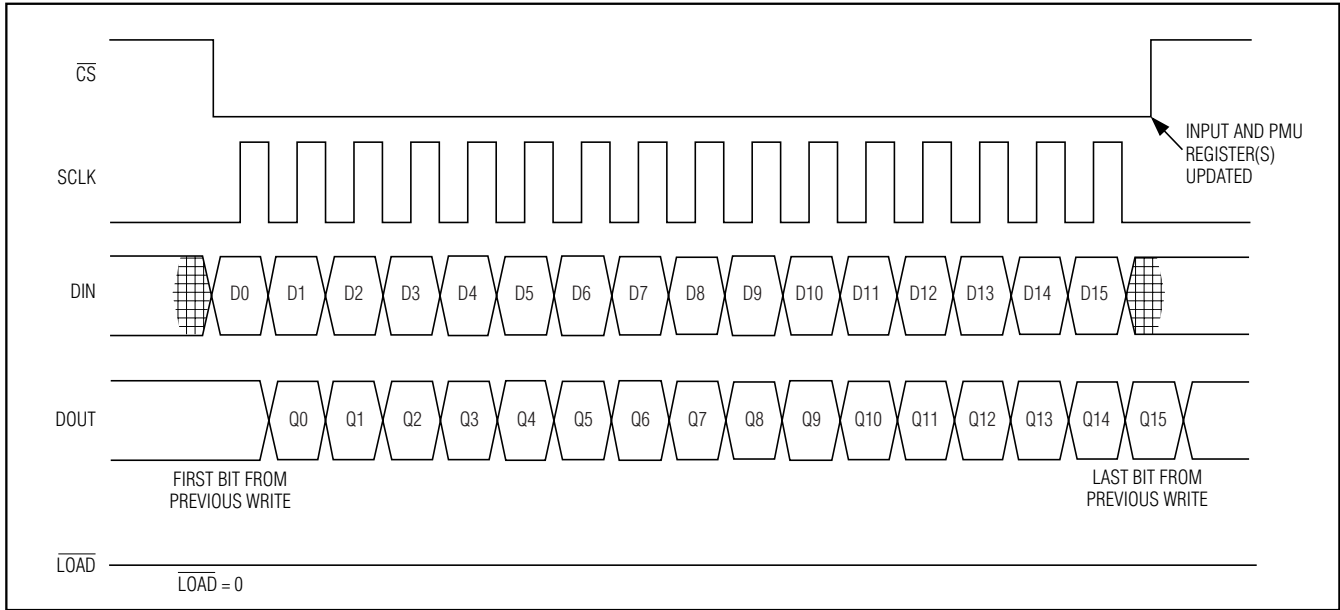


Figure 2. Serial Port Timing with Synchronous Load

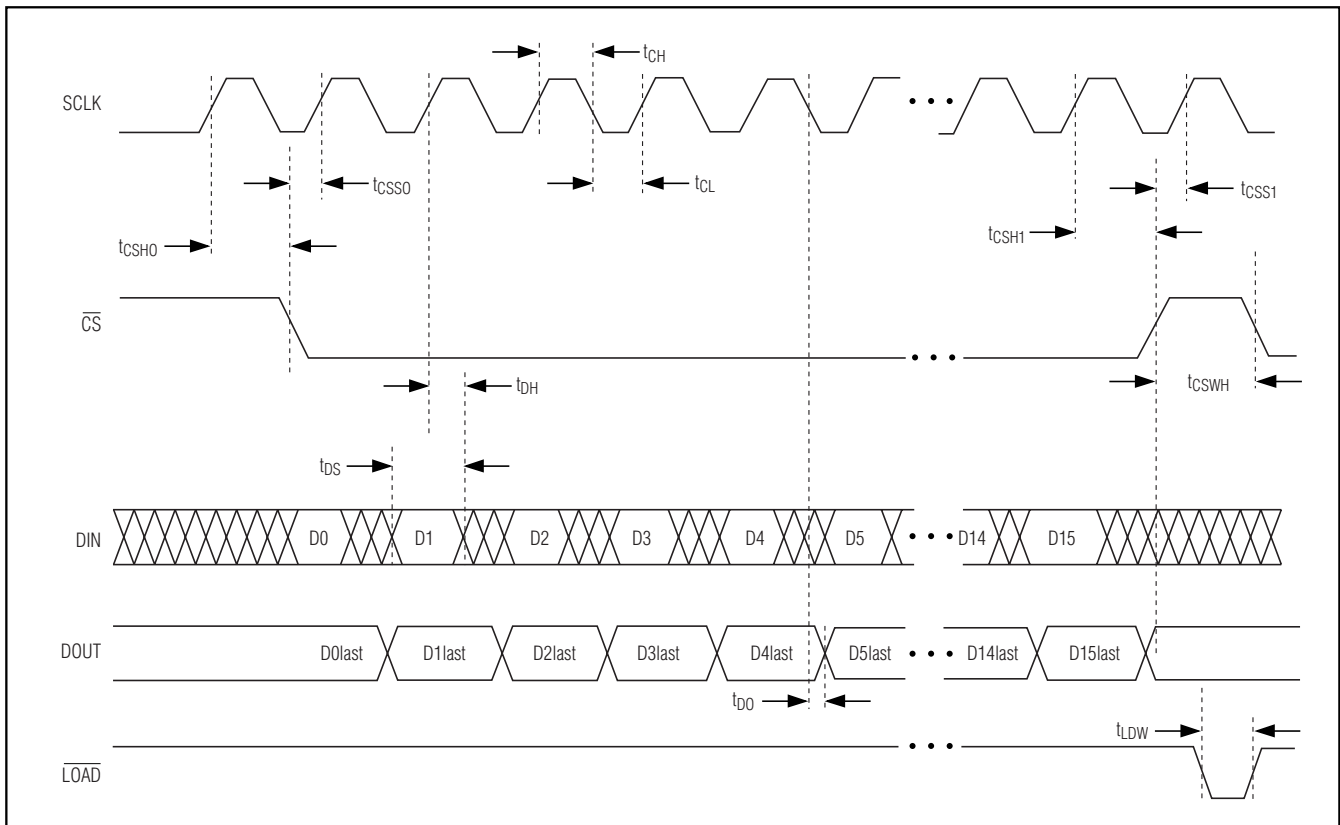


Figure 3. Detailed Serial Port Timing Diagram

Dual Per-Pin Parametric Measurement Units

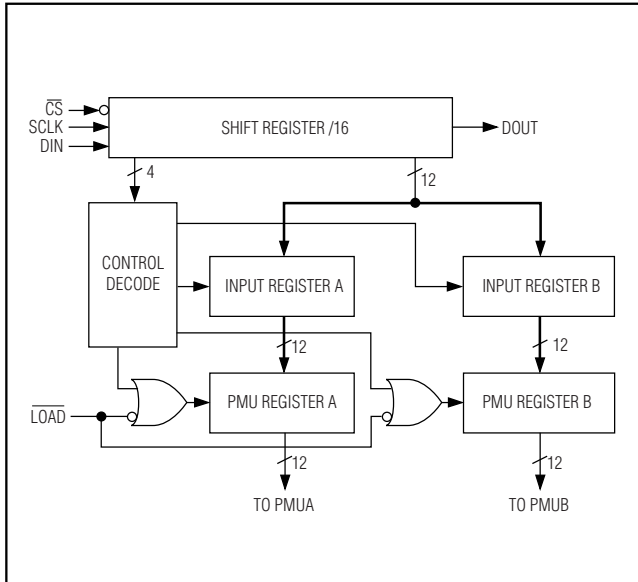


Figure 4. Dual PMU Serial Port Block Diagram

Use $\overline{\text{LOAD}}$ to asynchronously load all input registers into the PMU registers. If $\overline{\text{LOAD}}$ remains low when data latches into an input register, the data also transfers to the PMU register.

Bit Order

The MAX9951/MAX9952 use the bit order, MSB first in and first out, as shown in Table 1.

PMU Control

Programming both PMUs with the same data requires a 16-bit word. Programming each PMU with separate data requires two 16-bit words.

The address bits specify which input registers the shift-register loads. Table 2 describes the function of the address bits.

Bits C1 and C2 specify how the data loads into the second rank PMU registers. These 2 control bits serve a similar function as the $\overline{\text{LOAD}}$ input. The specified actions occur when $\overline{\text{CS}}$ goes high, whereas the $\overline{\text{LOAD}}$ input loads the PMU register at anytime. When either C1 or C2 is low, the corresponding PMU register is transparent. Table 3 describes the function of the 2 control bits.

The NOP operation requires $A1 = A2 = C1 = C2 = 0$. In this case, the data transfers through the shift register without changing the state of the device.

Table 1. Bit Order

BIT	BIT NAME
15 (MSB)	INMODE
14	FMODE
13	MMODE
12	RS2
11	RS1
10	RS0
9	CLENABLE
8	$\overline{\text{HI-ZFORCE}}$
7	$\overline{\text{HI-ZMSR}}$
6	$\overline{\text{DISABLE}}$
5	B2
4	B1
3	A2
2	A1
1	C2
0 (LSB)	C1

Table 2. Address Bit

(BIT 3) A2	(BIT 2) A1	OPERATION
0	0	Do not update any input register (NOP).
0	1	Only update input register A.
1	0	Only update input register B.
1	1	Update both input registers with the same data.

Table 3. Control Bit

(BIT 1) C2	(BIT 0) C1	OPERATION
0	0	Data stays in input register.
0	1	Transfer PMU-A input register to PMU register.
1	0	Transfer PMU-B input register to PMU register.
1	1	Transfer both input registers to the PMU registers.

Dual Per-Pin Parametric Measurement Units

C1 = C2 = 0 allows for data transfer from the shift register to the input register without transferring data to the PMU register (unless $\overline{\text{LOAD}}$ is low). This permits the latching of data into the PMU register at a later time by $\overline{\text{LOAD}}$ or subsequent command. Table 4 summarizes the possible control and address bit combinations. When asynchronously latching only one PMU's data, the input register of the other PMU maintains the same data. Therefore, loading both PMU registers would update the one PMU with new data while the other PMU remains in its current state.

Mode Selection

Four bits from the control word select between the various force-measure modes of operation. INMODE selects between the two input analog control voltages. FMODE selects whether the PMU forces a voltage or a current. MMODE selects whether the DUT current or DUT voltage is directed to MSR_. $\overline{\text{HI-ZFORCE}}$ places the driver amplifier in a high-output-impedance state. Table 5 describes the various force and measure modes of operation.

Table 4. PMU Operation Using Control and Address Bits

BIT (3:2)		BIT (1:0)		PMU-A OPERATION	PMU-B OPERATION
A2	A1	C2	C1		
0	0	0	0	NOP: data just passes through	
0	0	0	1	Transfer PMU register A from input register A.	NOP.
0	0	1	0	NOP.	Transfer PMU register B from input register B.
0	0	1	1	Transfer PMU register A from input register A.	Transfer PMU register B from input register B.
0	1	0	0	Transfer input register A from shift register.	NOP.
0	1	0	1	Transfer input register A and PMU register A from shift register.	NOP.
0	1	1	0	Transfer input register A from shift register.	Transfer PMU register B from input register B.
0	1	1	1	Transfer input register A and PMU register A from shift register.	Transfer PMU register B from input register B.
1	0	0	0	NOP.	Transfer input register B from shift register.
1	0	0	1	Transfer PMU register A from input register A.	Transfer input register B from shift register.
1	0	1	0	NOP.	Transfer input register B and PMU register B from shift register.
1	0	1	1	Transfer PMU register A from input register A.	Transfer input register B and PMU register B from shift register.
1	1	0	0	Transfer input register A from shift register.	Transfer input register B from shift register.
1	1	0	1	Transfer input register A and PMU register A from shift register.	Transfer input register B from shift register.
1	1	1	0	Transfer input register A from shift register.	Transfer input register B and PMU register B from shift register.
1	1	1	1	Transfer input register A and PMU register A from shift register.	Transfer input register B and PMU register B from shift register.

Dual Per-Pin Parametric Measurement Units

Table 5. PMU Force-Measure Mode Selection

(BIT 15) IN MODE*	(BIT 14) F MODE	(BIT 13) M MODE	(BIT 8) HI-ZFORCE	PMU MODE	FORCE OUTPUT	MEASURE OUTPUT	ACTIVE INPUT
0	0	1	1	FVMI	Voltage	IDUT	V _{IN0}
1	0	1	1	FVMI	Voltage	IDUT	V _{IN1}
0	0	0	1	FVMV	Voltage	VDUT	V _{IN0}
1	0	0	1	FVMV	Voltage	VDUT	V _{IN1}
0	1	1	1	FIMI	Current	IDUT	V _{IN0}
1	1	1	1	FIMI	Current	IDUT	V _{IN1}
0	1	0	1	FIMV	Current	VDUT	V _{IN0}
1	1	0	1	FIMV	Current	VDUT	V _{IN1}
X	0	1	0	FNMI (range E only)	High-Impedance	IDUT	X
X	0	0	0	FNMV	High-Impedance	VDUT	X
0	1	0	0	Termination	Voltage	VDUT	V _{IN0}
1	1	0	0	Termination	Voltage	VDUT	V _{IN1}
0	1	1	0	Termination	Voltage	IDUT	V _{IN0}
1	1	1	0	Termination	Voltage	IDUT	V _{IN1}

*INSEL = 0

Table 6. Current-Range Selection

(BIT 12) RS2	(BIT 11) RS1	(BIT 10) RS0	RANGE	NOMINAL RESISTOR VALUE (Ω)
0	0	X	±2μA	R _E = 500k
0	1	0	±20μA	R _D = 50k
0	1	1	±200μA	R _C = 5k
1	0	0	±2mA	R _B = 500
1	X	1	±64mA	R _A = 15.6
1	1	0	External	—

Table 7. MSR_o Output Truth Table

(BIT 7) HI-ZMSR	HI-Z _o	MSR _o
1	1	Measure output enabled
0	1	High-Impedance
1	0	High-Impedance
0	0	High-Impedance

Current-Range Selection

Three bits from the control word, RS0, RS1, and RS2, control the full-scale current range for either FI (force current) or MI (measure current). Table 6 describes the full-scale current-range control.

Clamp Enable

The CLENABLE bit enables the force-output-voltage clamps when high and disables the clamps when low. There is hysteresis equal to approximately 5% of the current range for clamp.

Measure Output High-Impedance Control

MSR_o attains a low-leakage, high-impedance state by using the HI-ZMSR control bit, or the HI-Z_o input. HI-Z_o is internally pulled up to V_L with a 1.5MΩ resistor. The 2 bits are logically ANDed together to control the MSR_o output. HI-Z_o allows external multiplexing among several PMU MSR_o outputs without using the serial interface. Table 7 explains the various output modes for the MSR_o output.

Digital Output (DOUT)

The digital output follows the last output of the serial-shift register and clocks out on the falling edge of SCLK. DOUT serially shifts the first bit of the incoming serial data word 16.5 clock cycles later. This allows for daisy-chaining additional devices using DOUT and the same clock.

Dual Per-Pin Parametric Measurement Units

A digital output decoded from the range select bits, EXTSEL_, indicates when to activate the booster. CCOM_ serves as an input to an external buffer through an internal 50Ω current-limit series resistor. Connect the external buffer output to the external current-sense resistor, R_EXT, and to R_X. Connect the other side of R_X to FORCE_. Ensure that the external switch is low leakage.

Voltage Clamps

The voltage clamps limit FORCE_ and operate over the entire specified current range. Set the clamp voltages externally at CLHI_ and CLLO_. The voltage at FORCE_ triggers the clamps independent of the voltage at SENSE_. When enabled, the clamps function in FI mode only. Use clamp voltages of 0.7V above and below the FORCE_ voltage range to ensure proper operation of the PMU.

Current Limit

The FORCE_ current-limiting circuitry, 92mA (maximum), ensures a well-behaved MSR_ output for currents between the full current range and the current limits. For currents greater than the full-scale current, the MSR_ voltage is greater than +4V, and for currents less than the full-scale current, the MSR_ voltage is less than -4V. Additionally, serial interface bit B2 enables a range-sensitive current limit of 2.5 times the nominal current range. Table 9 shows the current-limit operation.

Independent Control of the Feedback Switch and the Measure Switch

Two single-pole-double-throw (SPDT) switches determine the mode of operation of the PMU. One switch determines whether the sensed DUT current or DUT voltage feeds back to the input, and thus determines whether the MAX9951/MAX9952 force current or voltage. The other switch determines whether MSR_ senses the DUT current or DUT voltage.

Table 9. Current Limit

FMODE	RANGE	B2 (BIT 5)	CURRENT LIMIT
X	Any	0	65mA to 92mA
0	A	1	65mA to 92mA
0	B	1	5mA
0	C	1	500μA
0	D	1	50μA
0	E	1	5μA

Independent control of these switches and the HI-ZFORCE state permits flexible modes of operation beyond the traditional force-voltage/measure-current (FVMI) and force-current/measure-voltage (FIMV) modes. The MAX9951/MAX9952 support the following eight modes:

- FVMI
- FIMV
- FVMV
- FIMI
- FNMV
- FNMI (range E only)
- Terminate/Measure V
- Terminate/Measure I

Figure 6 shows the internal path structure for force-voltage/measure-current mode. In force-voltage/measure-current mode, the current across the appropriate external sense resistor (R_A to R_E) provides a voltage at MSR_. SENSE_ samples the voltage at the DUT and feeds the buffered result back to the negative input of the voltage amplifier. The voltage at MSR_ is proportional to the FORCE_ current in accordance with the following formula:

$$V_{MSR_} = I_{FORCE_} \times R_{SENSE} \times 4$$

Figure 7 shows the internal path structure for the force-current/measure-voltage mode. In force-current/measure-voltage mode, the appropriate external sense resistor (R_A to R_E) provides a feedback voltage to

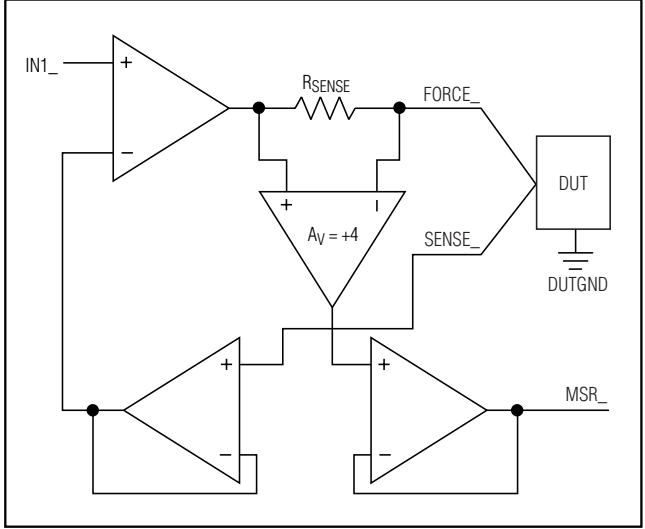


Figure 6. Force-Voltage/Measure-Current Functional Diagram

Dual Per-Pin Parametric Measurement Units

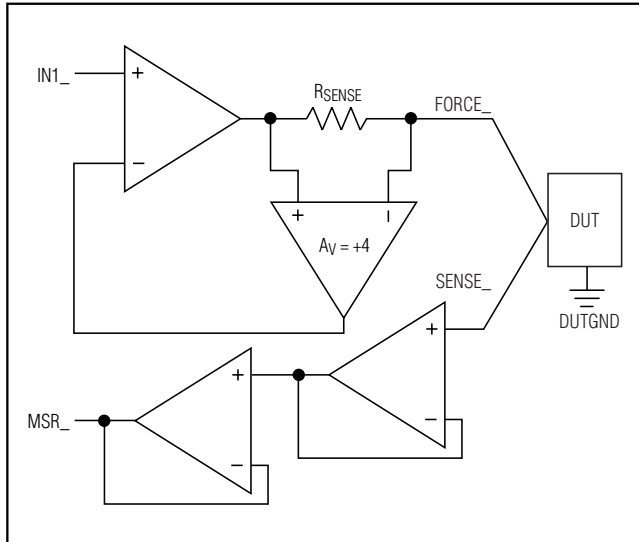


Figure 7. Force-Current/Measure-Voltage Functional Diagram

the inverting input of the voltage amplifier. SENSE_ samples the voltage at the DUT and provides a buffered result at MSR_.

High-Impedance States

The FORCE_, MSR_, and comparator outputs feature individual high-impedance control that places them into a high-impedance, low-leakage state. The high-impedance state allows busing of MSR_ and comparator outputs with other PMU measure and comparator outputs. The FORCE_ output high-impedance state allows for additional modes of operation as described in Table 5 and can eliminate the need for a series relay in some applications.

The FORCE_, MSR_, and comparator outputs power up in the high-impedance state.

Input Source Selection

Either one of two input signals, IN0_ or IN1_, can control both the forced voltage and the forced current. In this case, the two input signals represent alternate forcing values that can be selected either with the serial interface or INSEL_. Alternatively, each input signal can be dedicated to control a single forcing function (i.e., voltage or current).

Short-Circuit Protection

FORCE_ and SENSE_ input can withstand a short to any voltage between the supply rails.

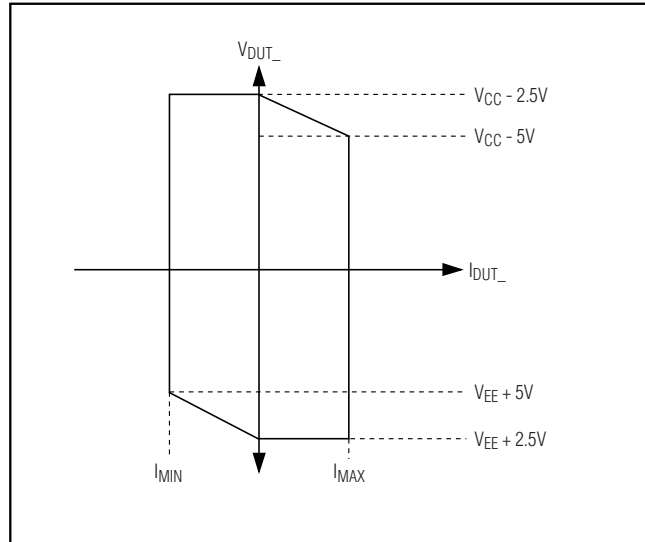


Figure 8. PMU Force-Output Capability

Mode and Range Change Transients

The MAX9951/MAX9952 feature make-before-break switching to minimize glitches. The integrated voltage clamps also reduce glitching at the output.

DUT Voltage Swing vs. DUT Current and Power-Supply Voltages

Several factors limit the actual DUT voltage that the PMU delivers:

- The overhead required by the device amplifiers and other integrated circuitry; this is typically 2.5V from each rail independent of load.
- The voltage drop across the current-range select resistor and internal circuitry in series with the sense resistor. At full current, the combined voltage drop is typically 2.5V.
- Variations in the power supplies.
- Variation of DUT ground vs. PMU ground.

Neglecting the effects of the third and fourth items, Figure 8 demonstrates the force-output capabilities of the PMU. For zero DUT current, the DUT voltage swings from (V_{EE} + 2.5V) to (V_{CC} - 2.5V). For larger positive DUT currents, the positive swing drops off linearly until it reaches (V_{CC} - 5V) at full current. Similarly, for larger negative DUT currents, the negative voltage swing drops off linearly until it reaches (V_{EE} + 5V) at full current.

Dual Per-Pin Parametric Measurement Units

Ground, DUT Ground, and IOS

The MAX9951/MAX9952 utilize two local grounds, AGND (analog ground) and DGND (digital ground). Connect AGND and DGND together on the PC board. In a typical ATE system, the PMU force voltage is relative to DUT ground. In this case, reference the input voltages IN0_ and IN1_ to DUT ground. Similarly, reference IOS to DUT ground. If it is not desired to offset the current control and measure voltages, connect IOS to DUT ground potential.

Reference the MSR_ output to DUT ground.

Settling Times and Compensation Capacitors

The data in the *Electrical Characteristics* table reflects the circuit shown in the *Functional Diagram* that includes a single compensation capacitor (CX_) effectively across all the sense resistors. Placing individual capacitors, CRA, CRB, CRC, CRD, and CRE directly across the sense resistors, R_A, R_B, R_C, R_D, and R_E, independently optimizes each range.

The combination of the capacitance across the sense resistors, along with the main amplifier compensation comparator, CM_, ensures stability into the maximum expected load capacitance while optimizing settling time for a given load.

Digital Inputs (SCLK, DIN, CS, and LOAD)

The digital inputs incorporate hysteresis to mitigate issues with noise, as well as provide for compatibility with opto-isolators that can have slow edges.

Temperature Monitor

Each device supplies a single temperature output signal, TEMP, that asserts a nominal output voltage of 2.98V at a die temperature of +25°C (298K). The output voltage increases proportionately with temperature at a rate of 10mV/°C. The temperature sensor output impedance is 15kΩ (typ). Determine the die temperature using:

$$T_{DIE} = (100) \times V_{TEMP} - 273 \text{ [}^\circ\text{C]}$$

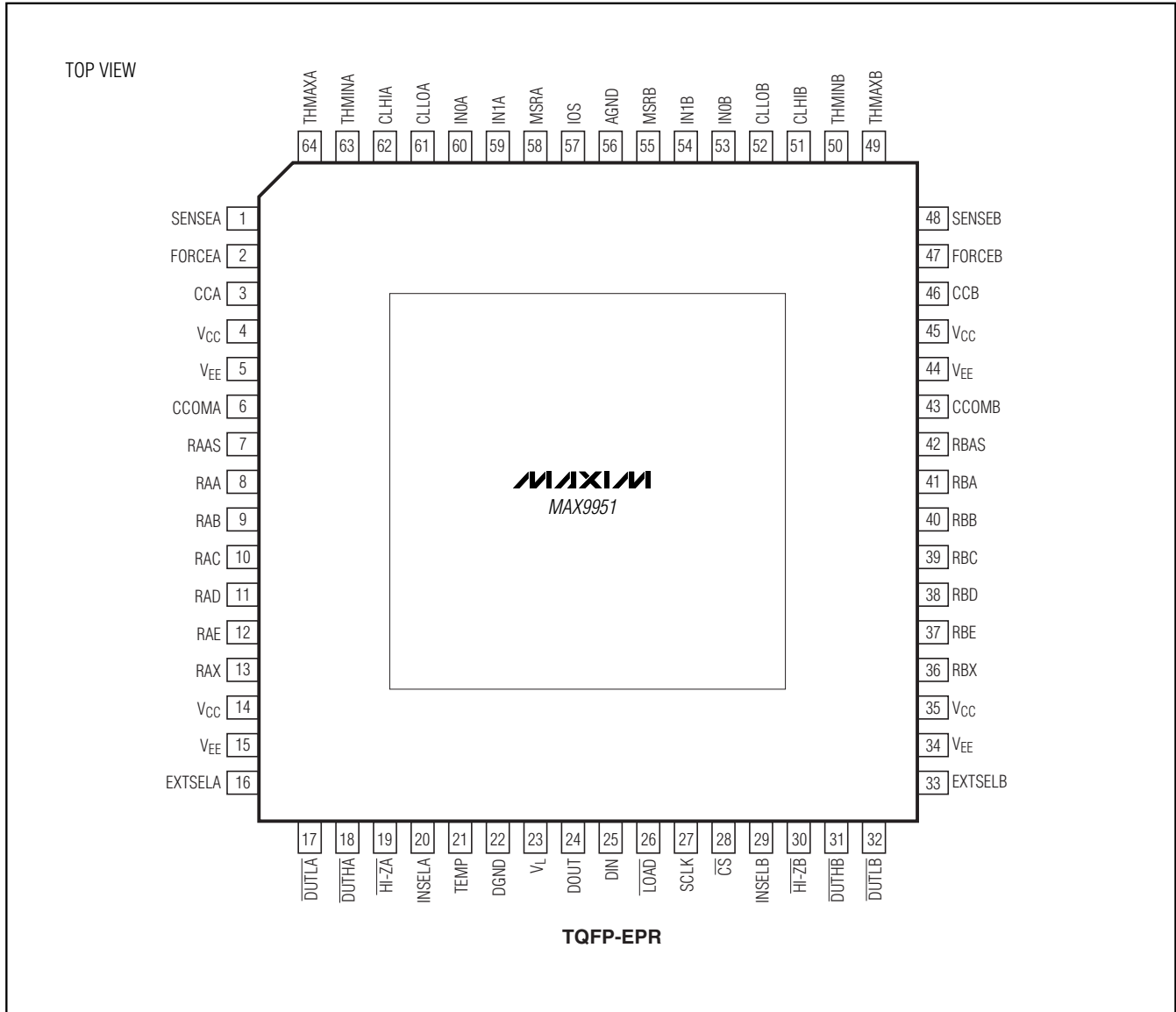
Chip Information

TRANSISTOR COUNT: 11,000

PROCESS: BICMOS

Dual Per-Pin Parametric Measurement Units

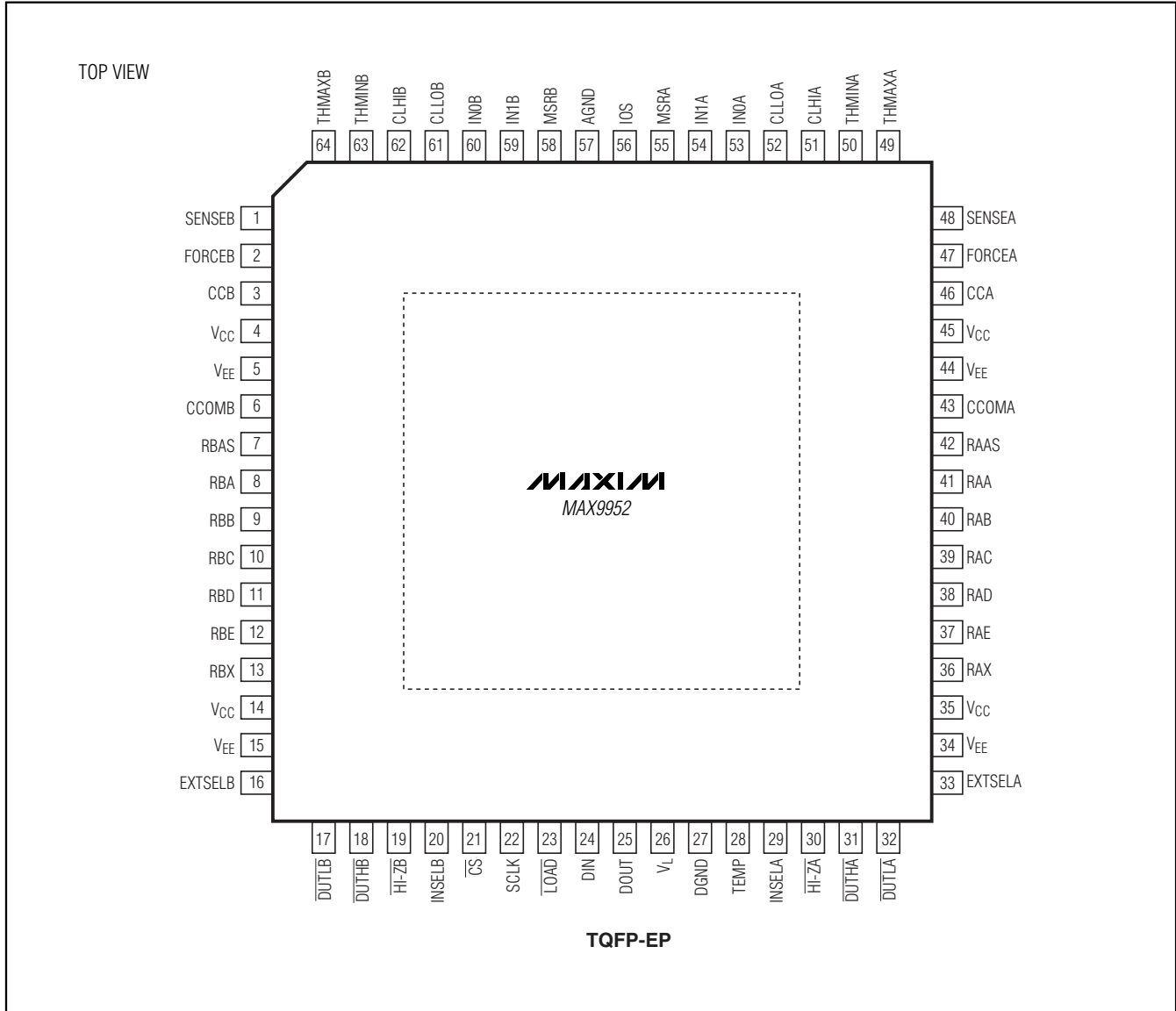
Pin Configurations



Dual Per-Pin Parametric Measurement Units

Pin Configurations (continued)

MAX9951/MAX9952



Package Information

For the latest package outline information, go to www.maxim-ic.com/packages.

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