HD74LV374A

Octal Edge-Triggered D-type Flip-Flops with 3-state Outputs

REJ03D0332–0200Z
(Previous ADE-205-275 (Z))
Rev.2.00
Jun. 25, 2004

Description

The HD74LV374A has eight edge trigger D type flip flops with three state outputs in a 20 pin package. Data at the D inputs meeting set up requirements, are transferred to the Q outputs on positive going transitions of the clock input. When the clock input goes low, data at the D inputs will be retained at the outputs until clock input returns high again. When a high logic level is applied to the output control input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements. Low-voltage and high-speed operation is suitable for the battery-powered products (e.g., notebook computers), and the low-power consumption extends the battery life.

Features

- V_{CC} = 2.0 V to 5.5 V operation
- All inputs V_{IH} (Max.) = 5.5 V (@V_{CC} = 0 V to 5.5 V)
- All outputs V_O (Max.) = 5.5 V (@V_{CC} = 0 V)
- Typical V_{OL} ground bounce < 0.8 V (@V_{CC} = 3.3 V, Ta = 25°C)
- Typical V_{OH} undershoot > 2.3 V (@V_{CC} = 3.3 V, Ta = 25°C)
- Output current ±8 mA (@V_{CC} = 3.0 V to 3.6 V), ±16 mA (@V_{CC} = 4.5 V to 5.5 V)
- Ordering Information

Part Name	Package Type	Package Code	Package Abbreviation	Taping Abbreviation (Quantity)
HD74LV374AFPEL	SOP–20 pin (JEITA)	FP–20DAV	FP	EL (2,000 pcs/reel)
HD74LV374ARPEL	SOP–20 pin (JEDEC)	FP–20DBV	RP	EL (1,000 pcs/reel)
HD74LV374ATELL	TSSOP–20 pin	TTP–20DAV	T	ELL (2,000 pcs/reel)

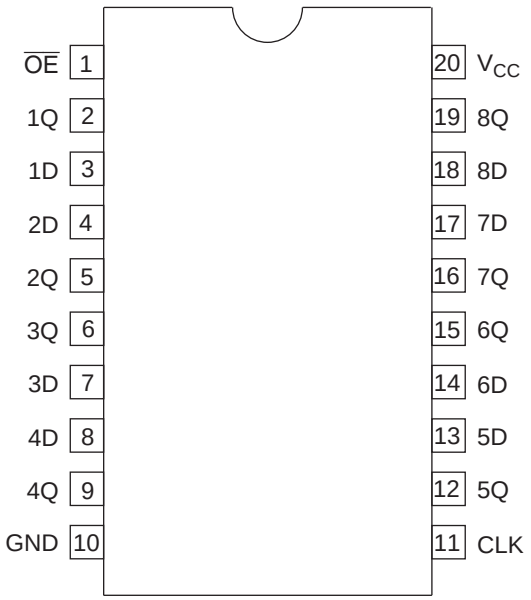
Note: Please consult the sales office for the above package availability.

Function Table

Inputs			
$\overline{OE}$	CLK	D	Output Q
H	X	X	Z
L	↑	L	L
L	↑	H	H
L	↓	X	Q_0

Note: H: High level
L: Low level
X: Immaterial
Z: High impedance
Q_0: Output level before the indicated steady state input conditions were established.

Pin Arrangement



(Top view)

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Conditions
Supply voltage range	V_{CC}	–0.5 to 7.0	V	
Input voltage range*[1]	V_I	–0.5 to 7.0	V	
Output voltage range*[1, 2]	V_O	–0.5 to V_{CC} + 0.5	V	Output: H or L
		–0.5 to 7.0		V_{CC}: OFF or Output: Z
Input clamp current	I_{IK}	–20	mA	$V_I < 0$
Output clamp current	I_{OK}	±50	mA	$V_O < 0$ or $V_O > V_{CC}$
Continuous output current	I_O	±35	mA	V_O = 0 to V_{CC}
Continuous current through V_{CC} or GND	I_{CC} or I_{GND}	±70	mA	
Maximum power dissipation at Ta = 25°C (in still air)*[3]	P_T	835	mW	SOP
		757		TSSOP
Storage temperature	Tstg	–65 to 150	°C	

Notes: The absolute maximum ratings are values, which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

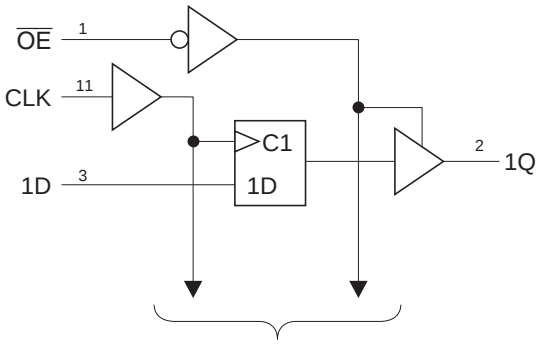
1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 5.5 V maximum.
3. The maximum package power dissipation was calculated using a junction temperature of 150°C.

Recommended Operating Conditions

Item	Symbol	Min	Max	Unit	Conditions
Supply voltage range	V_{CC}	2.0	5.5	V	
Input voltage range	V_I	0	5.5	V	
Output voltage range	V_O	0	V_{CC}	V	H or L
		0	5.5		High impedance state
Output current	I_{OH}	—	–50	μA	V_{CC} = 2.0 V
		—	–2	mA	V_{CC} = 2.3 to 2.7 V
		—	–8		V_{CC} = 3.0 to 3.6 V
		—	–16		V_{CC} = 4.5 to 5.5 V
	I_{OL}	—	50	μA	V_{CC} = 2.0 V
		—	2	mA	V_{CC} = 2.3 to 2.7 V
		—	8		V_{CC} = 3.0 to 3.6 V
		—	16		V_{CC} = 4.5 to 5.5 V
Input transition rise or fall rate	Δt /Δv	0	200	ns/V	V_{CC} = 2.3 to 2.7 V
		0	100		V_{CC} = 3.0 to 3.6 V
		0	20		V_{CC} = 4.5 to 5.5 V
Operating free-air temperature	Ta	–40	85	°C	

Note: Unused or floating inputs must be held high or low.

Logic Diagram



DC Electrical Characteristics

Ta = –40 to 85°C

Item	Symbol	V_{CC} (V)*	Min	Typ	Max	Unit	Test Conditions
Input voltage	V_{IH}	2.0	1.5	—	—	V	
		2.3 to 2.7	$V_{CC} \times 0.7$	—	—		
		3.0 to 3.6	$V_{CC} \times 0.7$	—	—		
		4.5 to 5.5	$V_{CC} \times 0.7$	—	—		
	V_{IL}	2.0	—	—	0.5		
		2.3 to 2.7	—	—	$V_{CC} \times 0.3$		
		3.0 to 3.6	—	—	$V_{CC} \times 0.3$		
		4.5 to 5.5	—	—	$V_{CC} \times 0.3$		
Output voltage	V_{OH}	Min to Max	V_{CC} – 0.1	—	—	V	I_{OH} = –50 µA
		2.3	2.0	—	—		I_{OH} = –2 mA
		3.0	2.48	—	—		I_{OH} = –8 mA
		4.5	3.8	—	—		I_{OH} = –16 mA
	V_{OL}	Min to Max	—	—	0.1		I_{OL} = 50 µA
		2.3	—	—	0.4		I_{OL} = 2 mA
		3.0	—	—	0.44		I_{OL} = 8 mA
		4.5	—	—	0.55		I_{OL} = 16 mA
Input current	I_{IN}	0 to 5.5	—	—	±1	µA	V_{IN} = 5.5 V or GND
Off-state output current	I_{OZ}	5.5	—	—	±5	µA	V_O = V_{CC} or GND
Quiescent supply current	I_{CC}	5.5	—	—	20	µA	V_{IN} = V_{CC} or GND, I_O = 0
Output leakage current	I_{OFF}	0	—	—	5	µA	V_I or V_O = 0 to 5.5 V
Input capacitance	C_{IN}	3.3	—	2.9	—	pF	V_I = V_{CC} or GND

Note: For conditions shown as Min or Max, use the appropriate values under recommended operating conditions.

Switching Characteristics

V_{CC} = 2.5 ± 0.2 V

Item	Symbol	Ta = 25°C			Ta = –40 to 85°C		Unit	Test Conditions	FROM (Input)	TO (Output)
		Min	Typ	Max	Min	Max				
Maximum clock frequency	t_{max}	60	105	—	50	—	MHz	C_L = 15 pF		
		50	85	—	40	—		C_L = 50 pF		
Propagation delay time	t_{PLH}	—	9.7	16.3	1.0	19.0	ns	C_L = 15 pF	CLK	Q
	t_{PHL}	—	11.8	19.3	1.0	23.0		C_L = 50 pF		
Enable time	t_{ZH}	—	8.9	15.9	1.0	19.0	ns	C_L = 15 pF	$\overline{OE}$	Q
	t_{ZL}	—	10.9	18.8	1.0	22.0		C_L = 50 pF		
Disable time	t_{HZ}	—	6.3	12.6	1.0	15.0	ns	C_L = 15 pF	$\overline{OE}$	Q
	t_{LZ}	—	8.2	17.3	1.0	19.0		C_L = 50 pF		
Setup time	t_{SU}	5.0	—	—	5.5	—	ns		Data before CLK ↑	
Hold time	t_h	2.5	—	—	2.5	—	ns		Data after CLK ↑	
Pulse width	t_w	6.0	—	—	7.0	—	ns		CLK: "H" or "L"	

V_{CC} = 3.3 ± 0.3 V

Item	Symbol	Ta = 25°C			Ta = –40 to 85°C		Unit	Test Conditions	FROM (Input)	TO (Output)
		Min	Typ	Max	Min	Max				
Maximum clock frequency	t_{max}	80	150	—	70	—	MHz	C_L = 15 pF		
		55	110	—	50	—		C_L = 50 pF		
Propagation delay time	t_{PLH}	—	6.8	12.7	1.0	15.0	ns	C_L = 15 pF	CLK	Q
	t_{PHL}	—	8.3	16.2	1.0	18.5		C_L = 50 pF		
Enable time	t_{ZH}	—	6.3	11.0	1.0	13.0	ns	C_L = 15 pF	$\overline{OE}$	Q
	t_{ZL}	—	7.7	14.5	1.0	16.5		C_L = 50 pF		
Disable time	t_{HZ}	—	4.7	10.5	1.0	12.5	ns	C_L = 15 pF	$\overline{OE}$	Q
	t_{LZ}	—	5.9	14.0	1.0	16.0		C_L = 50 pF		
Setup time	t_{SU}	4.5	—	—	4.5	—	ns		Data before CLK ↑	
Hold time	t_h	2.0	—	—	2.0	—	ns		Data after CLK ↑	
Pulse width	t_w	5.0	—	—	5.5	—	ns		CLK: "H" or "L"	

V_{CC} = 5.0 ± 0.5 V

Item	Symbol	Ta = 25°C			Ta = –40 to 85°C		Unit	Test Conditions	FROM (Input)	TO (Output)
		Min	Typ	Max	Min	Max				
Maximum clock frequency	t_{max}	130	205	—	110	—	MHz	C_L = 15 pF		
		85	170	—	75	—		C_L = 50 pF		
Propagation delay time	t_{PLH}	—	4.9	8.1	1.0	9.5	ns	C_L = 15 pF	CLK	Q
	t_{PHL}	—	5.9	10.1	1.0	11.5		C_L = 50 pF		
Enable time	t_{ZH}	—	4.6	7.6	1.0	9.0	ns	C_L = 15 pF	$\overline{OE}$	Q
	t_{ZL}	—	5.5	9.6	1.0	11.0		C_L = 50 pF		
Disable time	t_{HZ}	—	3.4	6.8	1.0	8.0	ns	C_L = 15 pF	$\overline{OE}$	Q
	t_{LZ}	—	4.0	8.8	1.0	10.0		C_L = 50 pF		
Setup time	t_{SU}	3.0	—	—	3.0	—	ns		Data before CLK ↑	
Hold time	t_h	2.0	—	—	2.0	—	ns		Data after CLK ↑	
Pulse width	t_w	5.0	—	—	5.0	—	ns		CLK: "H" or "L"	

Output-skew Characteristics

C_L = 50 pF

Item	Symbol	V_{CC} = (V)	Ta = 25°C		Ta = –40 to 85°C		Unit
			Min	Max	Min	Max	
Output skew	$t_{sk\ (O)}$	2.3 to 2.7	—	2.0	—	2.0	ns
		3.0 to 3.6	—	1.5	—	1.5	
		4.5 to 5.5	—	1.0	—	1.0	

Note: Skew between any outputs of the same package switching in the same direction. This parameter is warranted but not production tested.

Operating Characteristics

C_L = 50 pF

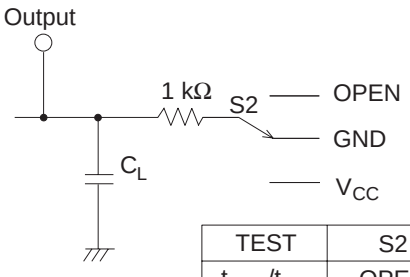
Item	Symbol	V_{CC} = (V)	Ta = 25°C			Unit	Test Conditions
			Min	Typ	Max		
Power dissipation capacitance	C_{PD}	3.3	—	21.1	—	pF	f = 10 MHz
		5.0	—	22.8	—		

Noise Characteristics

C_L = 50 pF

Item	Symbol	V_{CC} = (V)	Ta = 25°C			Unit	Test Conditions
			Min	Typ	Max		
Quiet output, maximum dynamic V_{OL}	$V_{OL\ (P)}$	3.3	—	0.6	0.8	V	
Quiet output, minimum dynamic V_{OL}	$V_{OL\ (V)}$	3.3	—	–0.5	–0.8	V	
Quiet output, minimum dynamic V_{OH}	$V_{OH\ (V)}$	3.3	—	2.9	—	V	
High-level dynamic input voltage	$V_{IH\ (D)}$	3.3	2.31	—	—	V	
Low-level dynamic input voltage	$V_{IL\ (D)}$	3.3	—	—	0.99	V	

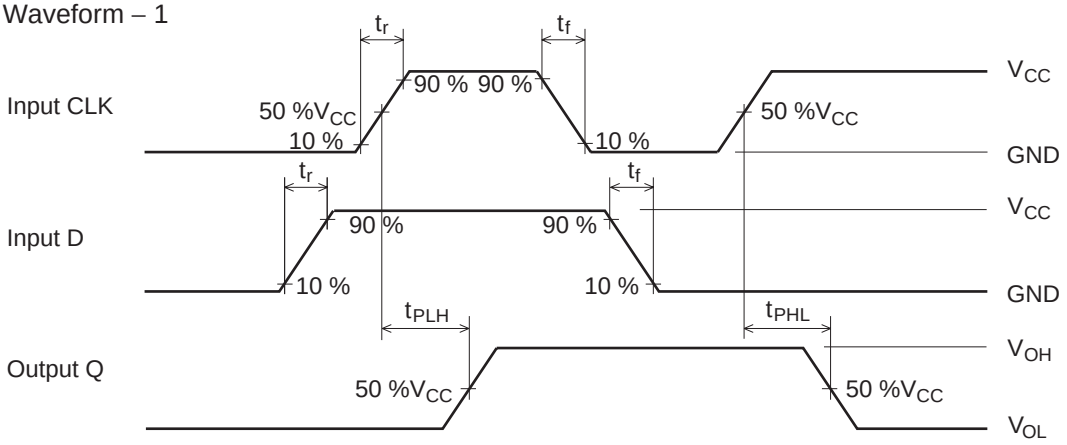
Test Circuit



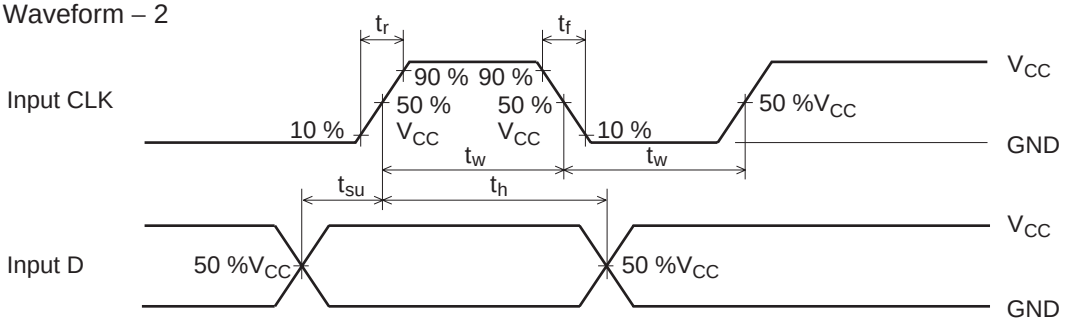
TEST	S2
t_{PLH}/t_{PHL}	OPEN
t_{ZH}/t_{HZ}	GND
t_{ZL}/t_{LZ}	V_{CC}

Note: C_L includes the probe and jig capacitance.

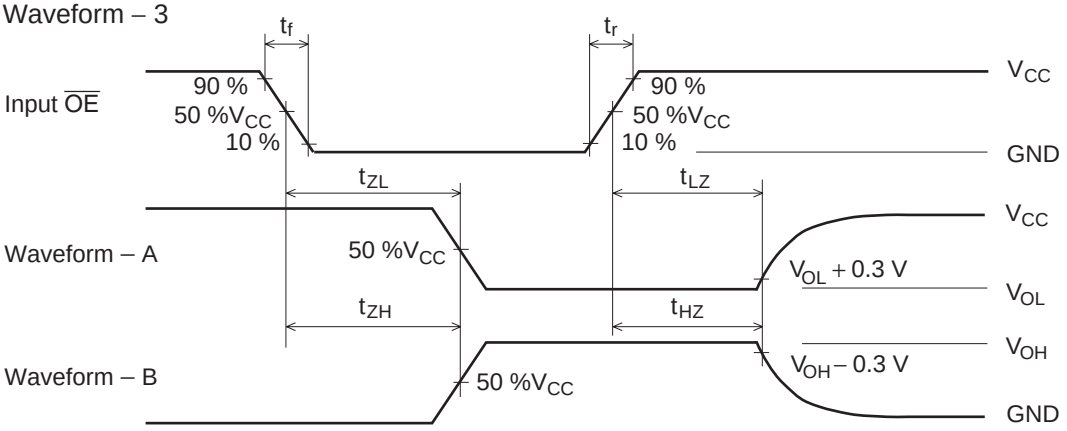
• Waveform – 1



• Waveform – 2



• Waveform – 3

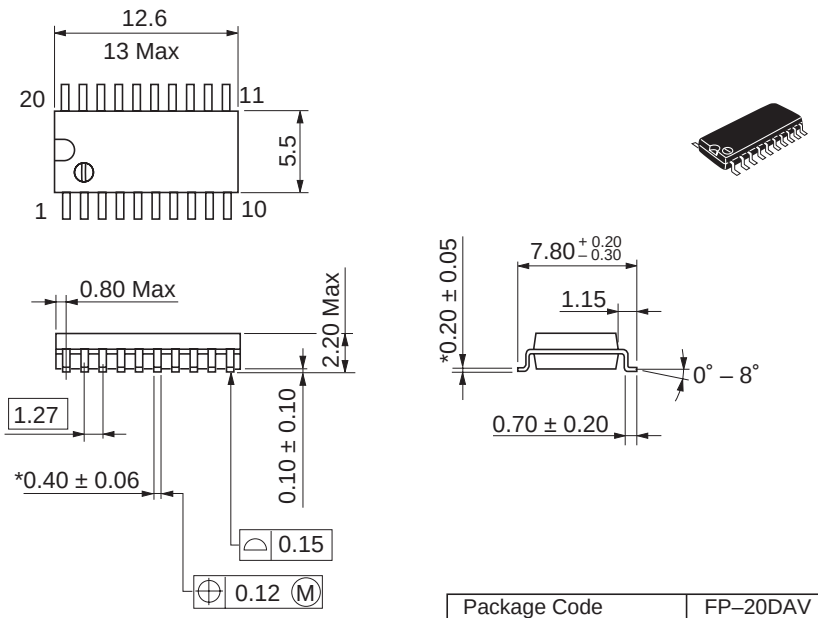


Notes: 1. $t_r \leq 3$ ns, $t_f \leq 3$ ns
2. Input waveform: PRR ≤ 1 MHZ, duty cycle 50%
3. Waveform–A is for an output with internal conditions such that the output is low except when disabled by the output control.
4. Waveform–B is for an output with internal conditions such that the output is high except when disabled by the output control.

Package Dimensions

As of January, 2002

Unit: mm

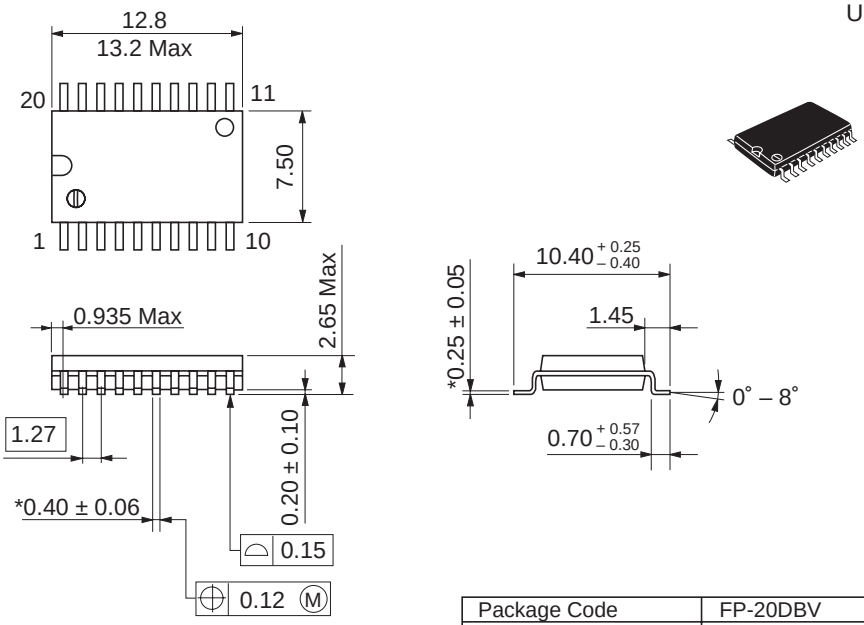


*Pd plating

Package Code	FP–20DAV
JEDEC	—
JEITA	Conforms
Mass (reference value)	0.31 g

As of January, 2003

Unit: mm

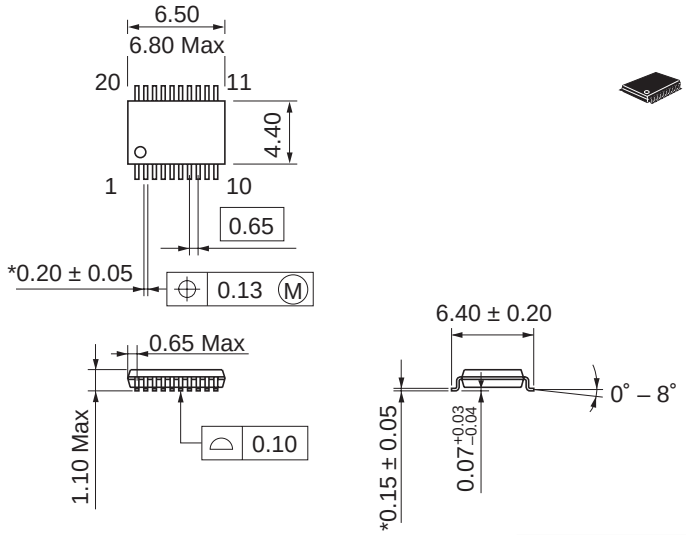


*Ni/Pd/Au plating

Package Code	FP-20DBV
JEDEC	Conforms
JEITA	—
Mass (reference value)	0.52 g

As of January, 2002

Unit: mm



Package Code	TTP–20DAV
JEDEC	—
JEITA	—
Mass (reference value)	0.07 g

*Pd plating

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