L4993

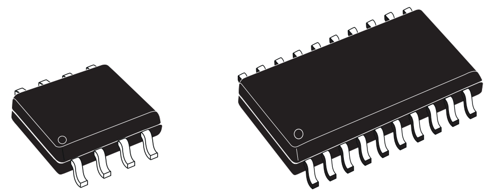
Low drop voltage regulator

Features

Max DC supply voltage	V_S	40V
Max output voltage tolerance	ΔV_0	+/-2%
Max dropout voltage	V_{dp}	400 mV
Output current	I_0	150 mA
Quiescent current	I_{qn}	79 µA(1)

1. Typical value with watchdog disabled.

- Operating DC supply voltage range 5.6V to 31V
- Reset circuit sensing the output voltage down to 1V
- Programmable reset pulse delay with external capacitor
- Watchdog
- Programmable watchdog timer with external capacitor
- Enable input for enabling/disabling the watchdog functionality
- Thermal shutdown and short circuit protection
- Wide temperature range (T_j = -40°C to 150°C)



SO-8 SO-20

Description

The L4993 is a monolithic integrated 5V Voltage regulator with a low drop voltage at currents up to 150mA.The output voltage regulating element consists in a p-channel MOS and the regulation is performed regardless of input voltage transients up to 40V. The high precision of the output voltage is obtained with a pre-trimmed reference voltage. The L4993 is protected against short circuit and an over-temperature protection switches off the device in case of extremely high power dissipation. The L4993 watchdog is active when the Enable is high. State of the art features like reset and watchdog make this device particularly suitable to supply microprocessor systems in automotive applications.

Table 1. Device summary

Package	Order codes	
	Tube	Tape & reel
SO-8	L4993D	L4993DTR
SO-20 (16+2+2)	L4993MD	L4993MDTR

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1 Block diagram and pins description

Figure 1. Block diagram

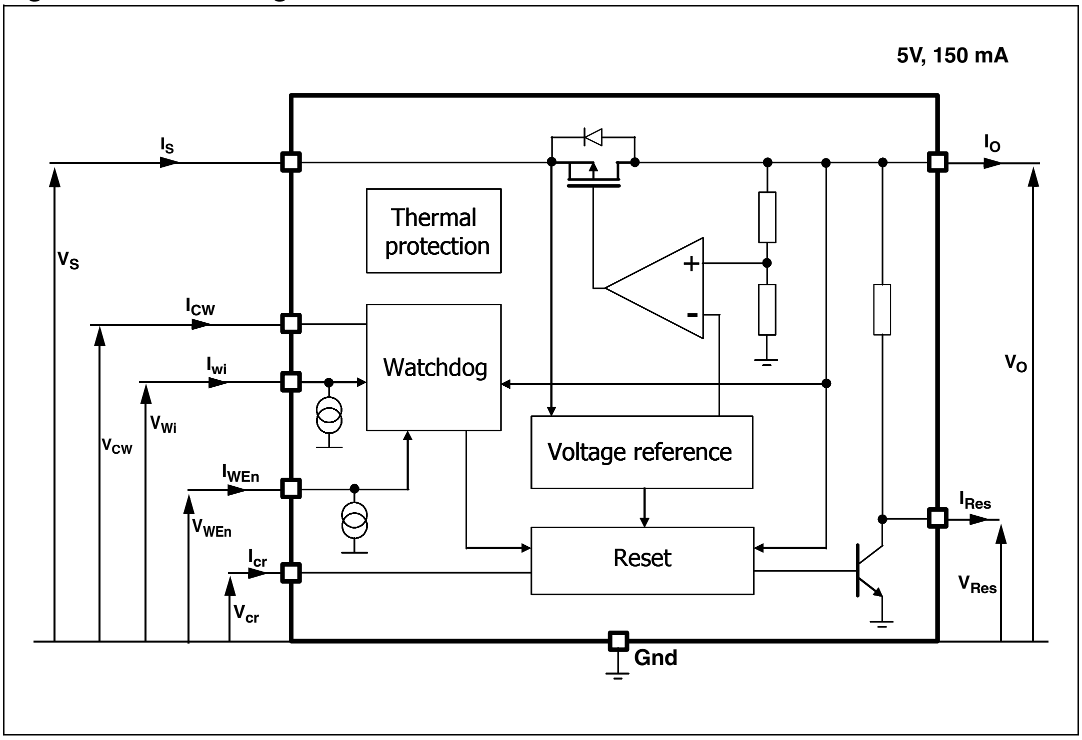
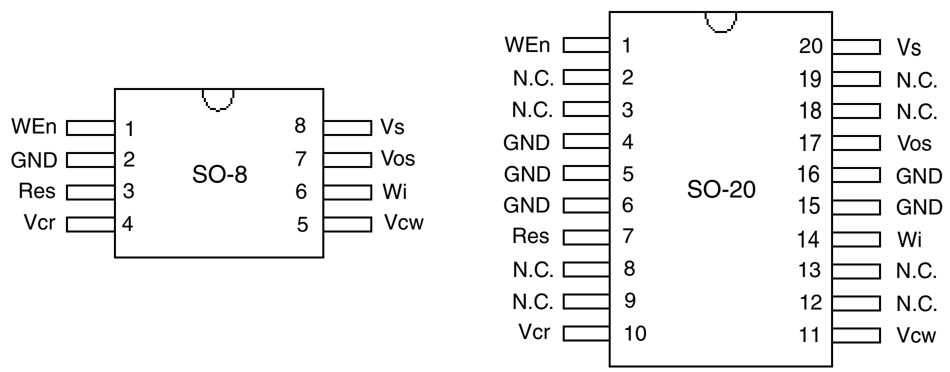


Table 2. **Pins description**

Pin name	SO-8 (D)	SO-20 (MD)	Function
WEn	1	1	Watchdog Enable input If high watchdog functionality is active
Gnd	2	4	Ground reference
Gnd		5, 6, 15, 16	Ground Connected these pins to a heat spreader ground
Res	3	7	Reset output. It is pulled down when output voltage goes below Vo_th or frequency at Wi is too low. Leave floating if not used.
Vcr	4	10	Reset timing adjust. A capacitor between Vcr pin and gnd, sets the reset delay time (trd)
Vcw	5	11	Watchdog timer adjust A capacitor between Vcw pin and gnd, sets the time response of the watchdog monitor.
Wi	6	14	Watchdog input. If the frequency at this input pin is too low, the Reset output is activated. Connect to ground if not used
Vo_S	7	17	Voltage regulator output Block to ground with a capacitor >100nF (needed for regulator stability)
Vs	8	20	Supply voltage Block to ground directly at IC pin with a capacitor
N.C.		2, 3, 8, 9, 12, 13, 18, 19	Not connected

Figure 2. **Pins configuration**



2 Electrical specifications

2.1 Absolute maximum ratings

Stressing the device above the rating listed in the “Absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{Vsdc}	DC supply voltage	-0.3 to 40	V
I_{Vsdc}	Input current	Internally limited	
V_{Vo}	DC output voltage	-0.3 to 6	V
I_{Vo}	DC output current	Internally limited	
V_{Wi}	Watchdog input voltage	-0.3 to V_{Vo} + 0.3	V
V_{od}	Open drain output voltage	-0.3 to V_{Vo} + 0.3	V
I_{od}	Open drain output current	Internally limited	
V_{cr}	Reset delay voltage	-0.3 to V_{Vo} + 0.3	V
V_{cw}	Watchdog delay voltage	-0.3 to V_{Vo} + 0.3	V
V_{WEn}	Watchdog Enable input voltage	-0.3 to V_{Vo} +0.3	V
T_j	Junction temperature	-40 to 150	°C
V_{ESD}	ESD voltage level (HBM-MIL STD 883C)	±2	kV
V_{ESD}	ESD voltage level (CDM AEC-Q100-011)	750	V

Note: Maximum ratings are absolute ratings; exceeding any one of these values may cause permanent damage to the integrated circuit.

2.2 Thermal data

For details, please refer to *Section 4.1: SO-8 thermal data* and *Section 4.2: SO-20 thermal data*.

Table 4. Thermal data(1)

Symbol	Parameter	Value	Unit
$R_{th-jamb}$	Thermal resistance Junction to Ambient: SO-8 SO-20	 130 51	 °C/W °C/W

1. The values quoted are for PCB FR4 area= 58mm x 58mm, PCB thickness = 2mm, Cu thickness = 35µm , Copper areas: SO-8= 2 cm^2, SO-20= 6 cm^2.

2.3 Electrical characteristics

Values specified in this section are for V_s =5.6V to 31V, T_j= -40°C to +150°C unless otherwise stated.

Table 5. General

Pin	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Vo	V_{o_ref}	Output voltage	Vs = 6 to 31V Io = 1 to 150mA	4.9	5.0	5.1	V
Vo	I_{short}	Short circuit current	Vs = 13.5V(1)	150	280	400	mA
Vo	I_{lim}(2)	Output current limitation	Vs = 13.5V(1)	150	320	500	mA
Vs, Vo	V_{line}	Line regulation voltage	Vs = 6 to 31V Io = 1 to 150mA			25	mV
Vo	V_{load}	Load regulation voltage	Io = 1 to 150mA			25	mV
Vs, Vo	V_{dp}(3)	Drop voltage	Io = 150mA		200	400	mV
Vs, Vo	SVR	Ripple rejection	fr = 100 Hz (4)	55			dB
Vs, Vo	I_{qn_150}	Quiescent current	Vs=13.5V, Io=150mA, WEn = high		1.25	2	mA
Vs, Vo	I_{qn_50}	Quiescent current	Vs=13.5V, Io= 50mA, WEn = high		470	1000	µA
Vs, Vo	I_{qn_1}	Quiescent current	Vs=13.5V, Io< 1mA, WEn = high		100	180	µA
Vs, Vo	I_{qs}	Quiescent current with watchdog regulator disabled	Vs=13.5V, Io< 1mA, WEn = low		79	125	µA
	Tw	Thermal protection temperature		150		190	°C
	Tw_hy	Thermal protection temperature hysteresis			10		°C

1. See *Figure 25*.
2. Measured output current when the output voltage has dropped 100mV from its nominal value obtained at Vs=13.5V and Io= 75mA.
3. Vs-Vo measured when the output voltage has dropped 100mV from its nominal value obtained at Vs=13.5V and Io= 75mA.
4. Guaranteed by design.

Table 6. Reset

Pin	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Res	Vres_l	Reset output low voltage	R_{ext} = 5kΩ to Vo, Vo > 1V			0.4	V
Res	I_{Res_h}	Reset output high leakage current	V_{Res} = 5V			1	µA
Res	R_p_u	Pull up internal resistance	With respect to Vo	12	25	50	kΩ
Res	Vo_th	Vo out of regulation threshold	Vs = 6 to 31V, Io = 1 to 150mA	6%	8%	10%	Below V_{o_ref}
Vcr	Vrlth	Reset delay circuit low threshold	Vs = 13.5V	10%	13%	16%	V_{o_ref}
Vcr	Vrhth	Reset delay circuit high threshold	Vs =13.5V	44%	47%	50%	V_{o_ref}
Vcr	Icr	Charge current	Vs = 13.5V	8	17.6	30	µA
Vcr	Idr	Discharge current	Vs = 13.5V	8	17.6	30	µA
Res	Trr_2	Reset reaction time(1)	Vo = V_{o_th} -100mV	100	275	1000	µs
Res	Trd	Reset delay time	Vs = 13.5V, Ctr = 1nF	65		150	ms

1. When Vo becomes lower than 4V, the reset reaction time decreases down to 2µs assuring a faster reset condition in this particular case.

Table 7. Watchdog

Pin	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Wi	Vih	Input high voltage	Vs = 13.5V	3.5			V
Wi	Vil	Input low voltage	Vs = 13.5V			1.5	V
Wi	Vih_hyst	Input hysteresis	Vs = 13.5V		500		mV
Wi	Ii	Pull down current	Vs = 13.5V		10	20	µA
Vcw	Vwhth	High threshold	Vs = 13.5V	44%	47%	50%	V_{o_ref}
Vcw	Vwlth	Low threshold	Vs = 13.5V	10%	13%	16%	V_{o_ref}
Vcw	Icwc	Charge current	Vs = 13.5V, Vcw = 0.1V	4	8	14	µA

Table 7. Watchdog (continued)

Pin	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Vcw	Icwd	Discharge current	Vs = 13.5V, Vcw = 2.5V	1.0	2.13	4.5	µA
Vcw	Twop	Watchdog period	Vs = 13.5V, Ctw = 47nF	25	50	90	ms
Res	twol	Watchdog output low time	Vs = 13.5V, Ctw = 47nF	6	10.5	22	ms

Table 8. Watchdog Enable

Pin	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
WEn	W_{En_low}	Enable input low voltage				1	V
WEn	W_{En_high}	Enable input high voltage		3			V
WEn	W_{En_hyst}	Enable input hysteresis		500	800	1100	mV
WEn	I_{leak}	Pull down current	WEn = 5V	2	8	20	µA

2.4 Electrical characteristics curves

Figure 3. Output voltage vs. Tj

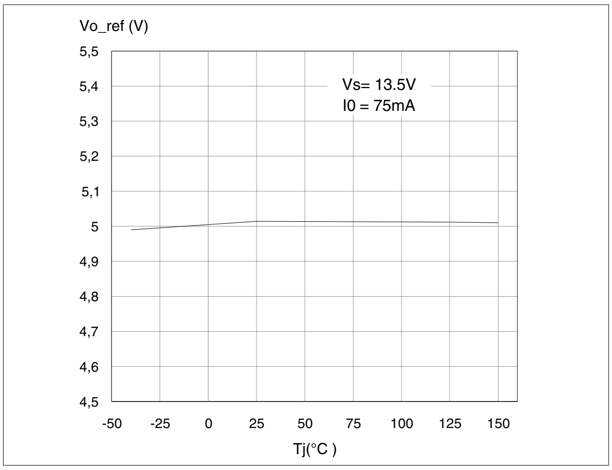


Figure 4. Output voltage vs. Vs

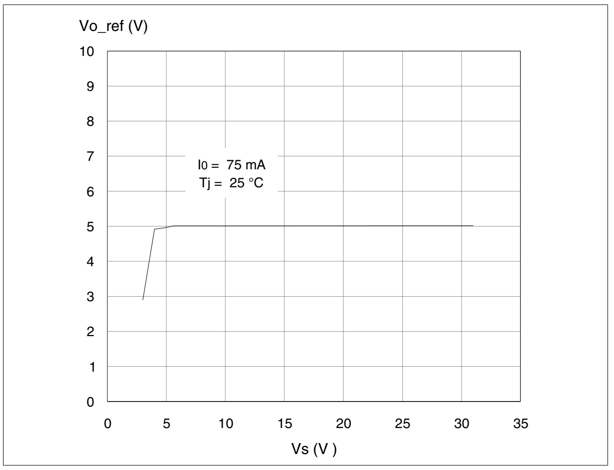


Figure 5. Drop Voltage vs. Output Current

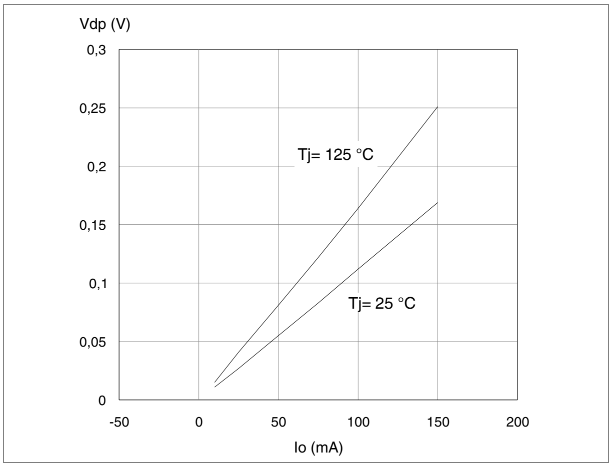


Figure 6. Current consumption vs. Output Current

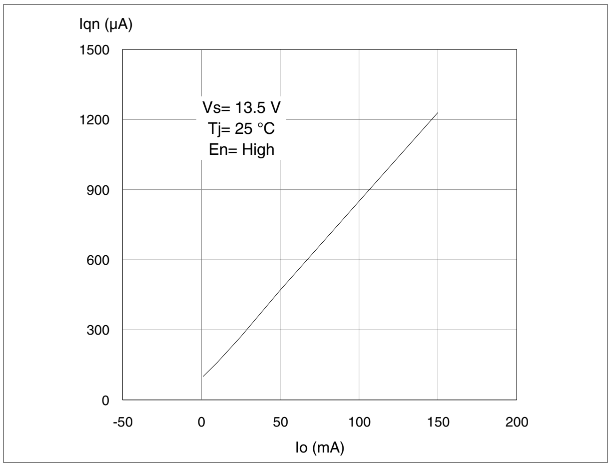


Figure 7. Current consumption vs. Input Voltage

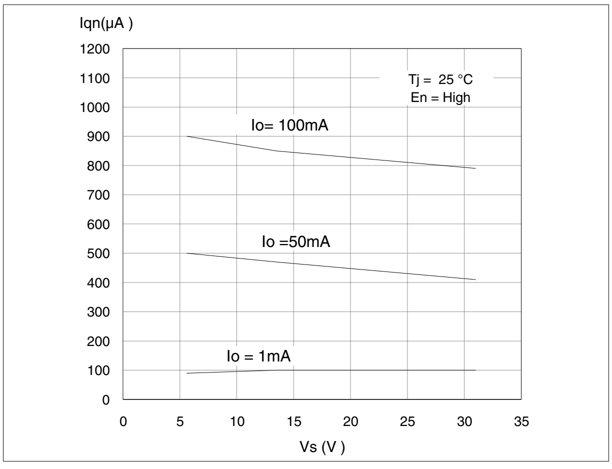


Figure 8. Current limitation vs. Tj

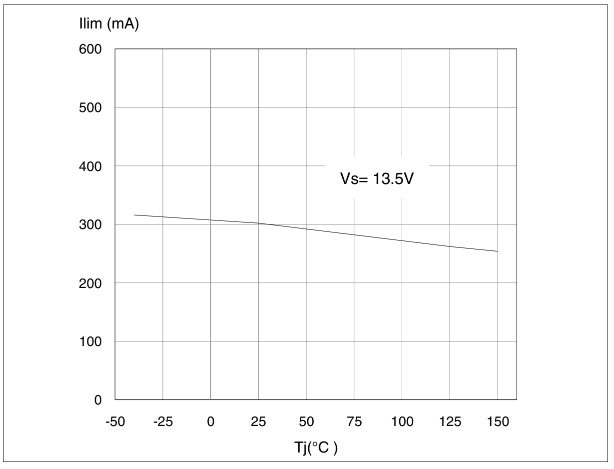


Figure 9. Current limitation vs. Input Voltage

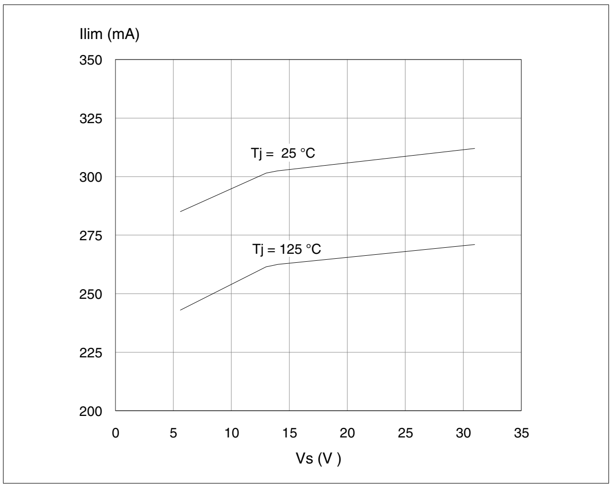


Figure 10. Short Circuit Current vs. Tj

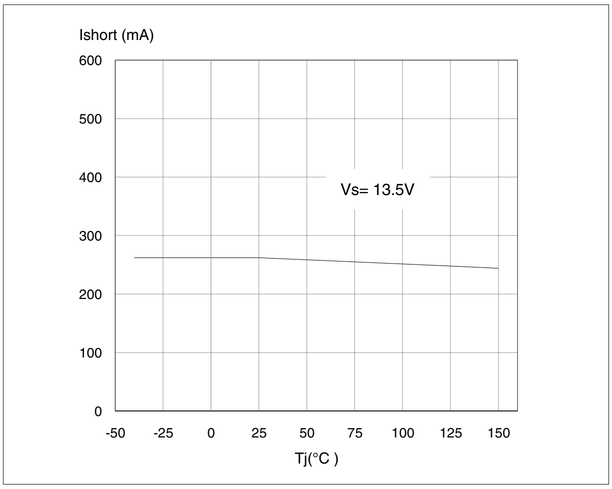


Figure 11. Short Circuit Current vs. Input Voltage

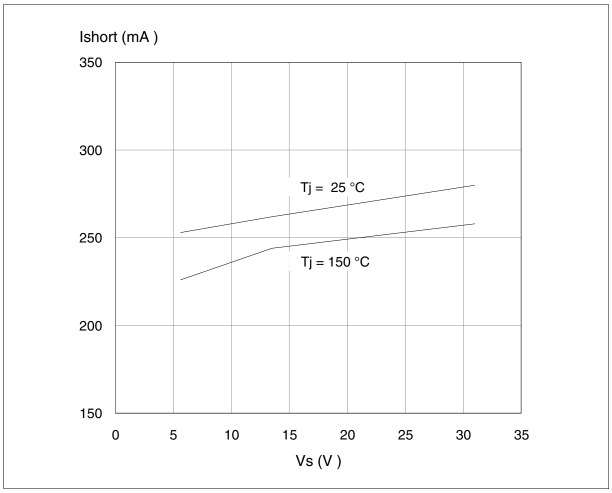


Figure 12. V_{WEn_high} vs. Tj

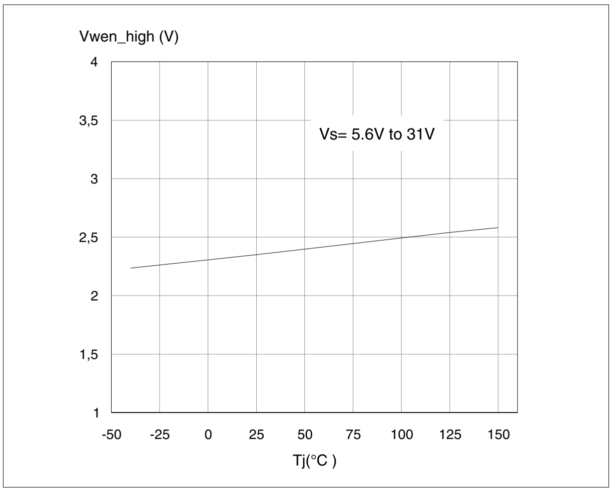


Figure 13. V_{WEN_LOW} vs. Tj

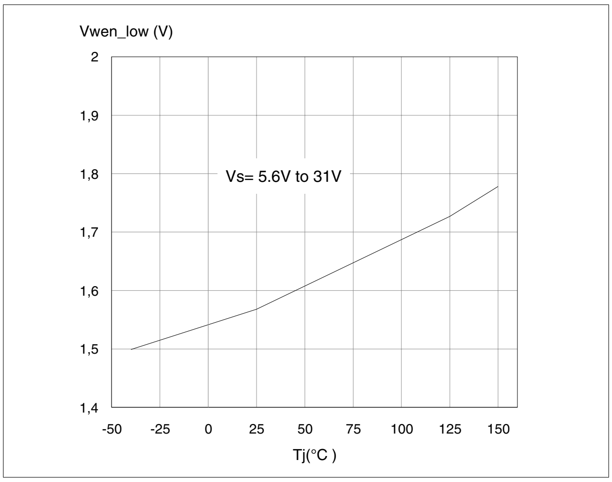


Figure 14. Vrhth vs. Tj

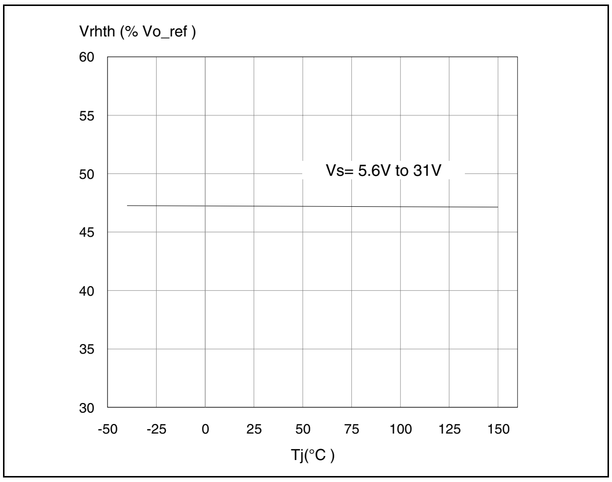


Figure 15. Vrlth vs. Tj

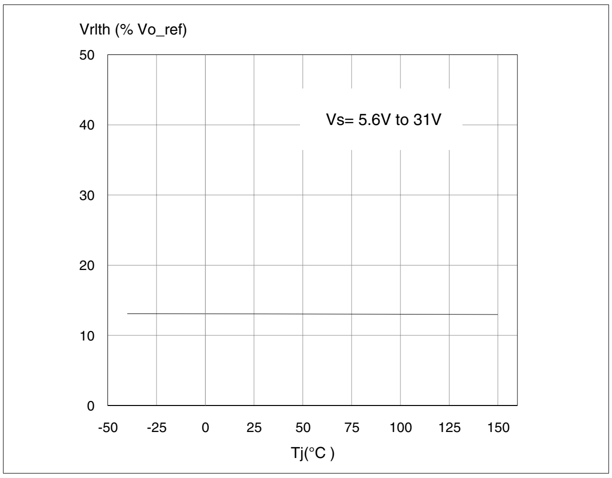


Figure 16. Vwhth vs. Tj

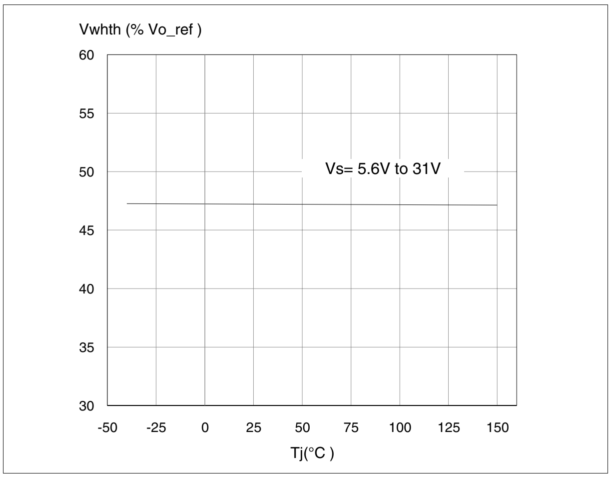


Figure 17. Vwlth vs. Tj

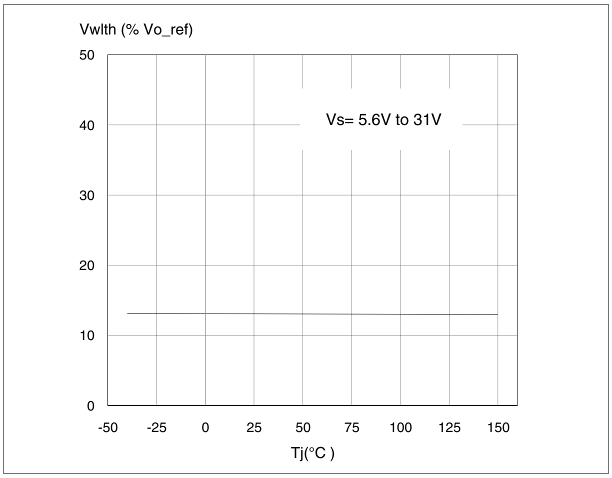


Figure 18. Icr & Icwc vs. Tj

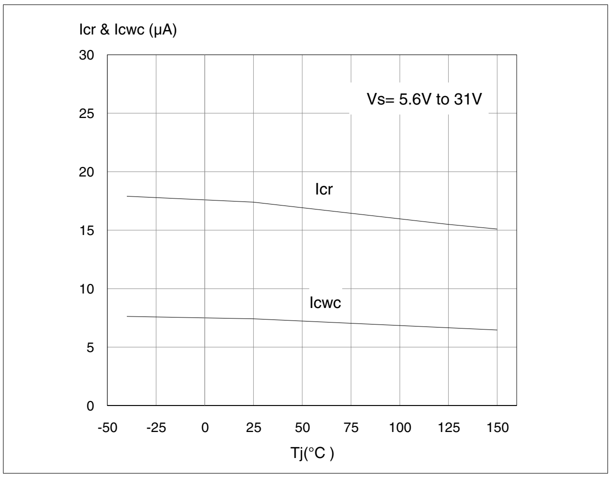


Figure 19. Idr & Icwd vs. Tj

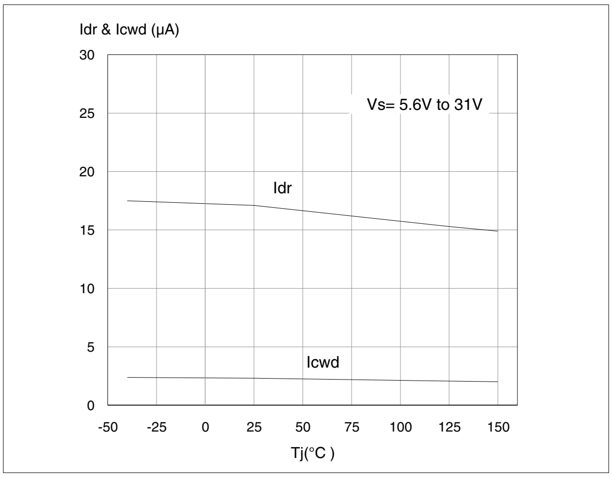


Figure 20. Twop vs. Tj

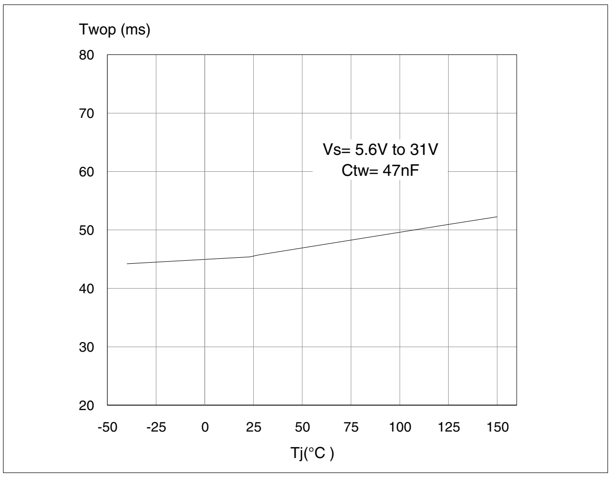
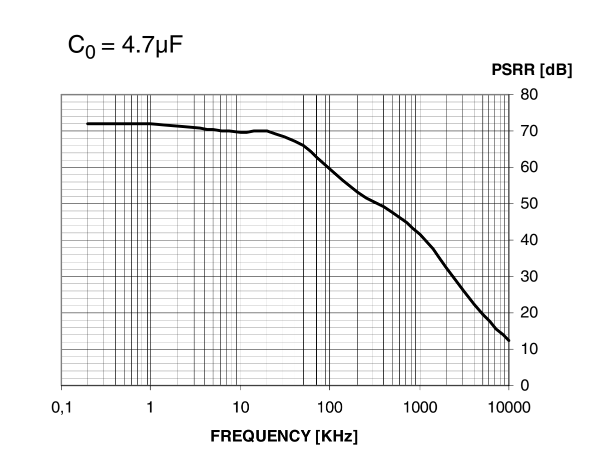


Figure 21. PSRR



2.5 Test circuit and waveforms plot

2.5.1 Load regulation

Figure 22. Load regulation test circuit

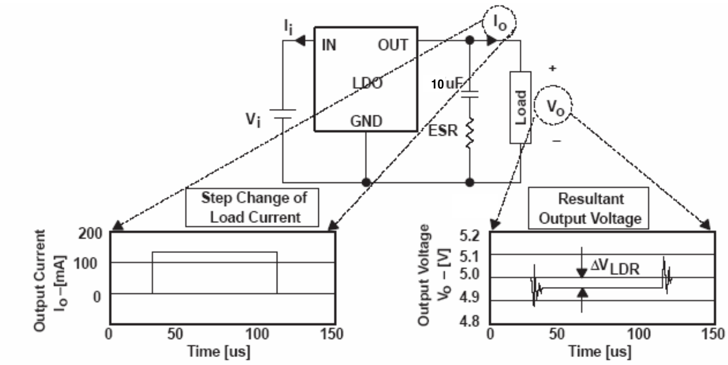
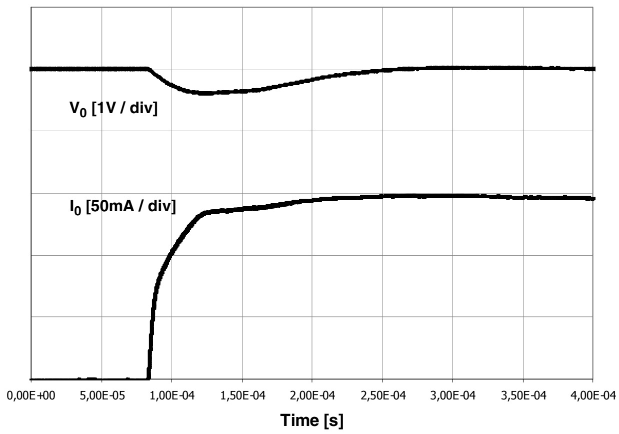
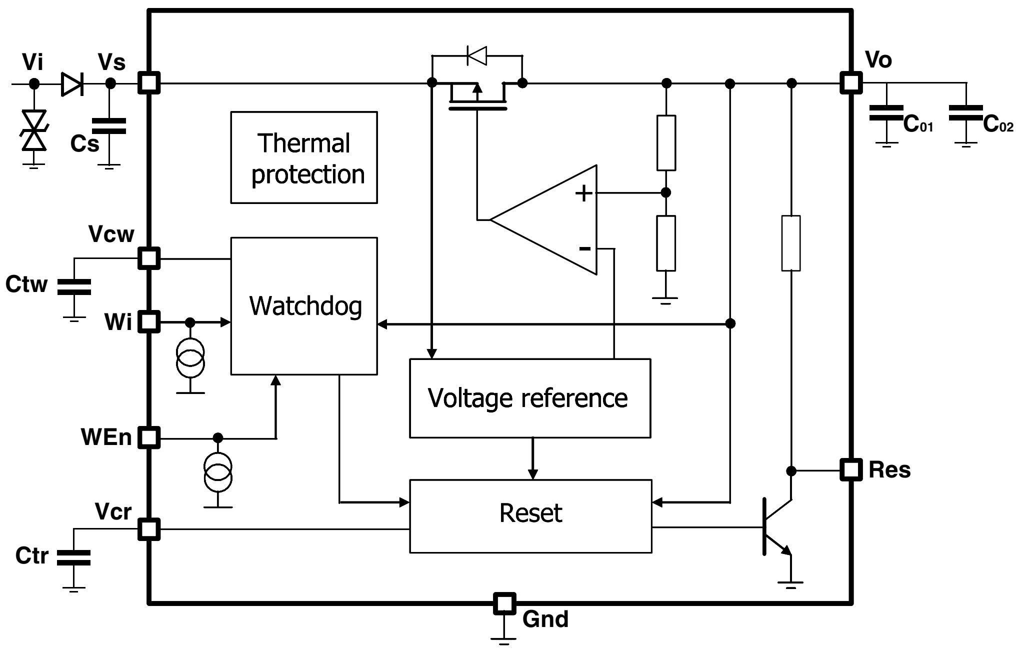


Figure 23. Maximum load variation response



3 Application information

Figure 24. L4993 application schematic

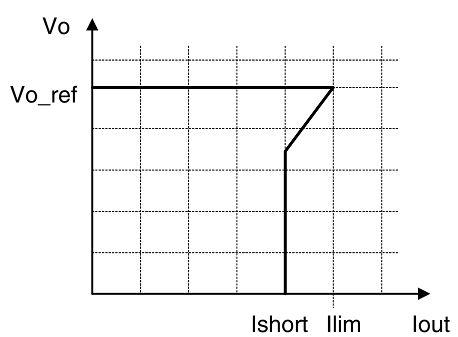


Note: The input capacitor Cs > 200nF is necessary for the smoothing of line disturbances. The output capacitor C01 > 100nF is necessary for the stability of the regulation loop. In order to damp output voltage oscillations during high load current surges, it is recommended put an additional electrolytic capacitor C02 > 10µF at the output pin.

3.1 Voltage regulator

Voltage regulator uses a p-channel transistor as a regulating element. With this structure, very low dropout voltage at current up to 500mA is obtained. The output voltage is regulated up to transient input supply voltage of 40V. No functional interruption due to over-voltage pulses is generated. A short circuit protection to GND is provided. The voltage regulator watchdog functionality can be disabled by putting WEn low.

Figure 25. Behavior of output current versus regulated voltage Vo



3.2 Reset

The reset circuit supervises the output voltage Vo. The Vo_th reset threshold is defined with the in-ternal reference voltage and a resistor output divider. If the output voltage becomes lower than Vo_th then Res goes low with a reaction time trr. The reset low signal is guaranteed for an output voltage Vo greater than 1V.

When the output voltage becomes higher than Vo_th then Res goes high with a delay trd. This delay is obtained by an internal oscillator.

The oscillator period is given by:

Tosc = [(Vrhth-Vrlth) x Ctr] / Icr + [(Vrhth-Vrlth) x Ctr] / Idr

where:

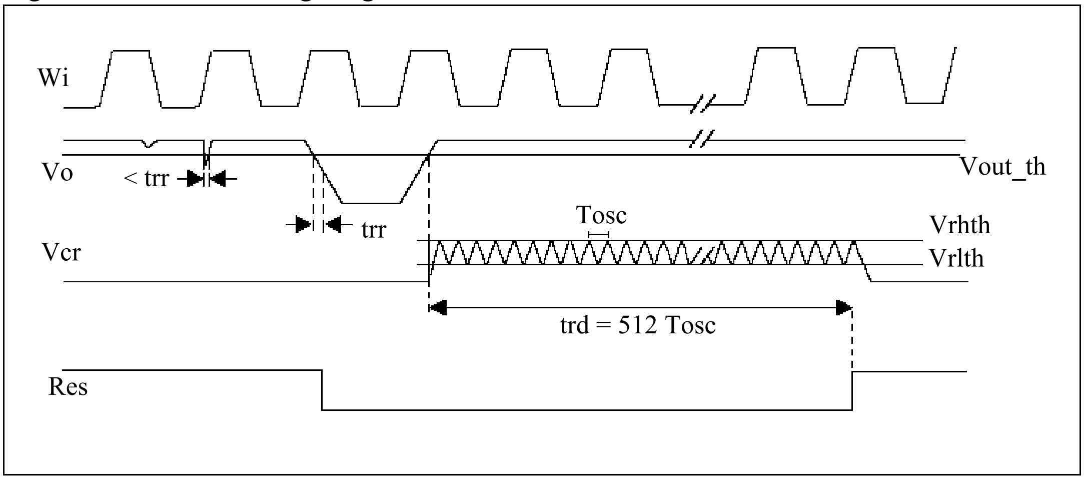
Icr:	is an internally generated charge current
Idr:	is an internally generated discharge current
Vrhth, Vrlth:	are two voltages defined with the output voltage and a resistor output divider
Ctr:	is an external capacitance.

trd is given by:

trd = 512 x Tosc

Reset is active when En is high.

Figure 26. Reset timing diagram



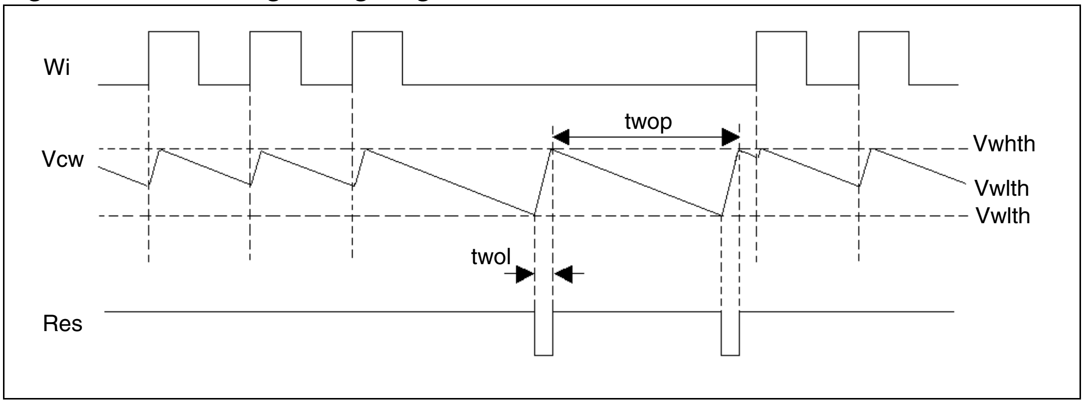
3.3 Watchdog

A connected microcontroller is monitored by the watchdog input Wi. If pulses are missing, the Reset output pin is set to low. The pulse sequence time can be set within a wide range with the external capacitor, Ctw. The watchdog circuit discharges the capacitor Ctw, with the constant current Icwd. If the lower threshold Vwlth is reached, a watchdog reset is generated. To prevent this the microcontroller must generate a positive edge during the discharge of the capacitor before the voltage has reached the threshold Vwlth. In order to calculate the minimum time t, during which the micro-controller must output the positive edge, the following equation can be used:

$$(Vwhth-Vwlth) \times Ctw = Icwd \times t$$

Every Wi positive edge switches the current source from discharging to charging. The same happens when the lower threshold is reached. When the voltage reaches the upper threshold, Vwhth, the current switches from charging to discharging. The result is a saw-tooth voltage at the watchdog timer capacitor Ctw.

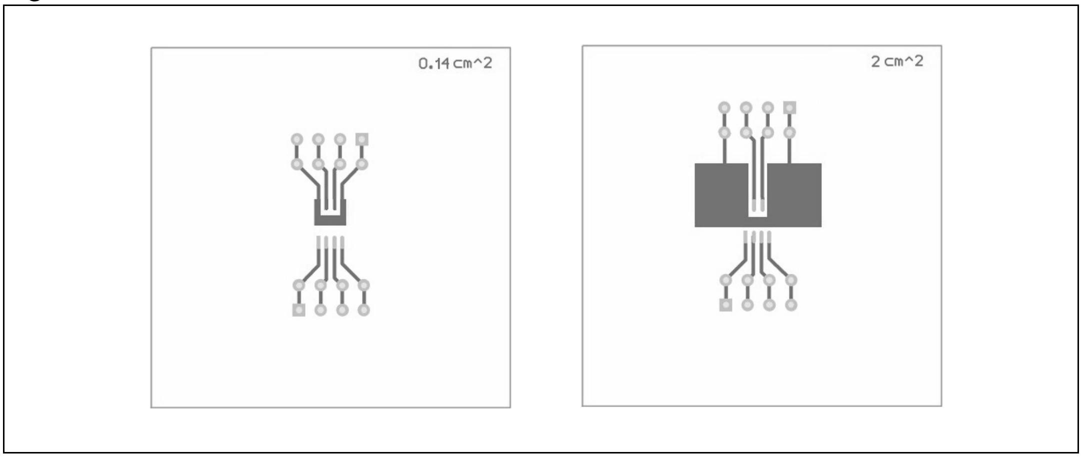
Figure 27. Watchdog timing diagram



4 Package and PCB thermal data

4.1 SO-8 thermal data

Figure 28. SO-8 PC board



Note: Layout condition of R_{th} and Z_{th} measurements (PCB FR4 area= 58mm x 58mm, PCB thickness = 2mm, Cu thickness = 35µm , Copper areas: from minimum pad lay-out to 2cm^2).

Figure 29. $R_{thj\text{-}amb}$ Vs. PCB copper area in open box free air condition

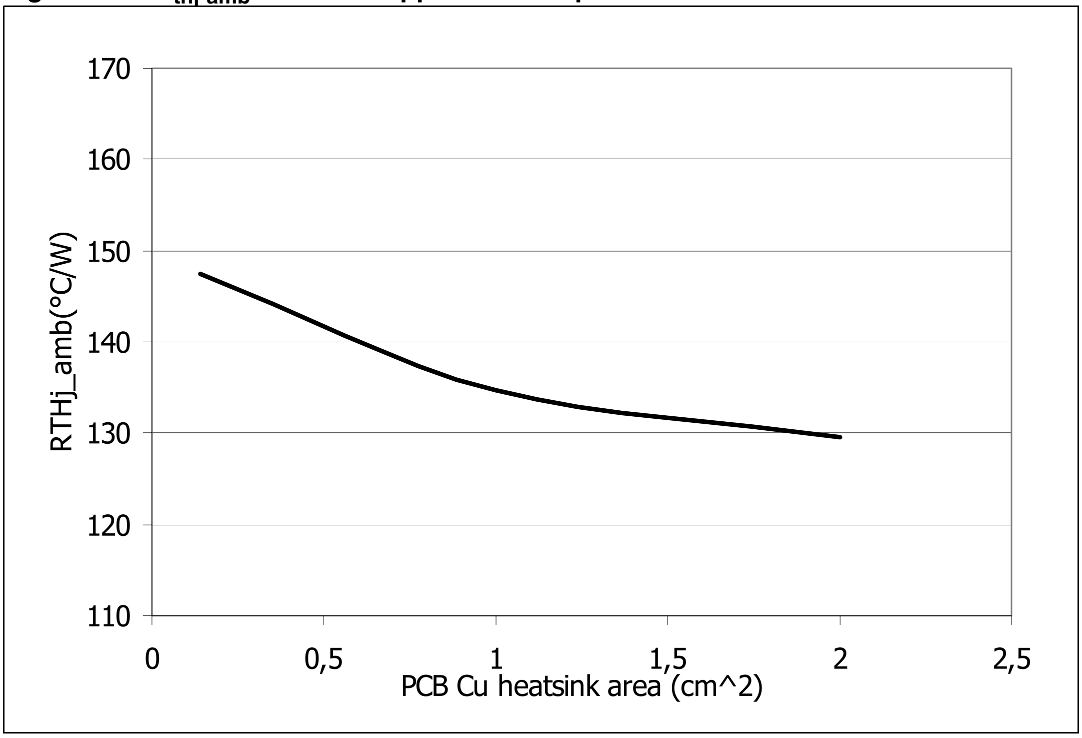
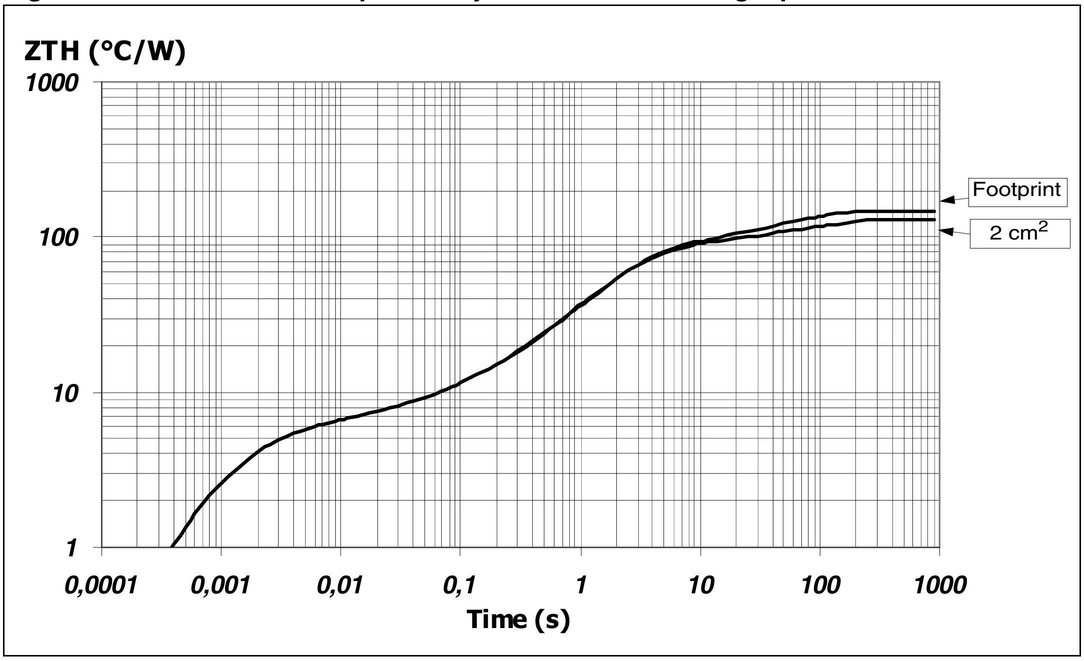


Figure 30. SO-8 thermal impedance junction ambient single pulse



Equation 1: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_P/T$

Figure 31. Thermal fitting model of Vreg in SO-8

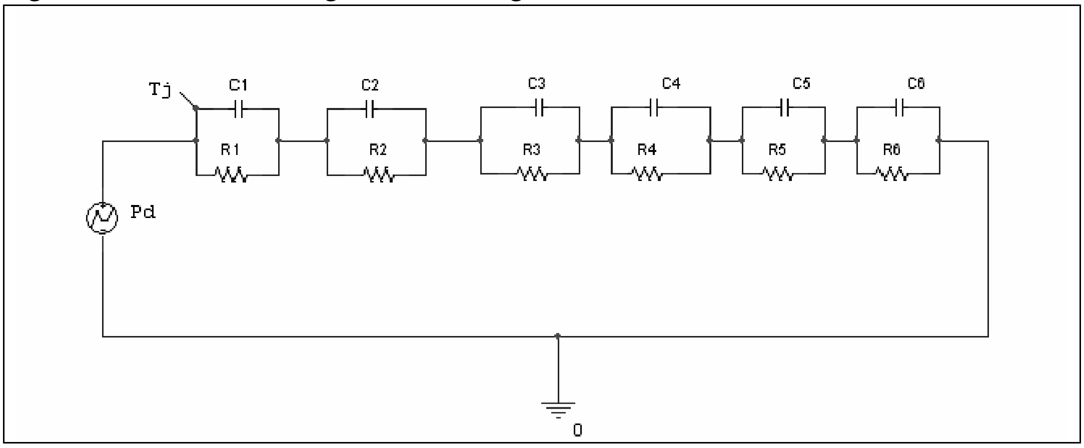
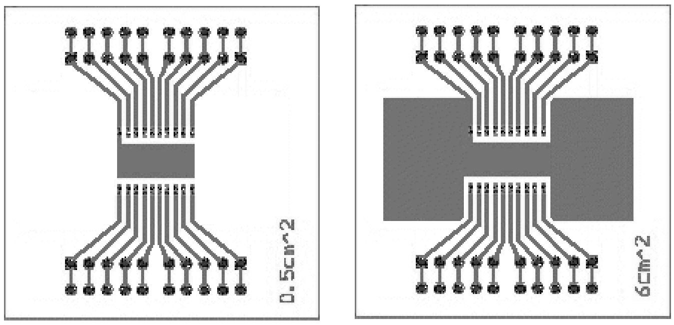


Table 9. SO-8 thermal parameter

Area/island (cm^2)	Footprint	2
R1 (°C/W)	4.21	
R2 (°C/W)	2.11	
R3 (°C/W)	2	
R4 (°C/W)	41	
R5 (°C/W)	40	
R6 (°C/W)	58	40
C1 (W.s/°C)	0.00029	
C2 (W.s/°C)	0.0024	
C3 (W.s/°C)	0.03	
C4 (W.s/°C)	0.04	
C5 (W.s/°C)	0.1	
C6 (W.s/°C)	1.05	2

4.2 SO-20 thermal data

Figure 32. SO-20 PC board



Note: *Layout condition of R_{th} and Z_{th} measurements (PCB FR4 area= 58mm x 58mm,PCB thickness = 2mm, Cu thickness=35µm , Copper areas: from minimum pad lay-out to 6cm^2).*

Figure 33. $R_{thj-amb}$ Vs. PCB copper area in open box free air condition

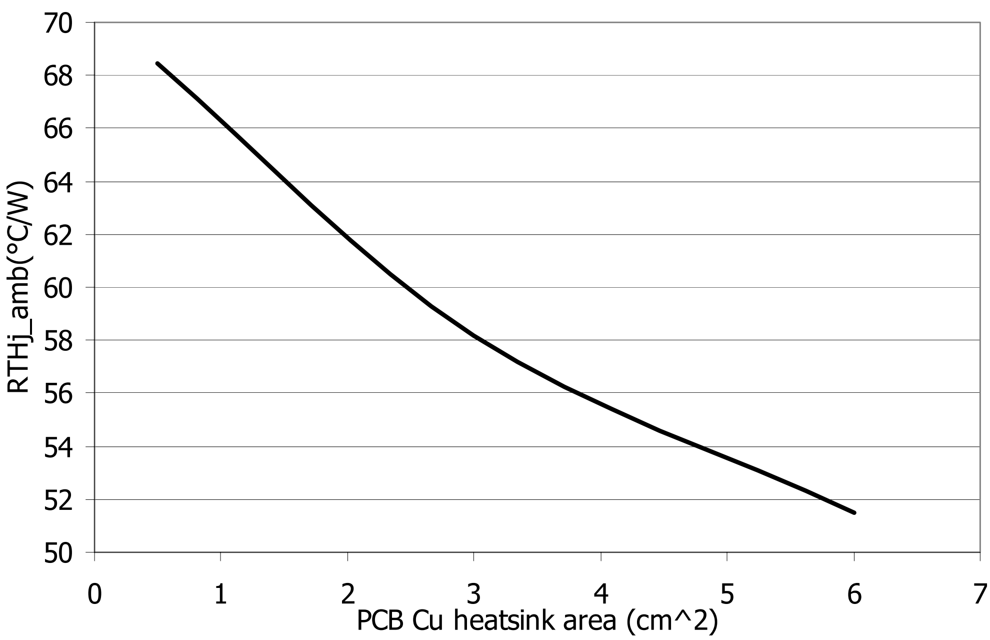
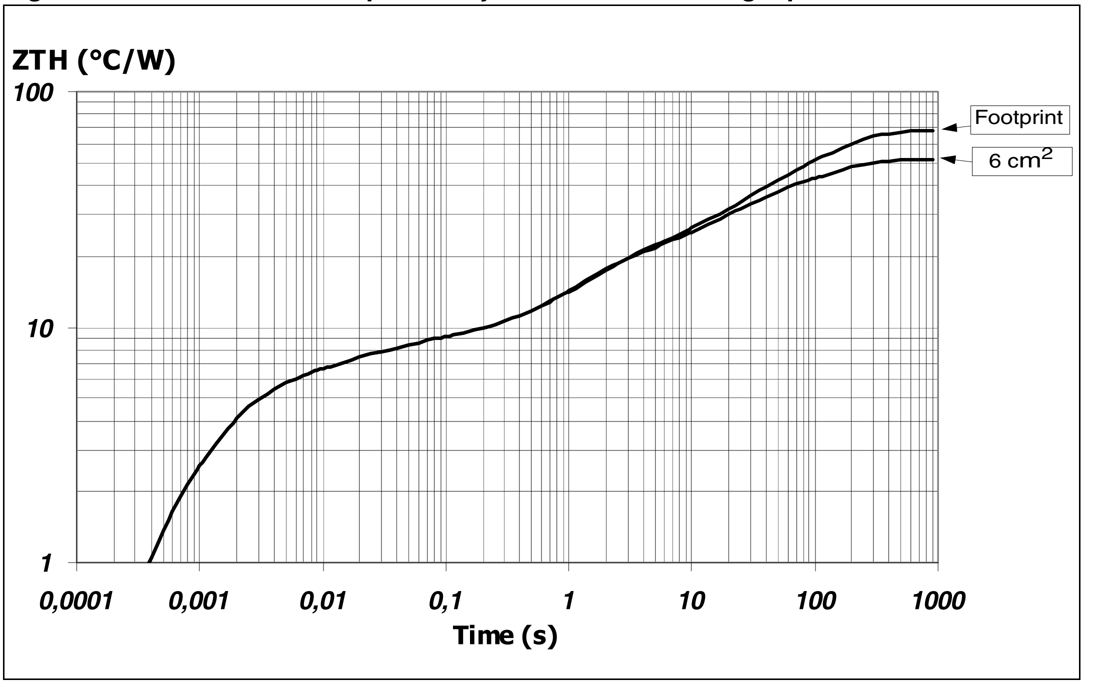


Figure 34. SO-20 thermal impedance junction ambient single pulse



Equation 2: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_P/T$

Figure 35. Thermal fitting model of Vreg in SO-20

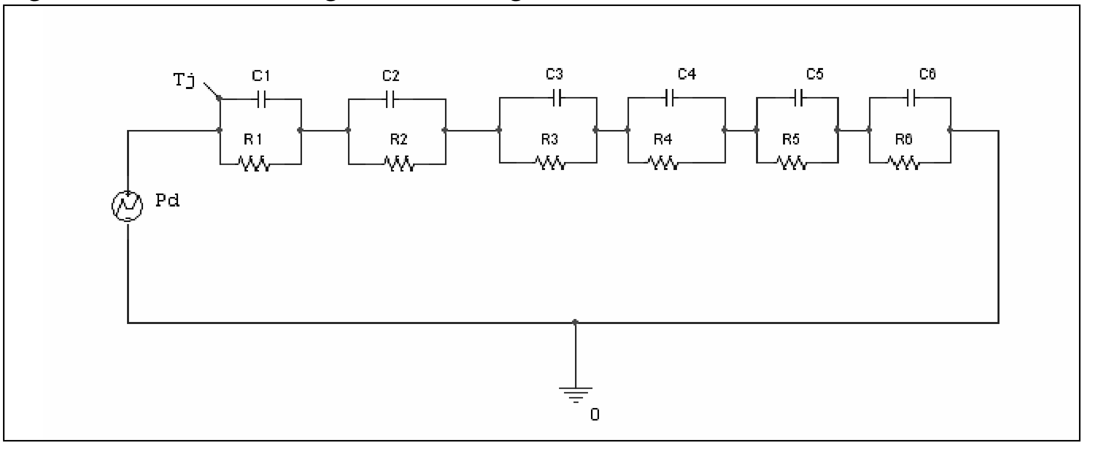


Table 10. SO-20 thermal parameter

Area/island (cm^2)	Footprint	2
R1 (°C/W)	4.21	
R2 (°C/W)	2.11	
R3 (°C/W)	2.2	
R4 (°C/W)	10	
R5 (°C/W)	15	
R6 (°C/W)	35	18
C1 (W.s/°C)	0.00029	
C2 (W.s/°C)	0.0024	
C3 (W.s/°C)	0.015	
C4 (W.s/°C)	0.15	
C5 (W.s/°C)	1.5	
C6 (W.s/°C)	4	7

5 Package and packing information

5.1 ECOPACK® packages

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second-level interconnect. The category of Second-Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label.

ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

5.2 SO-8 package information

Figure 36. SO-8 package dimensions

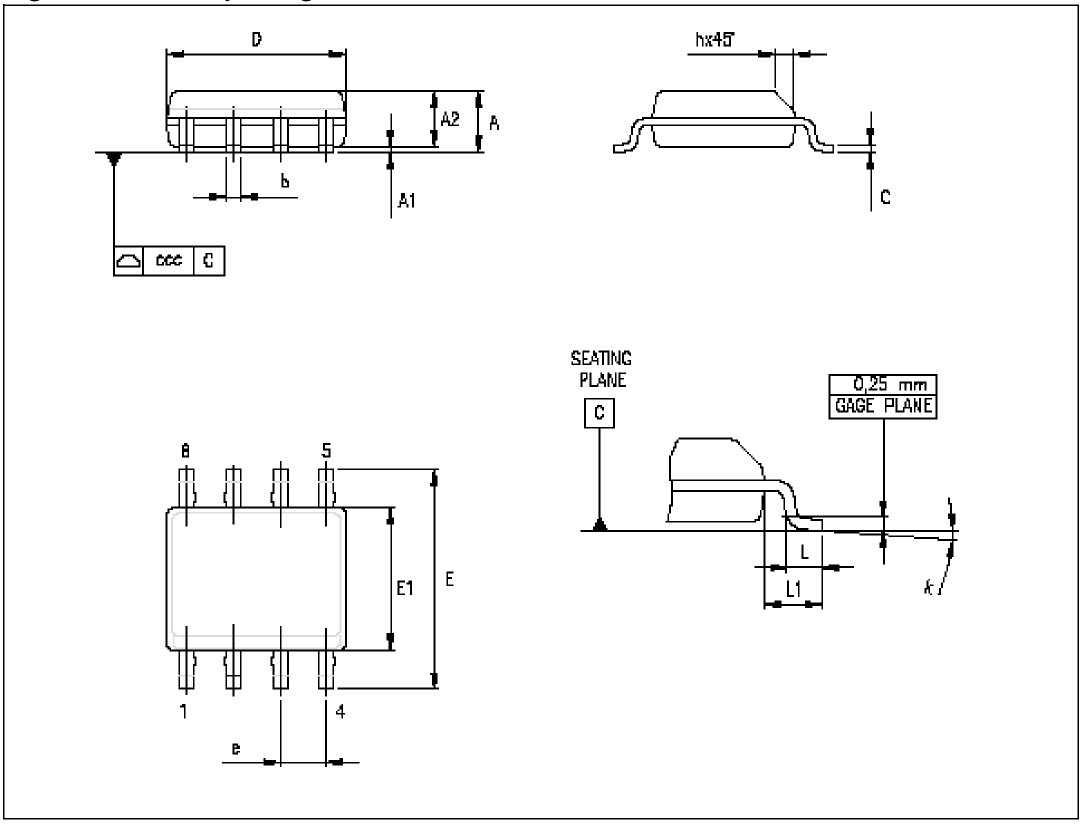


Table 11. SO-8 mechanical data

Symbol	Millimeters		
	Min.	Typ.	Max.
A			1.75
A1	0.10		0.25
A2	1.25		
b	0.28		0.48
c	0.17		0.23
D(1)	4.80	4.90	5.00
E	5.80	6.00	6.20
E1(2)	3.80	3.90	4.00
e		1.27	
h	0.25		0.50
L	0.40		1.27
L1		1.04	
k	0°		8°
ccc			0.10

1. Dimensions D does not include mold flash, protrusions or gate burrs. Mold flash, potrusions or gate burrs shall not exceed 0.15mm in total (both side).
2. Dimension “E1” does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25mm per side.

5.3 SO-20 package information

Figure 37. SO-20 package dimensions

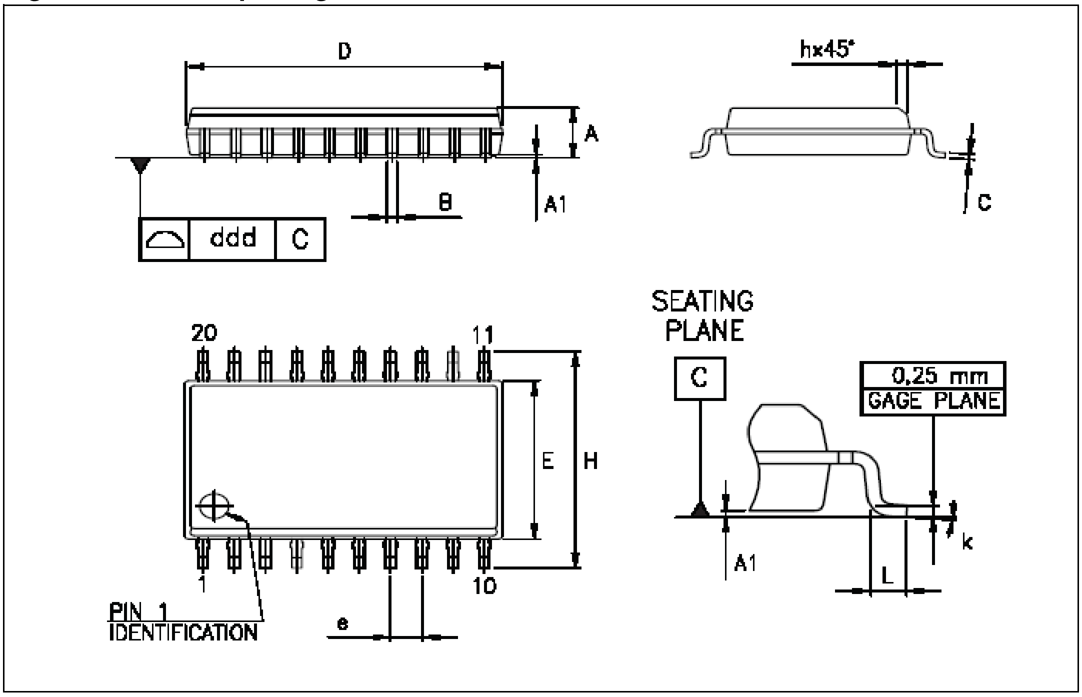


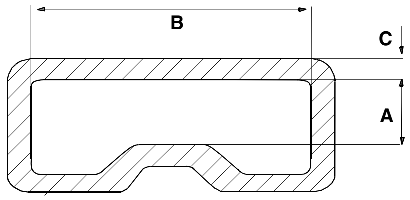
Table 12. SO-20 mechanical data

Symbol	Millimeters		
	Min.	Typ.	Max.
A	2.35		2.65
A1	0.10		0.30
B	0.33		0.51
C	0.23		0.32
D(1)	12.60		13.00
E	7.40		7.60
e		1.27	
H	10.0		10.65
h	0.25		0.75
L	0.40		1.27
k	0°		8°
ddd			0.10

1. “D” dimension does not include mold flash, protusions or gate burrs. Mold flash, protusions or gate burrs shall not exceed 0.15mm per side.

5.4 SO-8 packing information

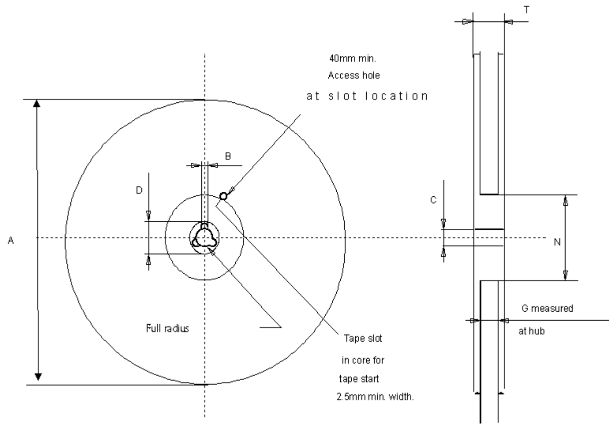
Figure 38. SO-8 tube shipment (no suffix)



Base Q.ty	100
Bulk Q.ty	2000
Tube length (± 0.5)	532
A	3.2
B	6
C (± 0.1)	0.6

All dimensions are in mm.

Figure 39. SO-8 tape and reel shipment (suffix “TR”)



REEL DIMENSIONS

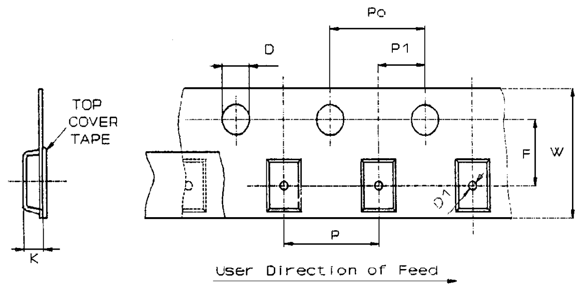
Base Q.ty	2500
Bulk Q.ty	2500
A (max)	330
B (min)	1.5
C (± 0.2)	13
F	20.2
G (+ 2 / -0)	12.4
N (min)	60
T (max)	18.4

All dimensions are in mm.

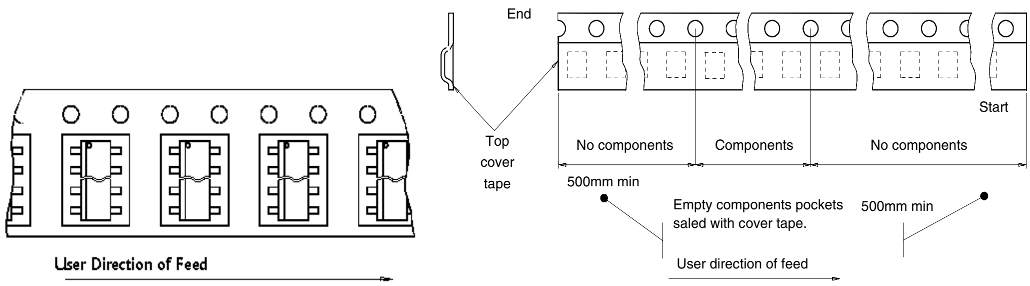
TAPE DIMENSIONS

According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb. 1986

Tape width	**W**	12
Tape Hole Spacing	**P0 (± 0.1)**	4
Component Spacing	**P**	8
Hole Diameter	**D (+ 0.1/-0)**	1.5
Hole Diameter	**D1 (min)**	1.5
Hole Position	**F (± 0.05)**	5.5
Compartment Depth	**K (max)**	4.5
Hole Spacing	**P1 (± 0.1)**	2

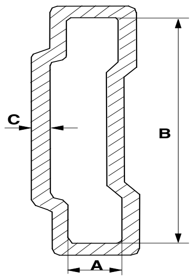


All dimensions are in mm.



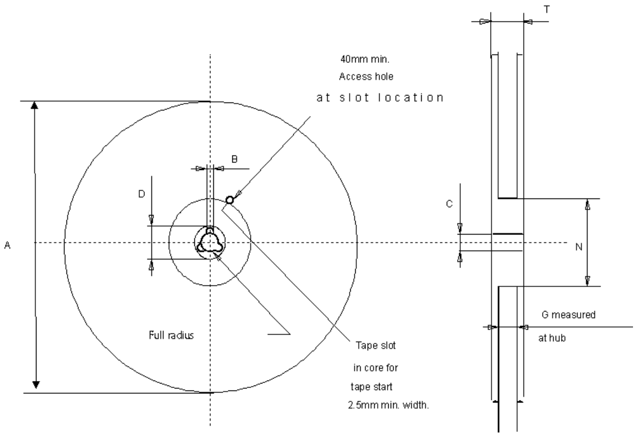
5.5 SO-20 packing information

Figure 40. SO-20 tube shipment (no suffix)



Base Q.ty	40
Bulk Q.ty	800
Tube length (± 0.5)	532
A	3.5
B	13.8
C (± 0.1)	0.6

Figure 41. SO-20 tape and reel shipment (suffix "TR")



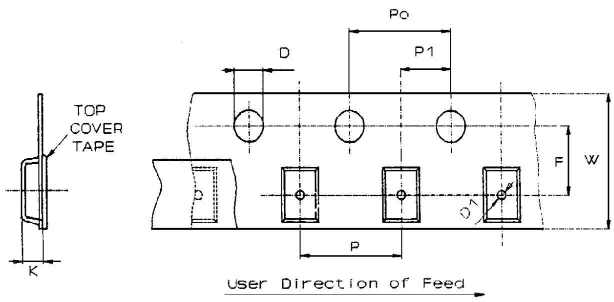
Reel dimensions

Base Q.ty	1000
Bulk Q.ty	1000
A (max)	330
B (min)	1.5
C (± 0.2)	13
D	20.2
G (+ 2 / -0)	24.4
N (min)	60
T (max)	30.4

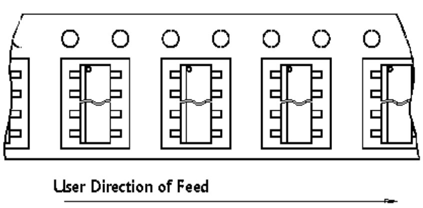
Tape dimensions

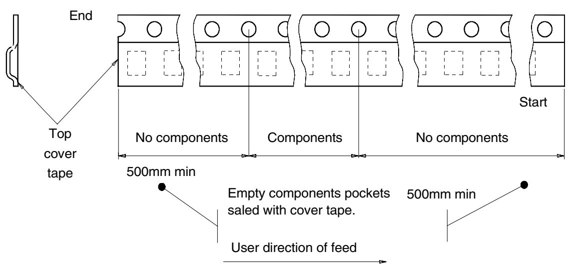
According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb. 1986

Tape width	**W**	24
Tape Hole Spacing	**P0 (± 0.1)**	4
Component Spacing	**P**	12
Hole Diameter	**D (+ 0.1/-0)**	1.5
Hole Diameter	**D1 (min)**	1.5
Hole Position	**F (± 0.05)**	11.5
Compartment Depth	**K (max)**	6.5
Hole Spacing	**P1 (± 0.1)**	2



All dimensions are in mm.





6 Revision history

Table 13. Document revision history

Date	Revision	Changes
June-2004	1	Initial release.
18-Jan-2007	2	Updated Table 5., 6, 7 and 8.
01-Jun-2007	3	Document put in corporate technical literature template. Updated Table 4.
22-Aug-2007	4	Table 5: General: updated I_{short}, I_{lim}, I_q, T_{rr2}, V_{ih_hist} parameters.
29-Aug-2007	5	Added list of tables and figures. Added Section 4: Package and PCB thermal data.
08-Apr-2008	6	Document restructured. Changed Figure 1: Block diagram. Updated Table 5: General: – changed I_{short} max value from 4000 mA to 400 mA – changed I_{qn_150} typ. value from 1.45 mA to 1.25 mA – changed I_{qn_50} typ. value from 538 µA to 470 µA – changed I_{qn_1} typ. value from 120 µA to 100 µA. Updated Table 6: Reset: – corrected trd formula. Updated Table 7: Watchdog: – changed Vwlth values in V_{o_ref} percentages – changed Vwhth values in V_{o_ref} percentages. Added Figure 24: L4993 application schematic. Added Section 2.4: Electrical characteristics curves. Added Section 2.5: Test circuit and waveforms plot.

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