

FEATURES

Integrates all typical controller functions

- Digital control loop**
- Remote and local voltage sense**
- Primary and secondary side current sense**
- PWM control**
- Synchronous rectifier control**
- Hot-swap sense and control**
- Current sharing**
- Integrated programmable loop filter**

I²C interface

Extensive fault detection and protection

Extensive programming

Fast calibration

8 Kb EEPROM

Standalone or microcontroller control

APPLICATIONS

AC/DC power supplies

Isolated dc/dc power supplies

Redundant power supplies

Parallel power supplies

Server, storage, network, and communications infrastructure

PRODUCT OVERVIEW

The ADP1043 is a secondary side power supply controller IC that is designed to provide all the functions that are typically needed in an isolated ac/dc or dc/dc control application.

The ADP1043 is optimized for minimal component count, maximum flexibility, and minimum design time. Features include remote voltage sense, local voltage sense, primary and secondary side current sense, PWM generation, and hot-swap sense and control. The control loop is digital, with an integrated programmable digital filter. Protection features include current limiting, ac sense, UVLO, and OVP (overvoltage protection).

The built-in EEPROM provides extensive programming of the integrated loop filter, PWM signal timing, inrush current, soft start timing and sequencing. Reliability is improved through a built-in checksum and redundancy of critical circuits.

A comprehensive GUI is provided for easy design of loop filter characteristics and programming of the safety features. The industry-standard I²C bus gives access to the many monitoring and system test functions.

The ADP1043 is available in a 32-lead LFCSP package and operates from a single 3.3 V supply.

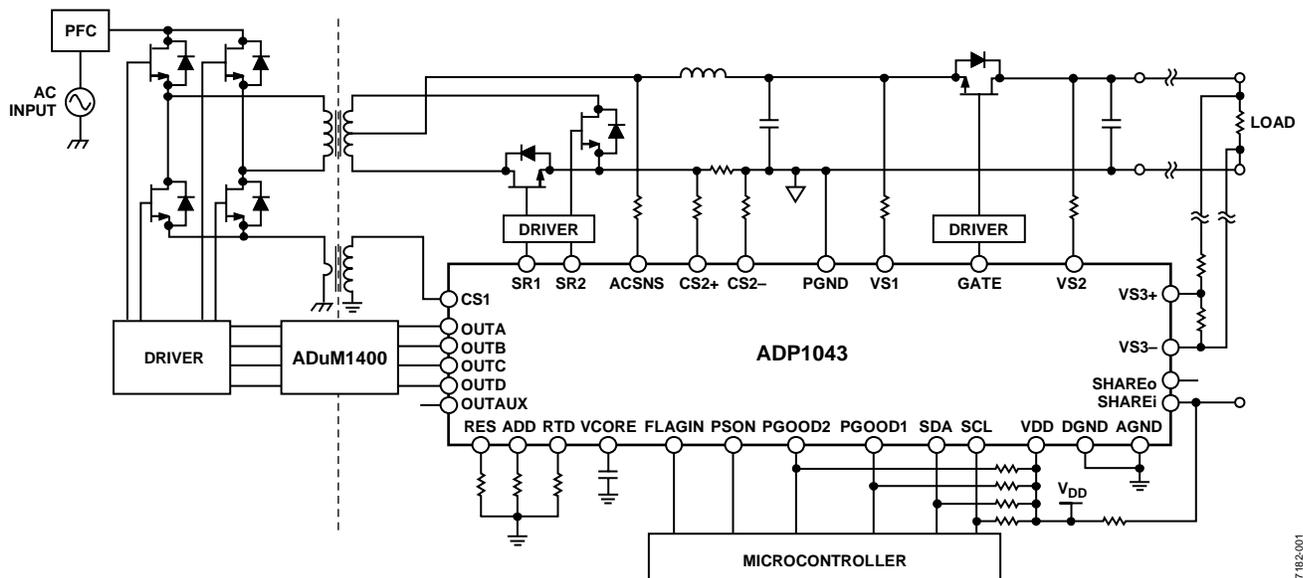


Figure 1. Typical Application Circuit

Rev. PrA

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GENERAL DESCRIPTION

The ADP1043 is a secondary side controller for switch mode power supplies (SMPS). It is designed for use in isolated redundant applications. The ADP1043 integrates the typical functions that are needed to control a power supply. These include

- Output voltage sense and feedback
- Digital loop filter compensation
- PWM generation
- Current sharing
- OrFET control
- Current, voltage, and temperature sense
- Housekeeping and I²C interface
- Calibration and trimming

The main function of controlling the output voltage is performed using the feedback ADCs, the digital loop filter, and the PWM block. The feedback ADCs use a patented multipath approach. There is a combination of a high speed, low resolution (fast and coarse) ADC and a low speed, high resolution (slow and accurate) ADC. Loop compensation is implemented using the digital filter. This PID (proportional, integral, derivative) filter is implemented in the digital domain, allowing easy programming of filter characteristics, which is of great value in customizing and debugging designs. The PWM block generates up to six programmable PWM outputs for control of FET drivers and synchronous rectification FET drivers. This programmability allows many traditional and unique switching topologies to be realized.

A current share bus interface is provided for parallel power supplies. The part also has hot-swap OrFET sense and control for N+1 redundant power supplies.

Conventional power supply housekeeping features, such as remote and local voltage sense and primary and secondary side current sense, are included. An extensive set of protections is offered, including overvoltage protection (OVP), overcurrent protection (OCP), overtemperature protection (OTP), undervoltage protection (UVP), ground continuity monitoring, and ac sensing.

All these features are programmable through the I²C bus interface. This bus interface is also used to calibrate the power supply. Other information, such as input current, output current, and fault flags, is also available through the digital bus interface.

The internal 1024-byte EEPROM makes it possible to store all programmed values and allows standalone control without a microcontroller. Approximately 700 bytes of the EEPROM are available for user information, such as version and manufacturing date.

The ADP1043 comes with a free downloadable GUI, which provides all the necessary software to program the part.

The ADP1043 operates from a single 3.3 V supply and is specified from -40°C to +85°C.

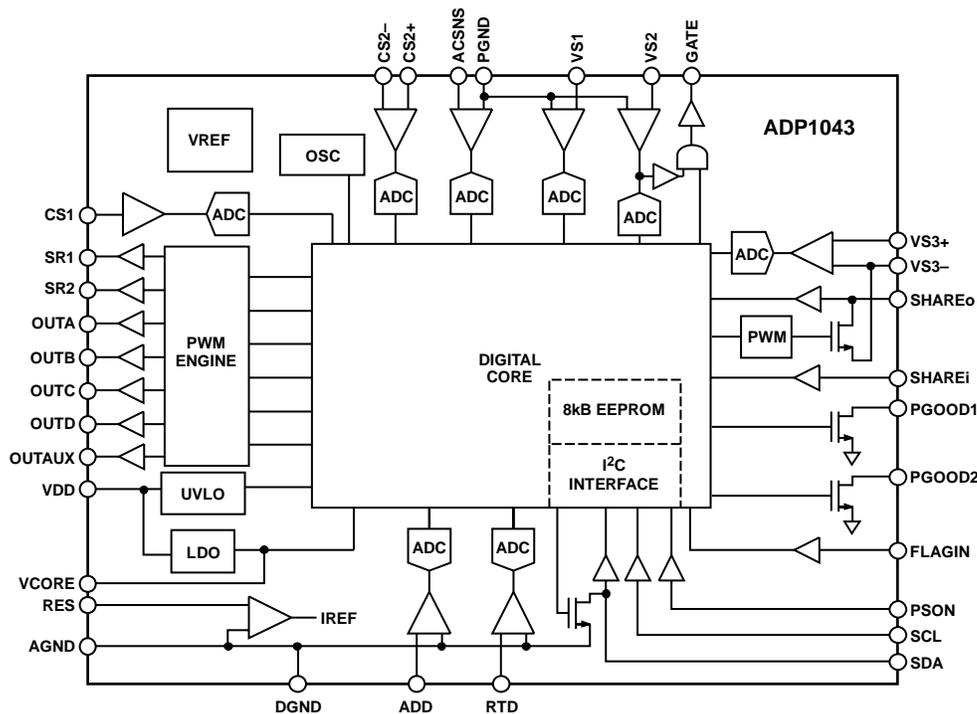


Figure 2. Functional Block Diagram

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PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

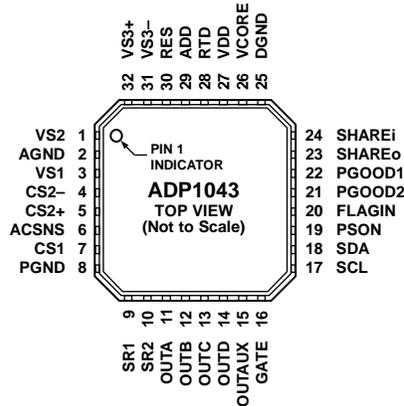


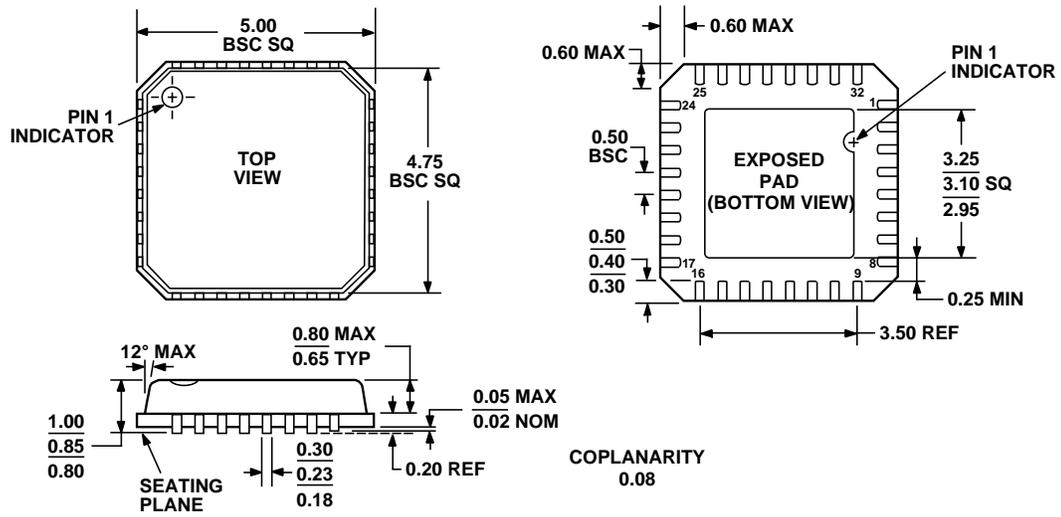
Figure 3. Pin Configuration

Table 1. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	VS2	Power Supply Output Sense Input. This signal is referred to PGND. Input to a low frequency Σ - Δ ADC. Nominal voltage at this pin should be 1 V.
2	AGND	Analog Ground. This pin is the ground for the analog circuitry of the ADP1043. Star connect to DGND.
3	VS1	Local Voltage Sense Input. This signal is referred to PGND. Input to a high frequency Σ - Δ ADC. Nominal voltage at this pin should be 1 V.
4	CS2-	Inverting Differential Current Sense Input. Nominal voltage at this pin should be 1 V for best operation. When using high-side current sense in a 12 V application, a 110 k Ω resistor should be placed between the sense resistor and this pin. When using low-side current sense, a 10 k Ω resistor should be placed between the sense resistor and this pin. When using high-side, use the formula $R = (V_{COMMONMODE} - 1)/100 \mu A$.
5	CS2+	Noninverting Differential Current Sense Input. Nominal voltage at this pin should be 1 V for best operation. When using high-side current sense in a 12 V application, a 110 k Ω resistor should be placed between the sense resistor and this pin. When using low-side current sense, a 10 k Ω resistor should be placed between the sense resistor and this pin. When using high-side, use the formula $R = (V_{COMMONMODE} - 1)/100 \mu A$.
6	ACSNS	AC Sense Input. This input is connected upstream of the main inductor through a resistor divider network. The nominal voltage at this pin should be 1 V. This signal is referred to PGND.
7	CS1	Primary Side Differential Current Sense Input. This is the current transformer input to measure and control the primary side current. This signal is referred to PGND.
8	PGND	Power Ground. This pin is the ground connection for the main power rail of the power supply. Star connect to AGND.
9	SR1	Synchronous Rectifier Output. This PWM output is connected to the input of a FET driver. This pin can be disabled when not in use. This signal is referred to AGND.
10	SR2	Synchronous Rectifier Output. This PWM output is connected to the input of a FET driver. This pin can be disabled when not in use. This signal is referred to AGND.
11	OUTA	PWM Output for Primary Side Switch. This pin can be disabled when not in use. This signal is referred to AGND.
12	OUTB	PWM Output for Primary Side Switch. This pin can be disabled when not in use. This signal is referred to AGND.
13	OUTC	PWM Output for Primary Side Switch. This pin can be disabled when not in use. This signal is referred to AGND.
14	OUTD	PWM Output for Primary Side Switch. This pin can be disabled when not in use. This signal is referred to AGND.
15	OUTAUX	Auxiliary PWM Output. This pin can be disabled when not in use. This signal is referred to AGND.
16	GATE	OrFET Gate Drive Output. This output is open drain. This signal is referred to AGND.

Pin No.	Mnemonic	Description
17	SCL	I ² C Serial Clock Input. This signal is referred to AGND.
18	SDA	I ² C Serial Data Input and Output (Open Drain). This signal is referred to AGND.
19	PSON	Power Supply On Input. This signal is referred to DGND.
20	FLAGIN	Flag Input. An external signal can be input here to generate a flag condition.
21	PGOOD2	Power-Good Output (Open Drain). This signal is referred to AGND. This pin is controlled by the PGOOD2 flag. If any flag is set, this pin toggles.
22	PGOOD1	Power-Good Output (Open Drain). This signal is referred to AGND. This pin is controlled by the PGOOD flag. If any of the following are out of range, this pin toggles: ACSNS, OCP CS1, OCP CS2, VS1 OVP, VS2 OVP, or UVP.
23	SHAREo	Share Bus Output Voltage Pin. When configured as a digital share bus, this pin is a digital output. When configured as an analog share bus, this pin is an open-drain analog output. This signal is referred to VS3–.
24	SHAREi	Analog Share Bus Feedback Pin. This signal is input to an ADC in the ADP1043. This signal is referred to VS3–.
25	DGND	Digital Ground. This pin is the ground for the digital circuitry of the ADP1043. Star connect to AGND.
26	VCORE	Output of 2.5 V Regulator. Connect a 100 nF capacitor from this point to DGND.
27	VDD	Positive Supply Input. Range is from 3 V to 3.6 V. This signal is referred to AGND.
28	RTD	Thermistor Input. A 10 k Ω or 100 k Ω thermistor is placed from this pin to AGND. This signal is referred to AGND.
29	ADD	Address Select Input. Connect a resistor from ADD to GND. This signal is referred to AGND.
30	RES	Resistor Input. This pin sets up the internal voltage reference for the ADP1043. Connect a 50 k Ω resistor ($\pm 1\%$) from RES to GND. This signal is referred to AGND. Decoupling this pin to AGND is recommended for noise immunity.
31	VS3–	Inverting Remote Voltage Sense Input. There should be a low ohmic contact to AGND.
32	VS3+	Noninverting Remote Voltage Sense Input. This signal is referred to VS3–.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-VHHD-2

Figure 4. Mechanical Package Dimensions

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