Revision: 1.1.0

PROCESS CHANGE NOTIFICATION
PCN0805

WAFER FABRICATION SITE CHANGE FOR SERIAL CONFIGURATION DEVICES

Change Description

This is an update to PCN0805; please see the revision history table for information specific to this update.

Serial Configuration devices, currently manufactured in the ST Microelectronics Catania (Italy) fabrication plant, will be manufactured in the ST Microelectronics Ang Mo Kyo (Singapore) Wafer fabrication plant.

Reason for Change

This change is to ensure product availability and to be in a better position to meet long-term customer demand.

Products Affected

Table 1 lists the products affected by this change and the transition time frame.

Table 1. Products Scheduled to Ship from ST Ang Mo Kyo fabrication plant

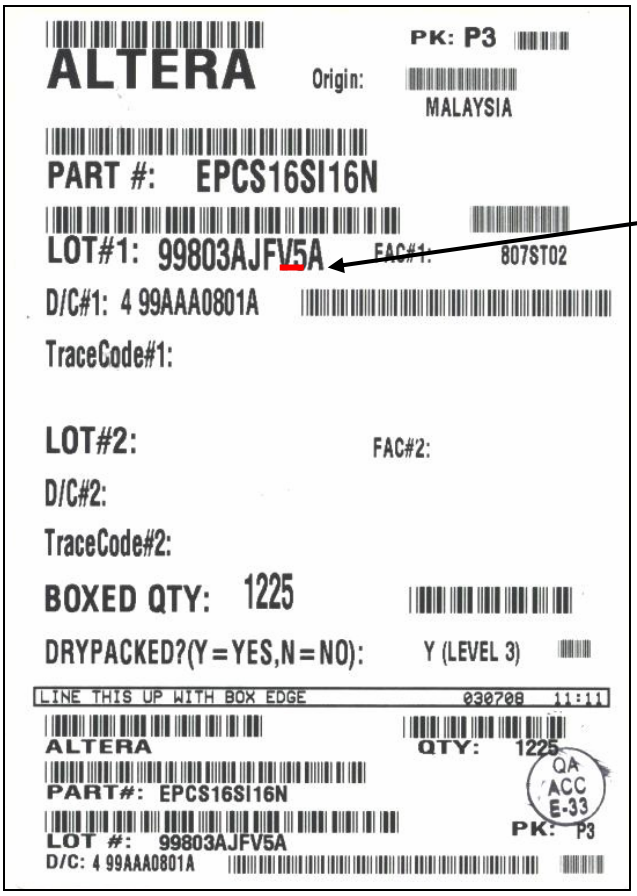
Product	Fab Location		Process Technology (µm)		Transition Time Frame
	Current	New	Current	New	
EPCS16SI8N	Catania	AMK	0.11µm	No Change	June 2008
EPCS16SI16N	Catania	AMK	0.11µm	No Change	June 2008
EPCS1SI8N (1)	Catania	AMK	0.15µm	No Change	August 2008
EPCS1SI8 (1)	Catania	AMK	0.15µm	No Change	August 2008
EPCS4SI8N	Catania	AMK	0.15µm	0.11µm	November 2008
EPCS4SI8	Catania	AMK	0.15µm	0.11µm	November 2008
EPCS64SI16N	Catania	AMK	0.13µm	0.11µm	August 2008
EPCS128SI16N	Catania	AMK	0.13µm	65nm	May 2009

Note (1): The EPCS1 mask will be revised to support an operating voltage range of 2.3V to 3.6V.

Product Traceability and Transition Dates

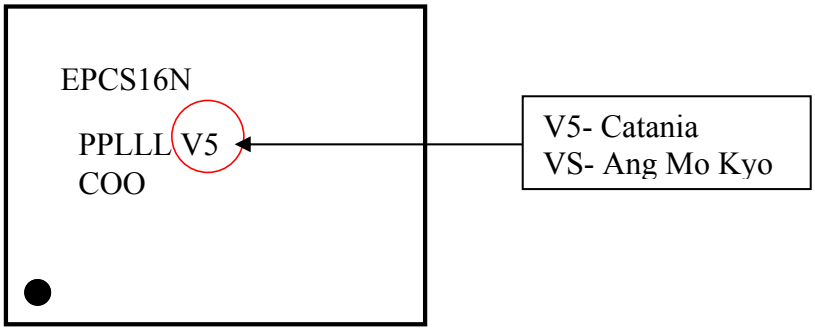
Devices manufactured at the ST Ang Mo Kyo fabrication plant can be identified on the box label. See Figure 1. For SOIC 16 packages, the unit marking will also indicate the fabrication plant. See Figure 2.

Figure 1. Fabrication Site Location Identification on Box label



V5- Catania
VS- Ang Mo Kyo

Figure 2. Fabrication Site Location Identification on Unit Marking for SOIC 16 Packages



Qualification Data

The device qualification data is summarized in Table 2.

Contact

For more information, please contact your local Altera sales representative or Altera Customer Quality Engineering at customer-quality@altera.com.

In accordance with JESD46-C, this change is deemed acceptable to the customer if no acknowledgement is received within 30 days from this notification.

Revision History

Date	Rev	Description
03/12/2008	1.0.0	Initial Release
04/30/2008	1.1.0	Updated Table 1 to include process technology information, revised EPCS1 transition date to August 2008 and added note with respect to operating voltage.

Table 2: Summary of Qualification Data (EPCS64 and EPCS16)

Sub-group	Test Procedure	Method	Test Conditions	Lot #1 EPCS64	Lot #2 EPCS16
1	High Temperature Operating Life	JEDEC/ JESD22-A108	140° C, 4.2V 168 hrs 500 hrs	 0/77 0/77	 0/77 --
2	Erase / Write Cycles	Internal	25° C 10,000 cyc 50,000 cyc 100,000 cyc	 0/77 0/77 0/77	 0/77 -- --
3	High Temperature Bake	JEDEC/ JESD22-A103	250° C 168 hrs 500 hrs	 0/77 0/77	 -- --
4	Electrostatic Discharge	JEDEC / JESD22 -A114 -A115	Human Body Model 1.5KΩ, 100pF Machine Model 0Ω, 200pF	-- --	> 2000 V > 200 V
5	Latch-Up	JEDEC-JESD78A	Class II – Level A	--	PASS