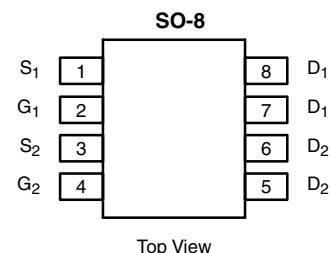


Dual N-Channel 40-V (D-S) MOSFET

PRODUCT SUMMARY

V _{DS} (V)	r _{DS(on)} (Ω)	I _D (A) ^a	Q _g (Typ)
40	0.060 at V _{GS} = 10 V	5.0	5.6
	0.070 at V _{GS} = 4.5 V	4.7	



Ordering Information: Si4908DY-T1-E3 (Lead (Pb)-free)

FEATURES

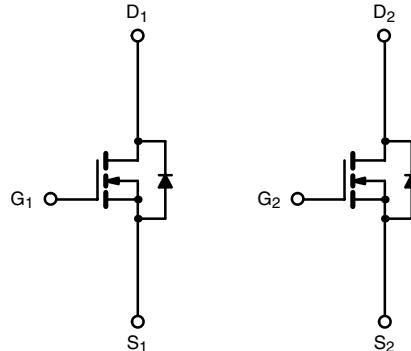
- TrenchFET® Power MOSFET
- 100 % R_g Tested

APPLICATIONS

- CCFL Inverter



RoHS
COMPLIANT



N-Channel MOSFET

N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C UNLESS OTHERWISE NOTED)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V _{DS}	40	V
Gate-Source Voltage	V _{GS}	±16	
Continuous Drain Current (T _J = 150 °C)	I _D	5	
		4.7	
		4.1 ^{b, c}	
		3.3 ^{b, c}	
Pulsed Drain Current (10 µs Pulse Width)	I _{DM}	20	A
Source-Drain Current Diode Current	I _S	2.3	
		1.5 ^{b, c}	
Pulsed Source-Drain Current	I _{SM}	20	
Single Pulse Avalanche Current	I _{AS}	7	mJ
Single Pulse Avalanche Energy	E _{AS}	2.5	
Maximum Power Dissipation	P _D	2.75	W
		1.75	
		1.85 ^{b, c}	
		1.18 ^{b, c}	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	-55 to 150	°C

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typ	Max	Unit
Maximum Junction-to-Ambient ^{b, d}	R _{thJA}	57	67.5	°C/W
Maximum Junction-to-Foot (Drain)	R _{thJF}	35	45	

Notes

- a. Based on T_C = 25 °C.
- b. Surface Mounted on 1" x 1" FR4 Board.
- c. t = 10 sec.
- d. Maximum under steady state conditions is 120 °C/W.

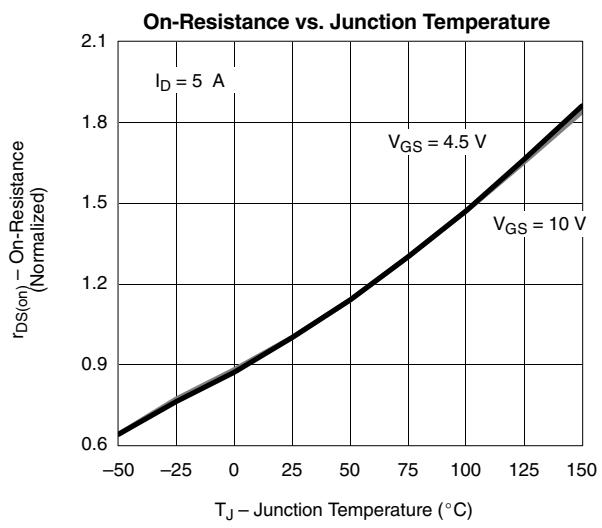
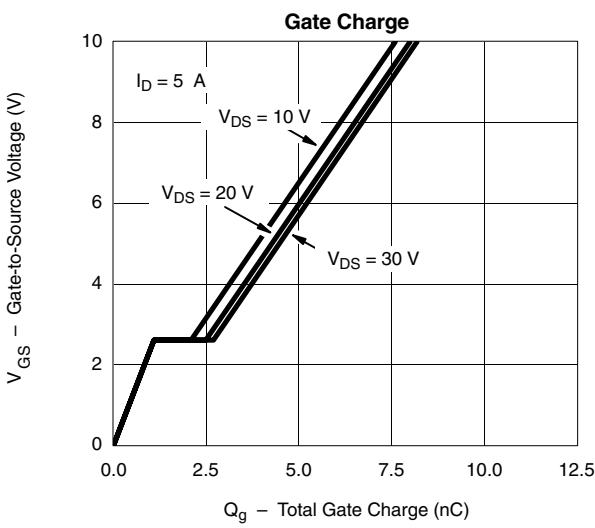
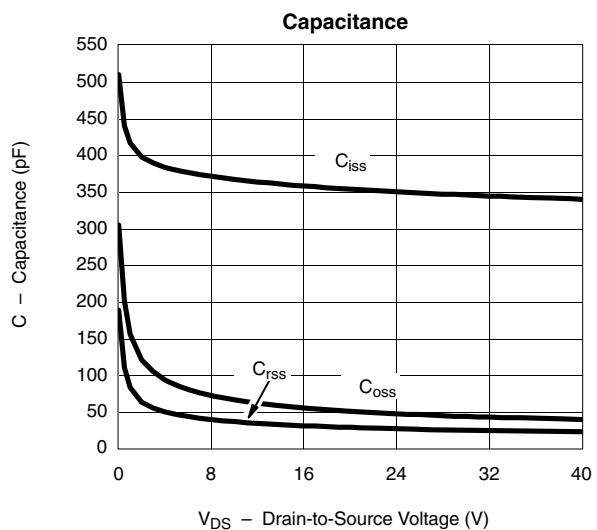
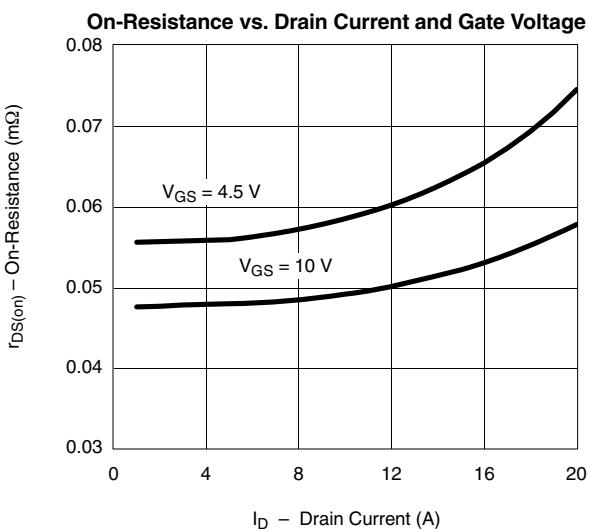
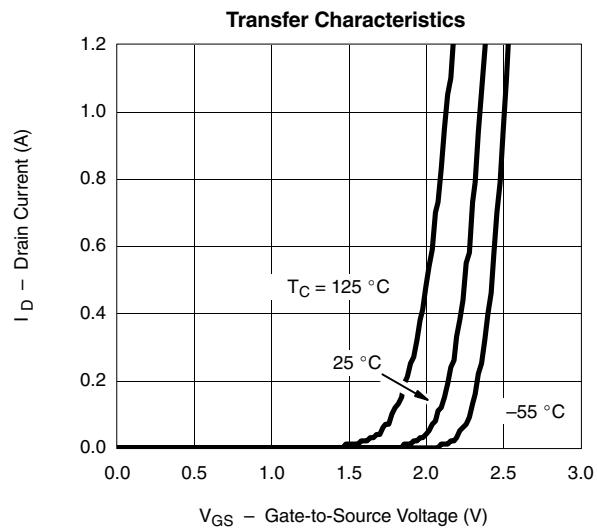
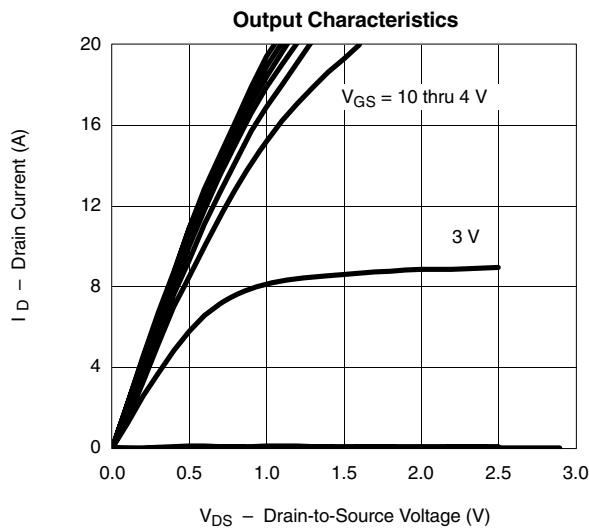
SPECIFICATIONS ($T_J = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

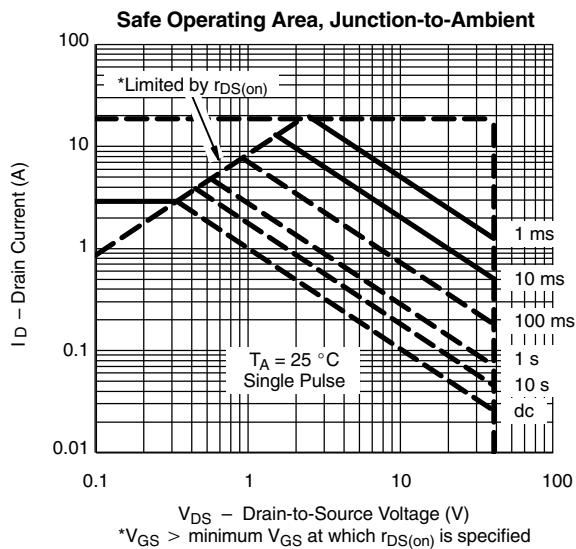
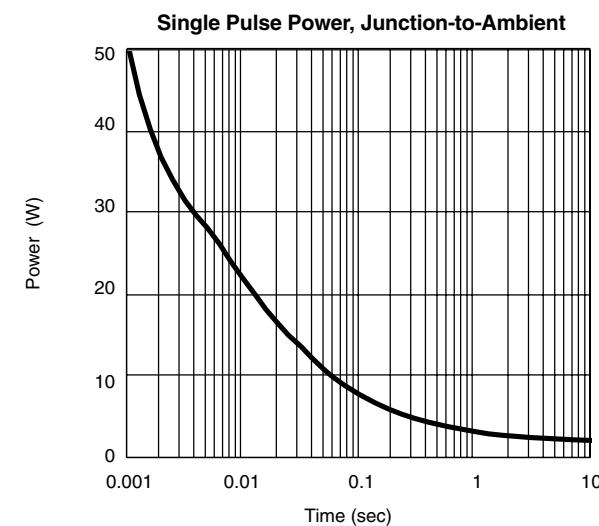
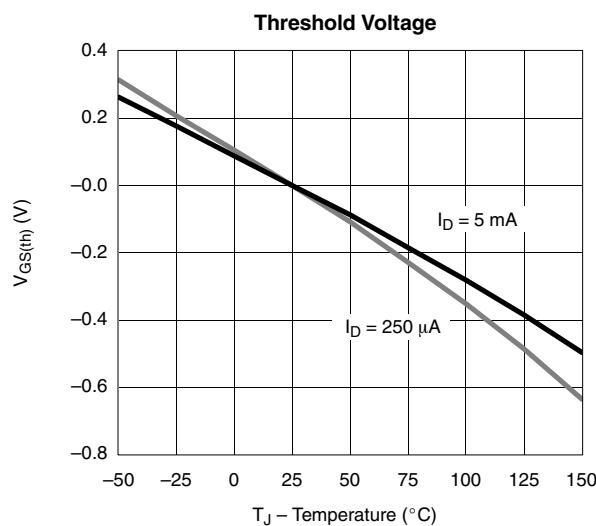
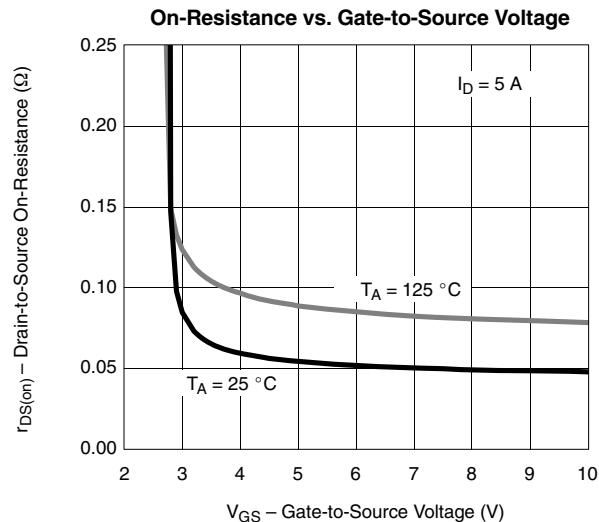
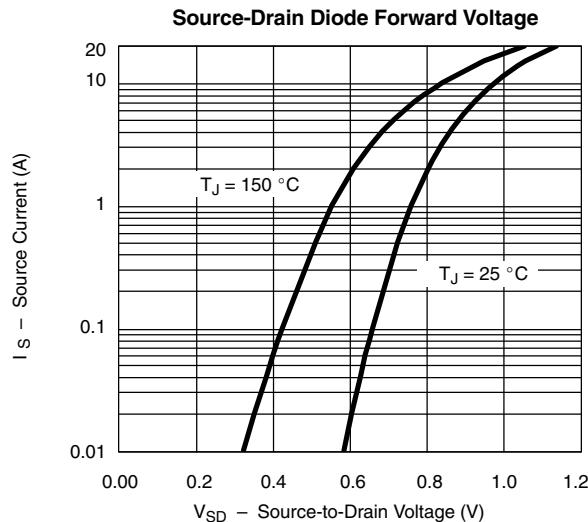
Parameter	Symbol	Test Condition	Min	Typ ^a	Max	Unit	
Static							
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	40			V	
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250 \mu\text{A}$		40			
$V_{GS(\text{th})}$ Temperature Coefficient	$\Delta V_{GS(\text{th})}/T_J$	$I_D = 250 \mu\text{A}$		-4.6			
Gate Threshold Voltage	$V_{GS(\text{th})}$	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$	0.8		2.2		
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 16 \text{ V}$		100		nA	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 40 \text{ V}, V_{GS} = 0 \text{ V}$		1		μA	
		$V_{DS} = 40 \text{ V}, V_{GS} = 0 \text{ V}, T_J = 55^\circ\text{C}$		10			
On-State Drain Current ^b	$I_{D(\text{on})}$	$V_{DS} = 5 \text{ V}, V_{GS} = 10 \text{ V}$	20			A	
Drain-Source On-State Resistance ^b	$r_{DS(\text{on})}$	$V_{GS} = 10 \text{ V}, I_D = 4.1 \text{ A}$		0.048	0.060	Ω	
		$V_{GS} = 4.5 \text{ V}, I_D = 3.8 \text{ A}$		0.056	0.070		
Forward Transconductance ^b	g_{fs}	$V_{DS} = 15 \text{ V}, I_D = 4.1 \text{ A}$		15		S	
Dynamic^a							
Input Capacitance	C_{iss}	N-Channel $V_{DS} = 20 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		355		pF	
Output Capacitance	C_{oss}			50			
Reverse Transfer Capacitance	C_{rss}			29			
Total Gate Charge	Q_g	N-Channel $V_{DS} = 20 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 5 \text{ A}$		8	12	nC	
Gate-Source Charge	Q_{gs}			3.7	6		
Gate-Drain Charge	Q_{gd}			1.1			
Gate Resistance	R_g			1.4			
Turn-On Delay Time	$t_{d(\text{on})}$	N-Channel $V_{DD} = 20 \text{ V}, R_L = 4 \Omega$ $I_D \approx 1 \text{ A}, V_{GEN} = 10 \text{ V}, R_g = 1 \Omega$		3.4	5.2	ns	
Rise Time	t_r			8	13		
Turn-Off Delay Time	$t_{d(\text{off})}$			20	30		
Fall Time	t_f			23	35		
Turn-On Delay Time	$t_{d(\text{on})}$			27	42		
Rise Time	t_r			74	110		
Turn-Off Delay Time	$t_{d(\text{off})}$	N-Channel $V_{DD} = 20 \text{ V}, R_L = 4 \Omega$ $I_D \approx 1 \text{ A}, V_{GEN} = 4.5 \text{ V}, R_g = 1 \Omega$		95	145	ns	
Fall Time	t_f			31	48		
				33	50		
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I_S	N-Channel $I_F = 2 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s}, T_J = 25^\circ\text{C}$			2.3	A	
Pulse Diode Forward Current ^a	I_{SM}				20		
Body Diode Voltage	V_{SD}			0.8	1.2	V	
Body Diode Reverse Recovery Time	t_{rr}			26	40		
Body Diode Reverse Recovery Charge	Q_{rr}			26	40	nC	
Reverse Recovery Fall Time	t_a			13			
Reverse Recovery Rise Time	t_b			13		ns	

Notes

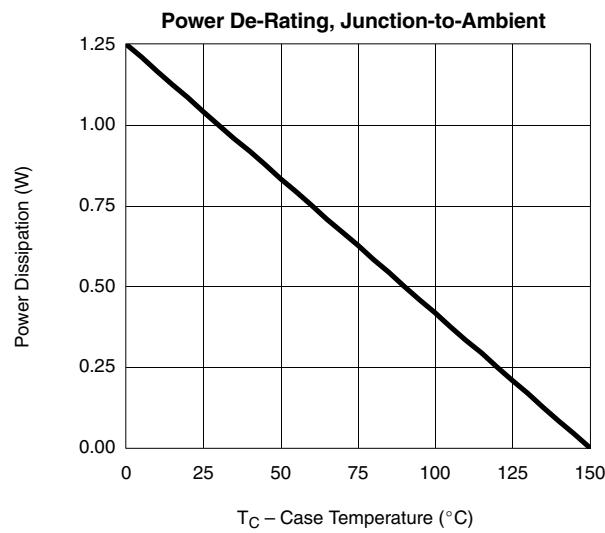
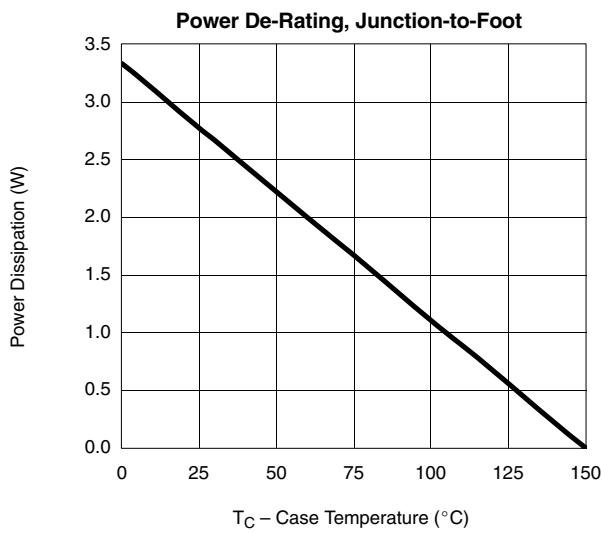
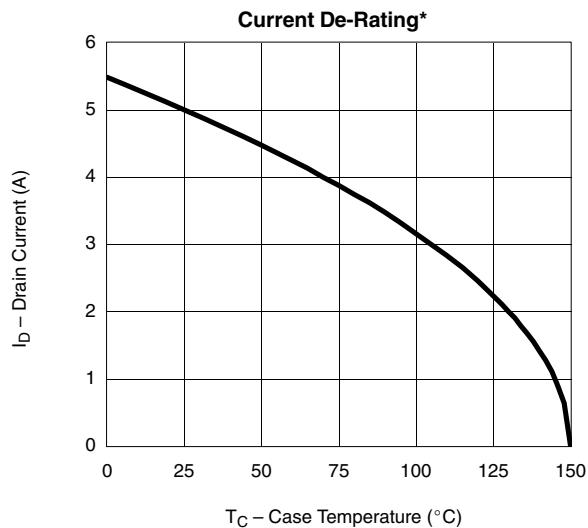
- a. Guaranteed by design, not subject to production testing.
- b. Pulse test; pulse width $\leq 300 \mu\text{s}$, duty cycle $\leq 2\%$.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

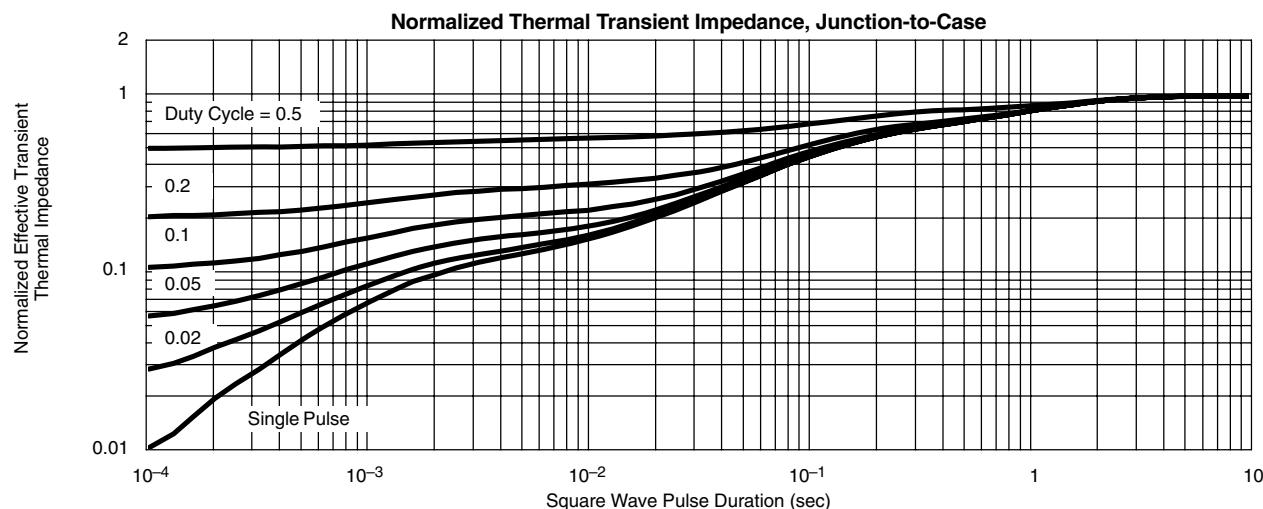
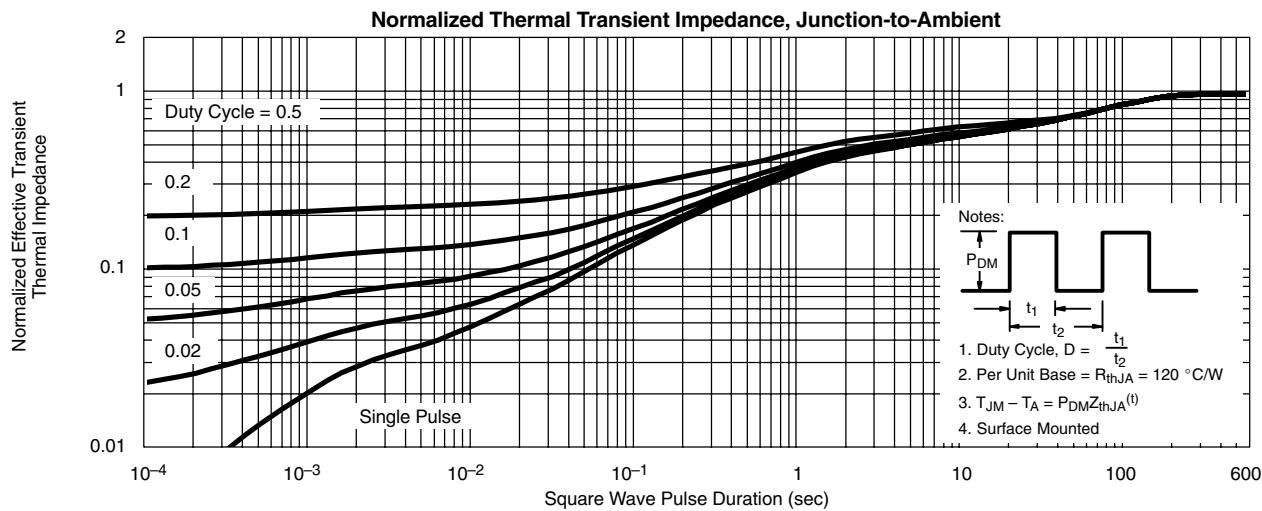
TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)


TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)

* $V_{GS} >$ minimum V_{GS} at which $r_{DS(on)}$ is specified

TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)


*The power dissipation P_b is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <http://www.vishay.com/ppg?73698>.



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