ispXPGA™ Family

March 2003 **Preliminary Data Sheet**

- **Non-volatile, Infinitely Reconfigurable**
  - Instant-on - Powers up in microseconds via on-chip E²CMOS® based memory
  - No external configuration memory
  - Excellent design security, no bit stream to intercept
  - Reconfigure SRAM based logic in milliseconds
- **High Logic Density for System-level Integration**
  - 139K to 1.25M system gates
  - 160 to 496 I/O
  - 1.8V, 2.5V, and 3.3V V_{CC} operation
  - Up to 414Kb sysMEM™ embedded memory
- **High Performance Programmable Function Unit (PFU)**
  - Four LUT-4 per PFU supports wide and narrow functions
  - Dual flip-flops per LUT-4 for extensive pipelining
  - Dedicated logic for adders, multipliers, multiplexers, and counters
- **Variable-Length Interconnect Routing Technology**
  - Optimum speed, power, and flexibility for logic interconnections
- **Flexible Memory Resources**
  - Multiple sysMEM Embedded RAM Blocks
    - Single port, Dual port, and FIFO operation
  - 64-bit distributed memory in each PFU
    - Single port, Double port, FIFO, and Shift Register operation
- **Eight sysCLOCK™ Phase Locked Loops (PLLs) for Clock Management**
  - True PLL technology
  - 10MHz to 320MHz operation
  - Clock multiplication and division
  - Phase adjustment
  - Shift clocks in 250ps steps
- **sysIO™ for High System Performance**
  - High speed memory support through SSTL and HSTL
  - Advanced buses supported through PCI, GTL+, LVDS, BLVDS, and LVPECL
  - Standard logic supported through LVTTL, LVCMOS 3.3, 2.5, and 1.8
  - Programmable drive strength for series termination
  - Programmable bus maintenance
- **sysHSI™ Capability for Ultra Fast Serial Communications**
  - Up to 850Mbps performance
  - Up to 20 channels per device
  - Built in Clock Data Recovery (CDR) and Serialization and De-serialization (SERDES)
- **Flexible Programming, Reconfiguration, and Testing**
  - IEEE 1532 and 1149.1 compliant
  - Microprocessor configuration interface
  - Program E²CMOS while operating from SRAM

Table 1. ispXPGA Family Selection Guide

	ispXPGA 125	ispXPGA 200	ispXPGA 500	ispXPGA 1200
System Gates	139K	210K	476K	1.25M
PFUs	484	676	1764	3844
LUT-4s	1936	2704	7056	15376
Logic FFs	3.8K	5.4K	14.1K	30.7K
sysMEM Memory	92K	111K	184K	414K
Distributed Memory	30K	43K	112K	246K
EBR	20	24	40	90
sysHSI Channels	4	8	12	20
User I/O	160/176	160/208	336	496
Packaging	256 fpBGA 516 fpBGA[1]	256 fpBGA 516 fpBGA[1]	516 fpBGA[1] 900 fpBGA	680 fpSBGA[1] 900 fpBGA

1. Thermally enhanced package.

Note: LFX1200B/C is preliminary, LFX125/200/500B/C information is advanced.

ispXPGA Family Overview

The ispXPGA family of devices allows the creation of high-performance logic designs that are both non-volatile and infinitely re-programmable. Other FPGA solutions force a compromise being either re-programmable or non-volatile. This family couples this capability with a mainstream architecture containing the features required for today's system-level design.

Electrically Erasable CMOS (E^2CMOS) memory cells provide the ispXPGA family with non-volatile capability. These allow logic to be functional microseconds after power is applied, allowing easy interfacing in many applications. This capability also means that expensive external configuration memories are not required and that designs can be secured from unauthorized read back. Internal SRAM cells allow the device to be infinitely reconfigured if desired. Both the SRAM and E^2CMOS cells can be programmed and verified through the IEEE 1532 industry standard. Additionally, the SRAM cells can be configured and read-back through the sysCONFIG™ peripheral port.

The family spans the density and I/O range required for the majority of today's logic designs, 139K to 1.25M system gates and 160 to 496 I/O. The devices are available for operation from 1.8V, 2.5V, and 3.3V power supplies, providing easy integration into the overall system.

The system-level needs of designers are met through the incorporation of sysMEM dual-port memory blocks, sysIO advanced I/O support, and sysCLOCK Phase Locked Loops (PLLs). High-speed serial communications are supported through multiple sysHSI blocks, which provide clock data recovery (CDR) and serialization/de-serialization (SERDES).

The ispLEVER™ design tool from Lattice allows designers easy implementation of designs using the ispXPGA product. Synthesis library support is available for the major logic synthesis tools. The ispLEVER tool takes the output from these common synthesis packages and place and routes the design in the ispXPGA product. The tool allows floor planning and the management of other constraints within the device. The tool also provides outputs to common timing analysis tools for timing analysis.

To increase designer productivity, Lattice provides a variety of pre-designed modules referred to as IP cores for the ispXPGA product. These IP cores allow designers to concentrate on the unique portions of their design while using pre-designed block to implement standard functions such as bus-interfaces, standard communication-interfaces, and memory-controllers.

Through the use of advanced technology and innovative architecture the ispXPGA FPGA devices provide designers with excellent speed performance. Although design dependent, many typical designs can run at over 150MHz. Certain designs can run at over 300MHz. Table 2 details the performance of several building blocks commonly used by logic designers.

Table 2. ispXPGA Speed Performance for Typical Building Blocks

Function	Performance
8:1 Asynch MUX	150 MHz
1:32 Asynch Demultiplexer	125 MHz
8 x 8 2-LL Piped Multiplier	225 MHz
32-bit Up/Down Counter	290 MHz
32-bit Shift Register	360 MHz

Architecture Overview

The ispXPGA architecture is a symmetrical architecture consisting of an array of Programmable Function Units (PFUs) enclosed by Input Output Groups (PICs) with columns of sysMEM Embedded Block RAMs (EBRs) distributed throughout the array. Figure 1 illustrates the ispXPGA architecture. Each PIC has two corresponding sysIO blocks, each of which includes one input and output buffer. On two sides of the device, between the PICs and the sysIO blocks, there are sysHSI High-Speed Interface blocks. The symmetrical architecture allows designers to easily implement their designs, since any logic function can be placed in any section of the device.

The PFUs contain the basic building blocks to create logic, memory, arithmetic, and register functions. They are optimized for speed and flexibility allowing complex designs to be implemented quickly and efficiently.

The PICs interface the PFUs and EBRs to the external pins of the device. They allow the signals to be registered quickly to minimize setup times for high-speed designs. They also allow connections directly to the different logic elements for fast access to combinatorial functions.

The sysMEM EBRs are large, fast memory elements that can be configured as RAM, ROM, FIFO, and other storage types. They are designed to facilitate both single and dual-port memory for high-speed applications.

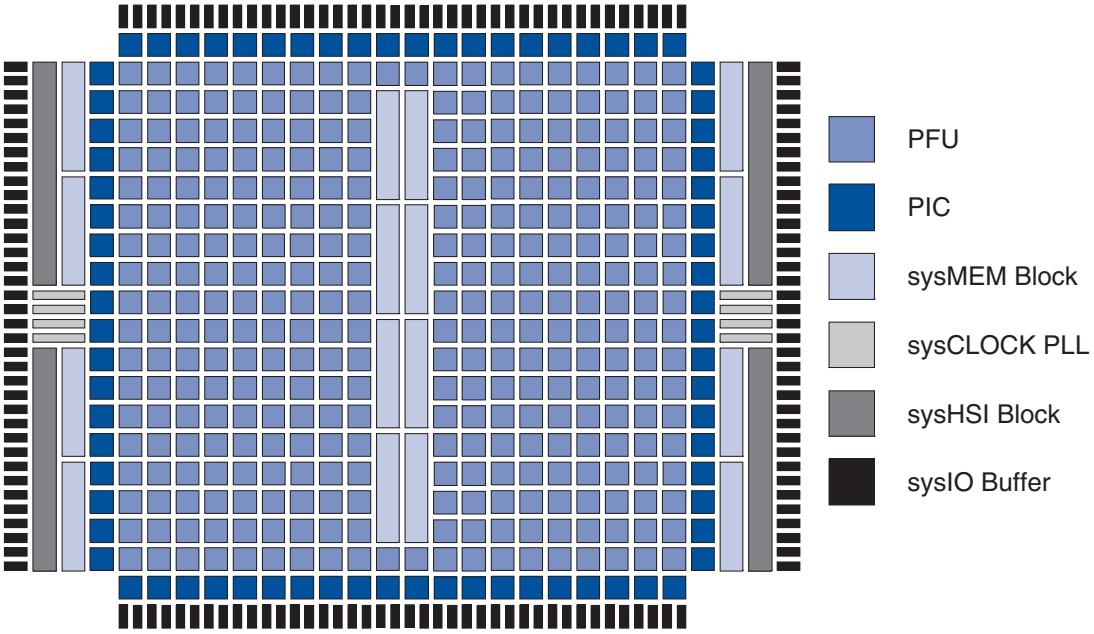
These three components of the architecture are interconnected via a high-speed, flexible routing array. The routing array consists of Variable Length Interconnect (VLI) lines between the PICs, PFUs, and EBRs. There is additional routing available to the PFU for feedback and direct routing of signals to adjacent PFUs or PICs.

The sysIO blocks consist of configurable input and output buffers connected directly to the PICs. These buffers can be configured to interface with 16 different I/O standards. This allows ispXPGA to interface with other devices without the need for external transceivers.

The sysHSI blocks provide the necessary components to allow the ispXPGA device to transfer data at up to 850Mbps using the LVDS standard. These components include serializing, de-serializing, and clock data recovery (CDR) logic.

The sysCLOCK blocks provide clock multiplication/division, clock distribution, delay compensation, and increased performance through the use of PLL circuitry that manipulates the global clocks. There is one sysCLOCK block for each global clock tree in the device.

Figure 1. ispXPGA Block Diagram



Programmable Function Unit

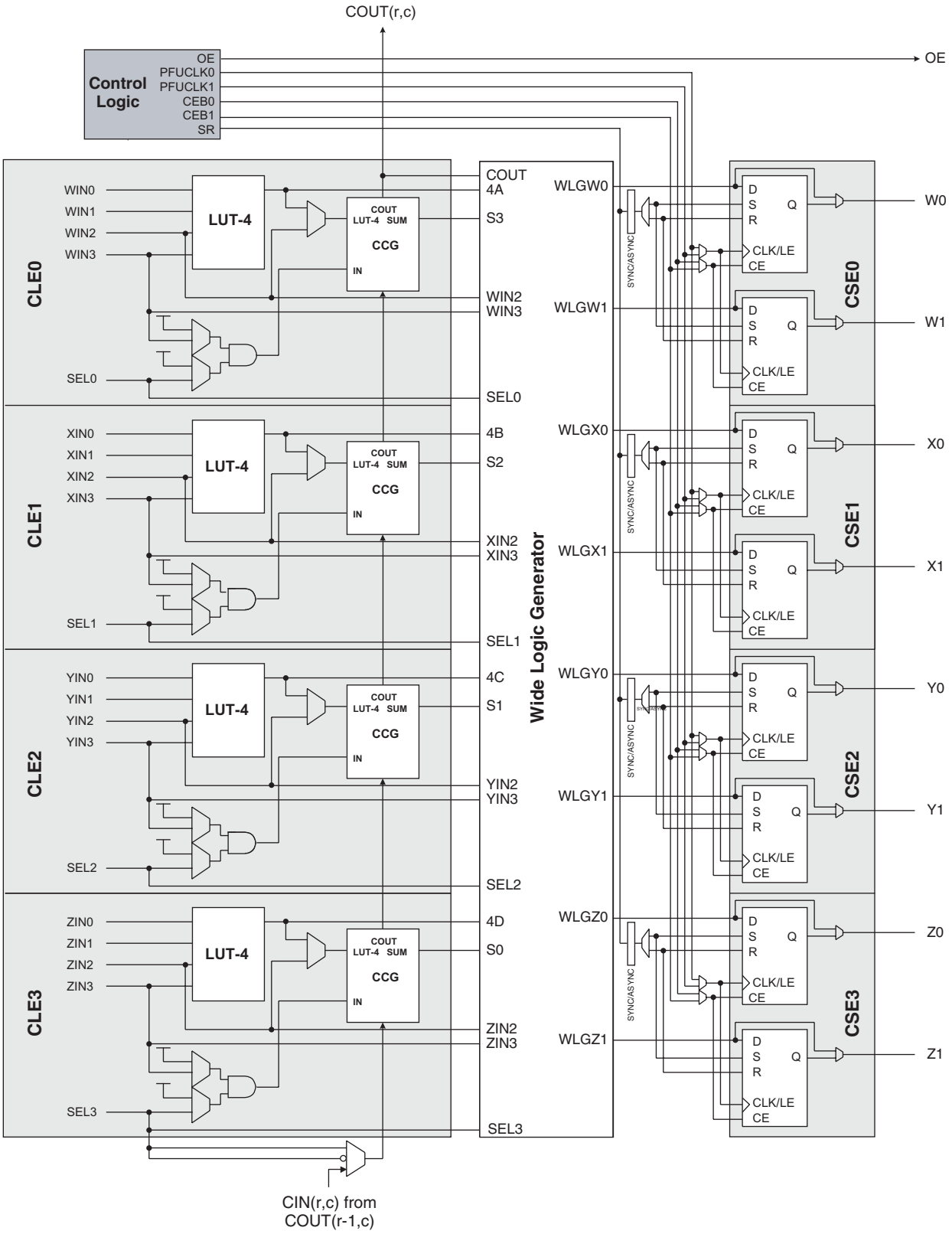
The Programmable Function Unit (PFU) is the basic building block of the ispXPGA architecture. The PFUs are arranged in rows and columns in the device with PFU (1,1) referring to (row 1, column 1). Each PFU consists of four Configurable Logic Elements (CLEs), four Configurable Sequential Elements (CSEs), and a Wide Logic Generator (WLG). By utilizing these components, the PFU can implement a variety of functions. Table 3 lists some of the function capabilities of the PFU.

There are 57 inputs to each PFU and nine outputs. The PFU uses 20 inputs for logic, and 37 inputs drive the control logic from which six control signals are derived for the PFU.

Table 3. Function Capability of ispXPGA PFU

Function	Capability
Look-up table	LUT-4, LUT-5, LUT-6
Wide logic functions	Up to 20 input logic functions
Multiplexing	2:1, 4:1, 8:1
Arithmetic logic	Dedicated carry chain and booth multiplication logic
Single-port RAM	16X1, 16X2, 16X4, 32X1, 32X2, 64X1
Double-port RAM	16X1, 16X2, 32X1
Shift register	8-bit shift registers (up to 32-bit shift capability)

Figure 2. ispXPGA PFU



Configurable Logic Element

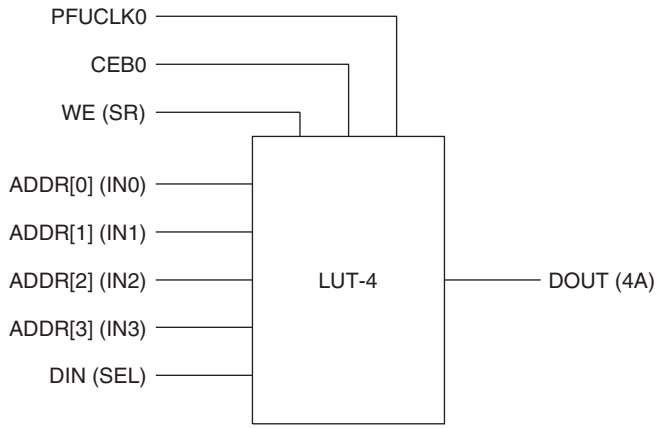
The CLE is made up of a four-input Look-up Table (LUT-4), a Carry Chain Generator (CCG), and a two-input AND gate. The LUT-4 creates various combinatorial and memory elements, the CCG creates a single one-bit full adder, and the two-input AND gate can expand the CCG to incorporate Booth Multiplier capability by feeding the output of the AND gate to one of the inputs of the CCG.

Of the five inputs that feed each CLE, two are dedicated inputs into each LUT-4 and the remaining three take on varying functionality. The third and fourth inputs can be used as either inputs to the LUT-4 or as a Feed-Thru to the CSE via the WLG. The fifth input can be a data port when the LUT is configured as Distributed Memory, a select line for multiplexer operation, or a Feed-Thru directly to the CSE via the WLG (Figure 2).

Look-Up Table – Combinatorial Mode
In combinatorial mode, the LUT-4 can implement any logic function up to four inputs. By using the carry chain and the WLG, each LUT-4 can be combined to form the enhanced functions listed in Table 3.

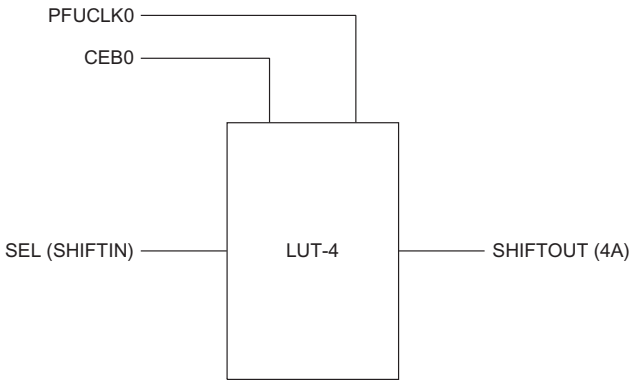
Look-Up Table – Distributed Memory Mode
In the distributed memory mode, the LUT functions as a memory element. The inputs to the LUT function as Address and Data. Each PFU is capable of implementing up to 64 SRAM bits. Both single and double port RAM can be performed in the PFU (Table 3). Furthermore, the distributed memory can be configured as either synchronous or asynchronous memory. Figure 3 illustrates the LUT while in distributed memory mode. When using any LUT in the PFU in memory mode, the Set/Reset signal will be used for Write Enable (WE(SR)) and the CLK0 signal will be used as the clock for synchronous read and write.

Figure 3. LUT in Distributed Memory Mode



Look-Up Table – Shift Register Mode
In the shift register mode, the LUT functions as a 1-bit to 8-bit shift register. This means that each PFU can implement up to four 8-bit shift registers or any cascaded combination. Figure 4 illustrates the LUT when configured in shift register mode.

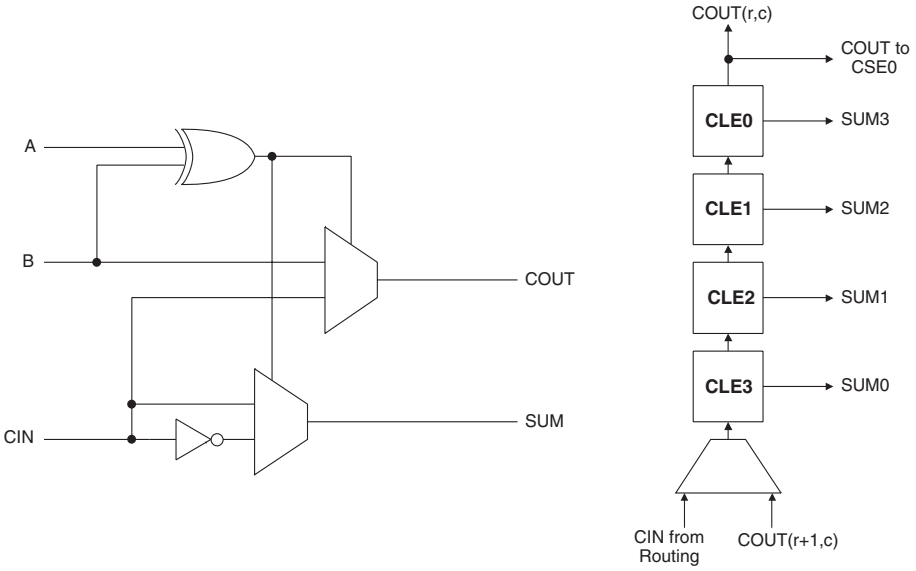
Figure 4. LUT in Shift Register Mode



Carry Chain Generator

The Carry Chain Generator is useful for implementing high-speed arithmetic functions. The CCG consists of a two-input XOR gate whose carryout can be cascaded with the input of the adjacent CCG. As shown in Figure 5, the carryin signal feeds CLE3 of the PFU and is propagated through CLE2 and CLE1 before reaching CLE0. The sum output of the CCG can be fed to the CSE through the WLG. The carryout must propagate to CLE0 for use outside the PFU. The carryout from the PFU can feed the W0 input of CSE0. The CCG also helps to effectively implement wider functions by using its logic elements to expand the capabilities of the LUT-4.

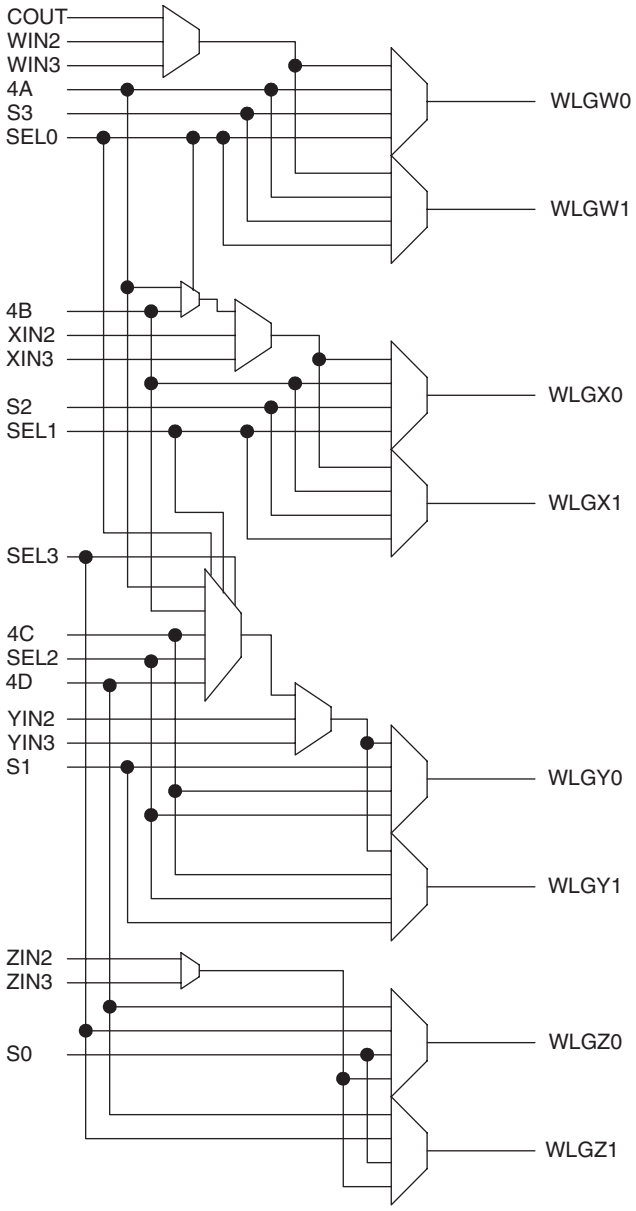
Figure 5. Carry Chain Generator



Wide Logic Generator

The WLG contains the logic necessary to implement wide gate functions. This is made up of a set of multiplexers that are located between the CLE and the CSE. The WLG helps in enhancing the wide gating capability of the PFU. The outputs of each CLE can be cascaded in the WLG to build wide gating functions. Wide multiplexing functions are also possible with a similar use of the WLG. Figure 6 illustrates the WLG.

Figure 6. ispXPGA Wide Logic Generator



Configurable Sequential Element

There are two registers in each CSE for a total of eight registers in each PFU. This high register count assists in implementing efficient pipelined applications with no utilization penalty. Each register can be configured as a latch or D type flip-flop with either synchronous or asynchronous set or reset. Figure 2 shows the signals that feed the register's D inputs. Feed-through signals in the architecture ensure that registers are efficiently utilized even if the accompanying LUT is occupied.

Control Logic

The control signals available to the registers in a PFU are Clock, Clock Enable, and Set/Reset. Figure 7 shows the various options available to generate the clock signal. As can be seen, the clock signal is the output of a 12:1 MUX with true and compliment versions available from the 12:1 MUX. Each CSE can chose whether it uses the true or compliment form of the clock. Figure 8 shows the Set/Reset selection for each PFU in the ispXPGA. A common

Set/Reset signal controls all the registers for each PFU. This common Set/Reset signal is composed of the logical OR term of the Global Set/Reset signal (GSR) and the selected signal from routing. The polarity of this signal is not controllable inside the PFU. Figure 9 shows the Clock Enable and Output Enable selection for each PFU.

Figure 7. Clock Selection per PFU

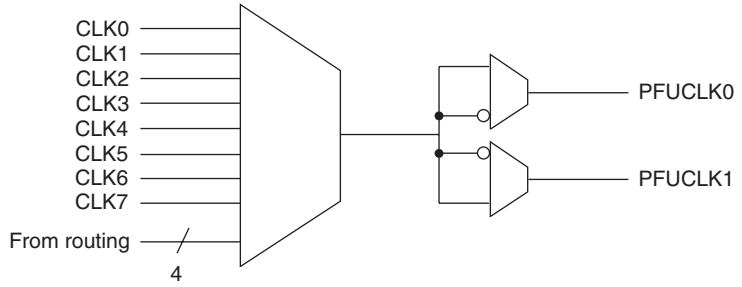


Figure 8. Set/Reset Selection per PFU

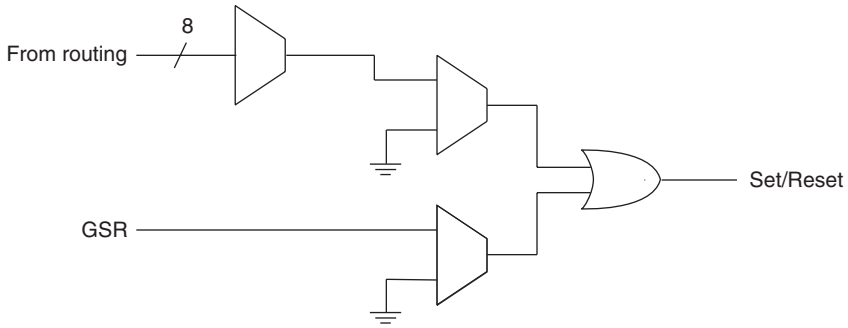
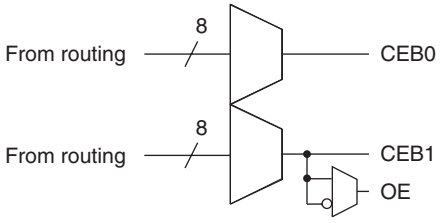


Figure 9. Clock Enable and Output Enable Selection per PFU

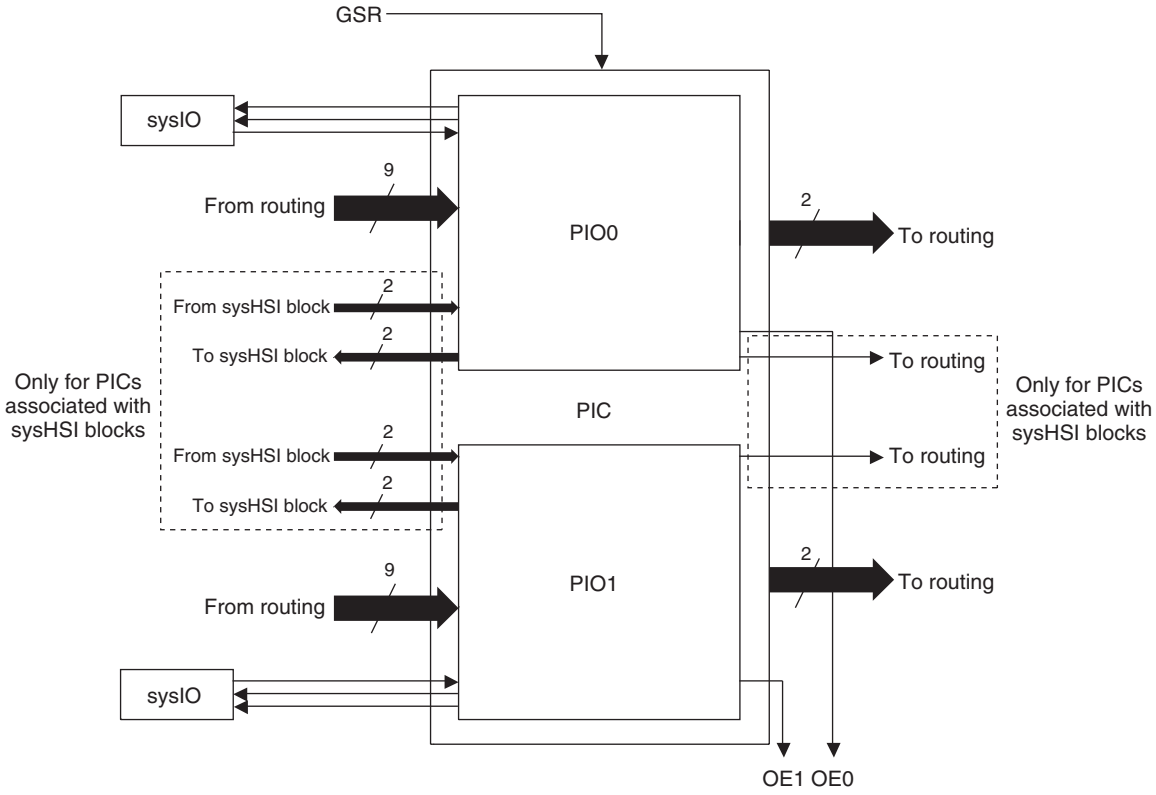


Programmable Input/Output Cell

The Programmable Input/Output Cell (PIC) is an essential part of the symmetrical architecture of the ispXPGA Family. The PICs interface the PFUs and EBRs to the sysIO and sysHSI blocks of the device.

Each PIC contains two Programmable Input/Outputs (PIOs) with a total of 21 inputs and 10 outputs. There are 18 inputs from routing, two inputs from the sysIO buffers, and the Global Set/Reset signal. Four outputs of the PIC connect to routing and two outputs are available as Output Enables for the tri-statable Long Lines. The remaining four outputs feed the sysIO buffers directly (one output enable and one output to each). Each PIC associated with a sysHSI block has four additional inputs and six additional outputs to support the sysHSI blocks. The four additional inputs come from the sysHSI block associated with the PIC. The four of the six additional outputs come from the PIC outputs and feed the sysHSI block, while the remaining two outputs feed routing. Figure 10 shows the block diagram of the PIC with the sysHSI block inputs and outputs.

Figure 10. ispXPGA PIC



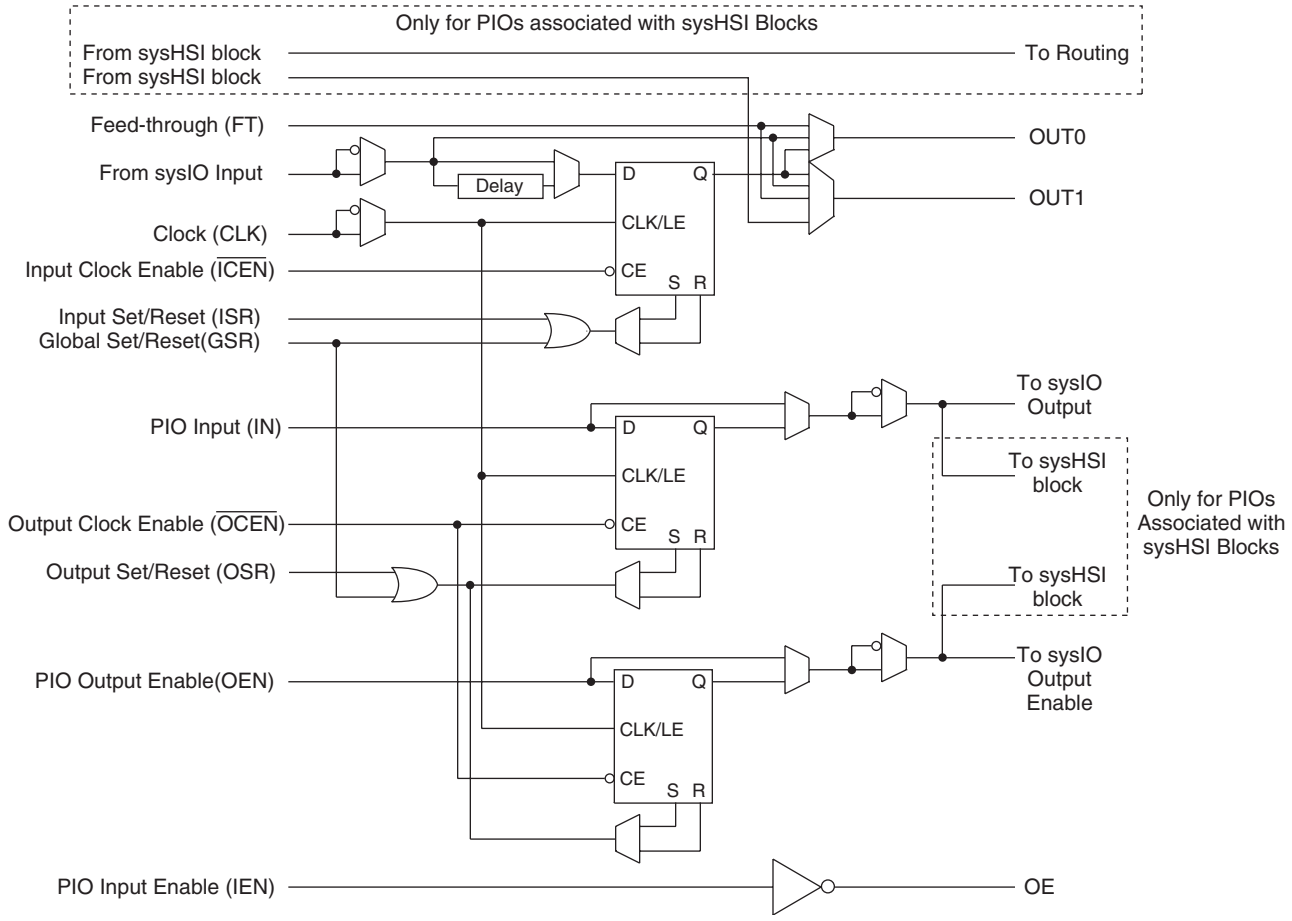
Programmable Input/Output

The PIO is the building block of a PIC. The PIO has a total of 11 inputs and five outputs. Nine of the 11 inputs are generated from routing. The inputs from routing are the PIO Input (IN), Feed-Thru (FT), Clock (CLK), Input Clock Enable (ICE), Input Set/Reset (ISR), Output Clock Enable (OCEN), Output Set/Reset (OSR), PIO Output Enable (OEN), and PIO Input Enable (IEN). The remaining inputs are the sysIO input buffer signal and the Global Set/Reset signal. Three of the five outputs (OUT0, OUT1, and OE) feed routing. The last two outputs feed the sysIO buffer directly as the output and output enable of the sysIO output buffer.

PIOs associated with sysHSI blocks contain two additional inputs and outputs to support the sysHSI block. The two inputs come from the sysHSI block associated with the PIO, and the two outputs feed the sysHSI block. One of the inputs routes directly through the PIO to routing, while the other is multiplexed with the Feed-Thru, register bypass, and Q output of the register to form the OUT1 output of the PIO. The outputs to the sysHSI block are the same signals as the outputs which feed the sysIO buffers (sysIO Output and sysIO Output Enable).

Each PIO has an input register, an output register, and an output enable register as shown in Figure 11. The input register path of the PIO has a ‘delay’ option, which slows the data-flow. A two-input OR function of the Global Set/Reset (GSR) and Set/Reset (ISR or OSR) signals creates the set/reset term for the respective registers. Each PIO has two pairs of set/reset and clock enable signals. One is exclusive to the input register, whereas the other is common for both the output and output enable registers. The clock (CLK) is common to all registers in a PIO, and the polarity of the clock is controllable. The input, output, and the output enable registers can be configured as a latch or D-type flip-flop. Each PIO is capable of generating an output enable signal, which in turn becomes a PIC output.

Figure 11. ispXPGA PIO



VLI Routing Resources

The ispXPGA architecture contains a Variable-Length-Interconnect (VLI) routing technology connecting the PFUs, PICs, and EBRs in the device. There are four types of routing resources, Global Lines, Long Lines, General Interconnect, and Local Lines forming the global routing structure. This allows a signal to be routed to any element in the device with the optimal delay.

The Global Lines consist of global clock lines and a global set/reset line. These lines are routed to all elements in the device. They are specifically designed for high speed, predictable timing regardless of fan-out. The global clock lines can also be used as dedicated inputs.

The Long Lines consist of Horizontal and Vertical Long Lines (HLL and VLL). The VLL and HLL are tri-statable lines spanning the entire device. These lines allow fast routing for high fan-out nets and general-purpose functions.

The General Interconnect consists of Double and Deca Lines. The Double Lines connect up to three elements (two plus the driving element), while the Deca Lines connect up to eleven elements (ten plus the driving element).

The Local Lines are extremely fast routing paths consisting of Feedback and Direct Connect Lines. The Feedback Lines are internal routing paths from the PFU outputs to the PFU inputs. The Direct Connect Lines connect all adjacent elements.

The Common Interface Block (CIB) provides the link between the logic element (PFU, PIC, or EBR) and the VLI Routing resources. The CIB is a switch matrix that can be programmed to connect virtually any routing resource to any input or output of the logic element.

Memory

The ispXPGA architecture provides a large amount of resources for memory intensive applications. Embedded Block RAMs (EBRs) are available to complement the Distributed Memory that is configured in the PFUs (see Look-Up Table -Distributed Memory Mode in the PFU section above). Each memory element can be configured as RAM or ROM. Additionally, the internal logic of the device can be used to configure the memory elements as FIFO and other storage types. These EBRs are referred to as sysMEM blocks. Refer to Table 1 for memory resources per device.

sysMEM Blocks

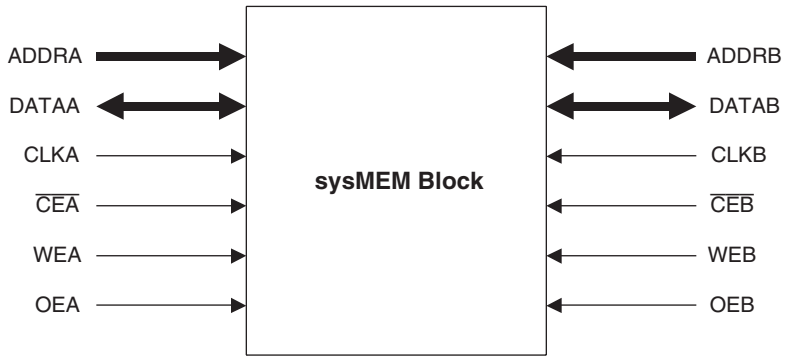
The sysMEM blocks are organized in columns distributed throughout the device. Each EBR contains 4.6K bits of dual-port RAM with dedicated control, address, and data lines for each port. Each column of sysMEM blocks has dedicated address and control lines that can be used by each block separately or cascaded to form larger memory elements. The memory cells are symmetrical and contain two sets of identical control signals. Each port has a read/write clock, clock enable, write enable, and output enable. Figure 12 illustrates the sysMEM block.

The ispXPGA memory block can operate as single-port or dual-port RAM. Supported configurations are:

- 512 x 9 bits single-port (8 bits data / 1 bit parity)
- 256 x 18 bits single-port (16 bits data / 2 bits parity)
- 512 x 9 bits dual-port (8 bits data / 1 bit parity)
- 256 x18 bits dual-port (16 bits data / 2 bits parity)

The data widths of “9” and “18” are ideal for applications where parity is necessary. This allows 9 data bits, 8 data bits plus a parity bit, 18 data bits, or 16 data bits plus two parity bits. The logic for generating and checking the parity must be customized separately.

Figure 12. sysMEM Block Diagram

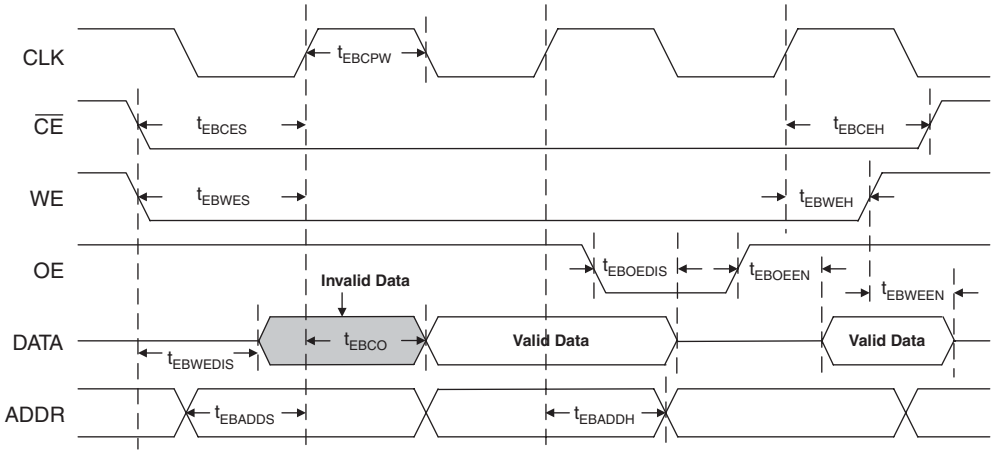


Read and Write Operations

The ispXPGA EBR has fully synchronous read and write operations as well as an asynchronous read operation. These operations allow several different types of memory to be implemented in the device.

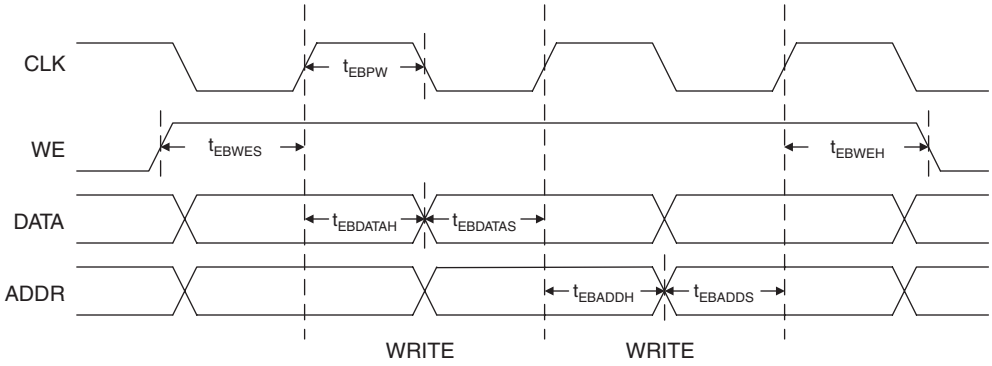
Synchronous Read: The Clock Enable ($\overline{CE}$) and Write Enable (WE) signals control the synchronous read operation. When the $\overline{CE}$ signal is low, the clock is enabled. When the WE signal is low the read operation begins. Once the address (ADDR) is present, a rising clock edge (or falling edge depending on polarity) causes the stored data to be available on the DATA port. Figure 13 illustrates the synchronous read timing.

Figure 13. EBR Synchronous Read Timing Diagram



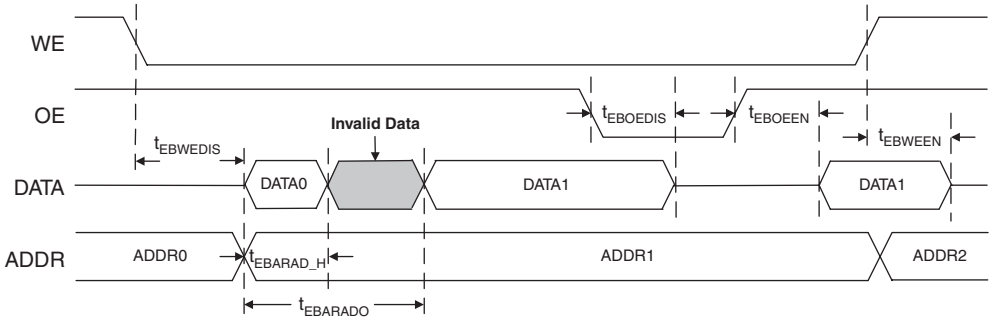
Synchronous Write: The WE signal controls the synchronous write operation. When the WE signal is high and the write operation begins. Once the address and data are present and the Output Enable (OE) is active, a rising clock edge (or falling edge depending on polarity) causes the data to be stored into the EBR. Figure 14 illustrates the synchronous write timing.

Figure 14. EBR Synchronous Write Timing Diagram



Asynchronous Read: The WE signal controls the asynchronous read operation. When the WE signal is low, the read operation begins. Shortly after the address is present, the stored data is available on the DATA port. Figure 15 illustrates the asynchronous read timing. For more information about the EBR, refer to Lattice technical note number TN1028 *ispXPGA Memory Usage Guidelines,* available at www.latticesemi.com.

Figure 15. EBR Asynchronous Read Timing Diagram



sysCLOCK PLL Description

The sysCLOCK PLL circuitry consists of Phase-Lock Loops (PLLs) and the various dividers, reset, and feedback signals associated with the PLLs. This feature gives the user the ability to synthesize clock frequencies and generate multiple clock signals for routing within the device. Furthermore, it can generate clock signals that are aligned either at the board level or the device level.

The ispXPGA devices provide up to eight PLLs. Each PLL receives its input clock from its associated global clock pin, and its output is routed to the associated global clock net. For example, PLL0 receives its clock input from the GCLK0 global clock pin and provides output to the CLK0 global clock net. The PLL also has the ability to output a secondary clock that is a division of the primary clock output. When using the secondary clock, the secondary clock will be routed to the neighboring global clock net. For example, PLL0 will drive its primary clock output on the CLK0 global clock net and its secondary clock output will drive the CLK1 global clock net. Additionally, each PLL has a set of PLL_RST, PLL_FBK, and PLL_LOCK signals. The PLL_RST signal can be generated through routing or a dedicated dual-function I/O pin. The PLL_FBK signal can be generated through a dedicated dual-function I/O pin or internally from the Global Clock net associated with the PLL. The PLL_LOCK signal feeds routing directly from the sysCLOCK PLL circuit. Figure 17 illustrates how the PLL_RST and PLL_FBK signals are generated.

Each PLL has four dividers associated with it, M, N, V, and K. The M divider is used to divide the clock signal, while the N divider is used to multiply the clock signal. The V divider allows the VCO frequency to operate at higher frequencies than the clock output, thereby increasing the frequency range. The K divider is only used when a secondary clock output is needed. This divider divides the primary clock output and feeds to the adjacent global clock net. Different combinations of these dividers allow the user to synthesize clock frequencies. Figure 16 shows the ispXPGA PLL block diagram.

The PLL also has a delay feature that allows the output clock to be advanced or delayed to improve set-up and clock-to-out times for better performance. This operates by inserting delay on the input or feedback lines of the PLL. For more information on the PLL, please refer to Lattice technical note number TN1003, *sysCLOCK PLL Usage and Design Guidelines,* available at www.latticesemi.com.

Figure 16. ispXPGA PLL Block Diagram

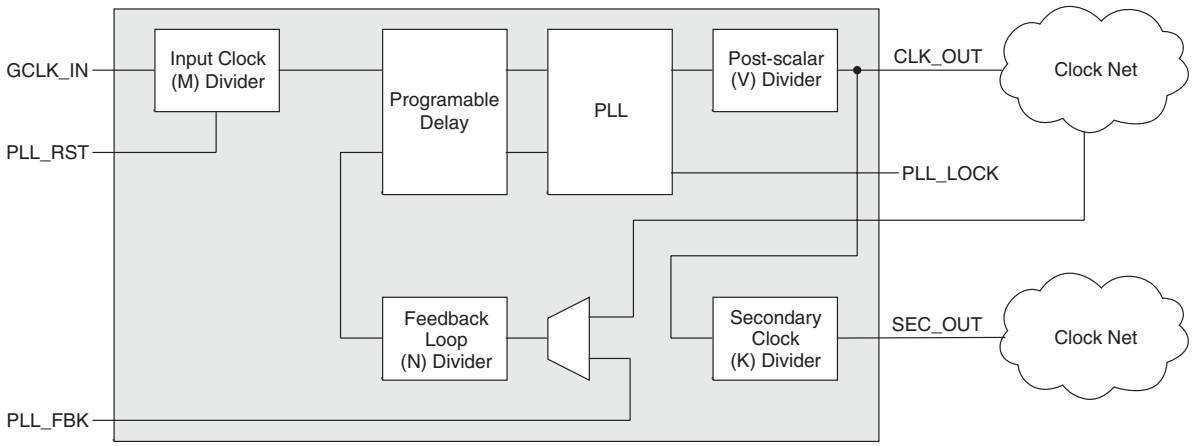
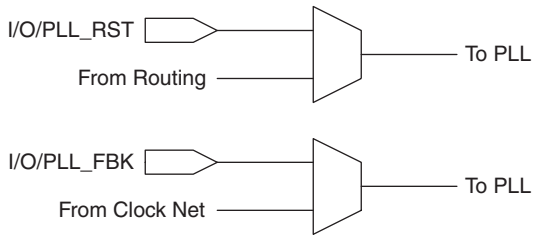


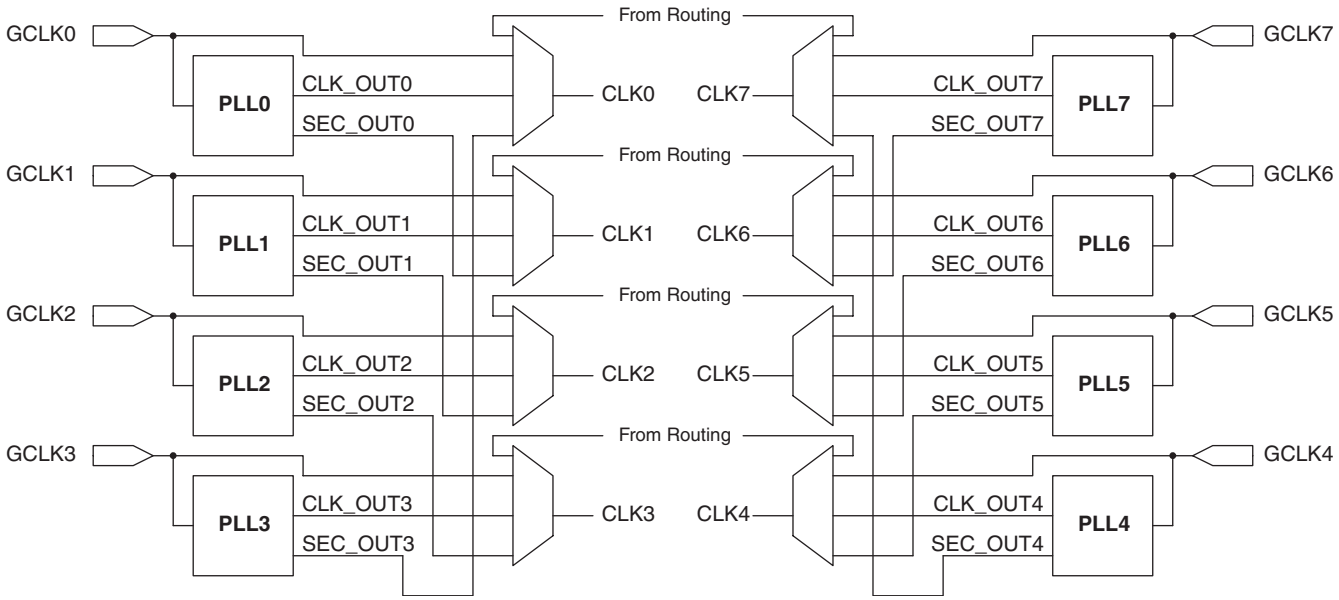
Figure 17. ispXPGA PLL_RST and PLL_FBK Generation



Clock Routing

The Global Clock Lines (GCLK) have two sources, their dedicated pins and the sysCLOCK circuit. Figure 18 illustrates the generation of the Global Clock Lines.

Figure 18. Global Clock Line Generation



sysIO Capability

All the ispXPGA devices have eight sysIO banks, where each bank is capable of supporting multiple I/O standards. Each sysIO bank has its own I/O supply voltage (V_{CCO}) and reference voltage (V_{REF}) resources allowing each bank complete independence from the others. Each I/O is individually configurable based on the bank's V_{CCO} and V_{REF} settings. In addition, each I/O has configurable drive strength, weak pull-up, weak pull-down, or a bus-keeper latch. Table 4 lists the number of I/Os supported per bank in each of the ispXPGA devices.

Table 5 lists the sysIO standards with the typical values for V_{CCO}, V_{REF} and V_{TT}.

The TOE, JTAG TAP pins, PROGRAM, CFG0 and DONE pins of the ispXPGA device are the only pins that do not have the sysIO capabilities. The TOE and CFG0 pins operate off the V_{CC} of the device, supporting only the LVCMOS standard corresponding to the device supply voltage. The TAP pins have a separate supply voltage (V_{CCJ}), which determines the LVCMOS standard corresponding to that supply voltage.

There are three classes of I/O interface standards that are implemented in the ispXPGA devices. The first is the unterminated, single-ended interface. It includes the 3.3V LVTTL standard along with the 1.8V, 2.5V, and 3.3V LVCMOS interface standards. Additionally, PCI and AGP-1X are subsets of this type of interface.

The second type of interface implemented is the terminated, single-ended interface standard. This group of interfaces includes different versions of SSTL and HSTL interfaces along with CTT, and GTL+. Usage of these particular I/O interfaces requires an additional V_{REF} signal. At the system level a termination voltage, V_{TT}, is also required. Typically an output will be terminated to V_{TT} at the receiving end of the transmission line it is driving.

The third type of interface standards are the differential standards LVDS, BLVDS, and LVPECL. The differential standards require two I/O pins to create the differential pair. The logic level is determined by the difference in the two signals. Table 6 lists how these interface standards are implemented in the ispXPGA devices.

For more information on sysIO capability, refer to Lattice technical note number TN1000, *sysIO Usage Guidelines for Lattice Devices* available at www.latticesemi.com.

Figure 19. sysIO Banks per Device

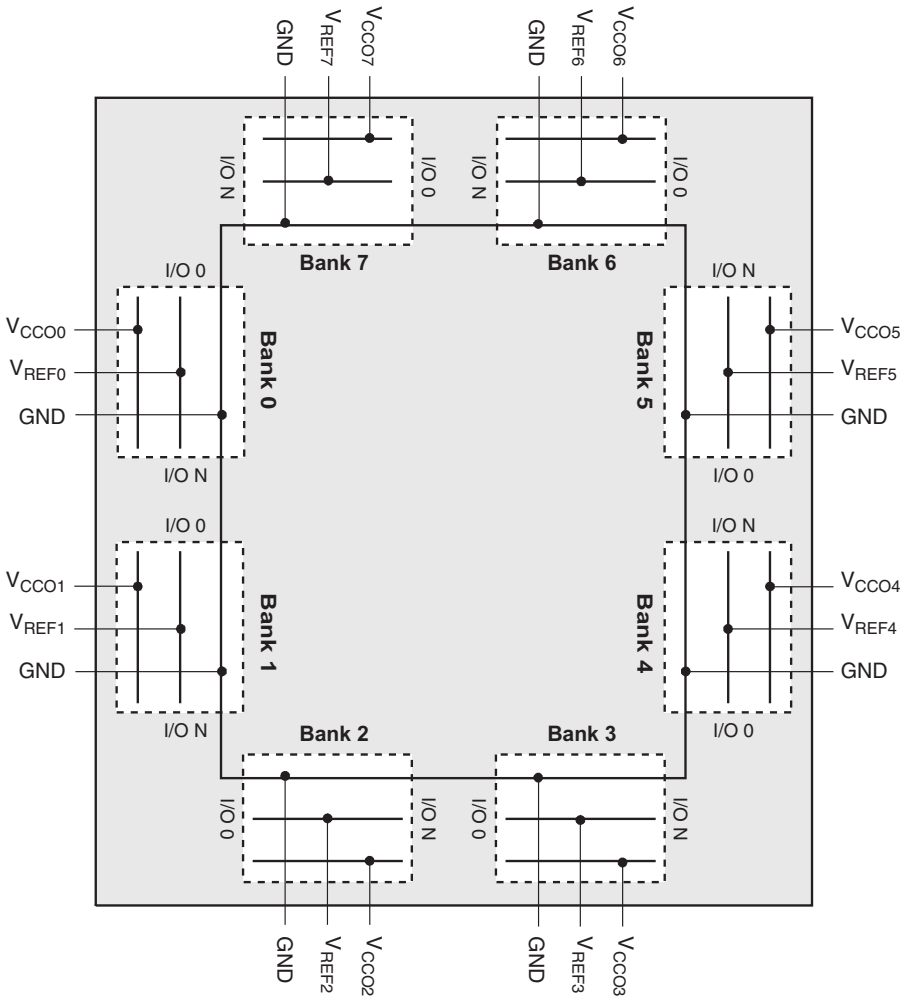


Table 4. Number of I/Os per Bank

Device	Max. Number of I/Os per Bank (N)
XPGA 1200	62
XPGA 500	42
XPGA 200	26
XPGA 125	22

Table 5. ispXPGA Supported I/O Standards

sysIO Standard	V_{CCO}	V_{REF}	V_{TT}
LVTTL	3.3V	N/A	N/A
LVCMOS-3.3	3.3V	N/A	N/A
LVCMOS-2.5	2.5V	N/A	N/A
LVCMOS-1.8	1.8V	N/A	N/A
PCI	3.3V	N/A	N/A
AGP-1X	3.3V	N/A	N/A
SSTL3, Class I, II	3.3V	1.5V	1.5V
SSTL2, Class I, II	2.5V	1.25V	1.25V
HSTL, Class I	1.5V	0.75V	0.75V
HSTL, Class III	1.5V	0.9V	1.5V
GTL+	N/A	1.0V	1.5V
LVPECL	3.3V	N/A	N/A
LVDS[1]	2.5V	N/A	N/A
BLVDS	2.5V	N/A	N/A

1. V_{CCO} must be 2.5V for high speed serial operations (sysHSI block).

Table 6. Differential Interface Standard Support[1]

		sysIO Buffer Not Using sysHSI Block	sysIO Buffer Using sysHSI Block
LVDS	Driver	Supported with external resistor network	Supported
	Receiver	Supported with standard termination	Supported with standard termination
BLVDS	Driver	Supported with external resistor network	Not supported
	Receiver	Supported (may need termination)	Supported (may need termination)
LVPECL	Driver	Supported with external resistor network	Not supported
	Receiver	Supported with termination	Supported with termination

1. For more information, refer to Lattice technical note TN1000, *sysIO Usage Guidelines,* available at www.latticesemi.com.

High Speed Serial Interface Block (sysHSI Block)

The High Speed Serial Interface (sysHSI) allows high speed serial data transfer over a pair of LVDS I/O. The ispXPGA devices have multiple sysHSI blocks.

Each sysHSI block has two SERDES blocks which contain two main sub-blocks, Transmitter (with a serializer) and Receiver (with a deserializer) including Clock/Data Recovery Circuit (CDR). Each SERDES can be used as a full duplex channel. The two SERDES in sysHSI blocks share a common clock and must operate at the same nominal frequency. Figure 20 shows the sysHSI block.

Device features support two data coding modes: 10B/12B and 8B/10B (for use with other encoding schemes, see Lattice's sysHSI technical notes). The encoding and decoding of the 10B/12B standard are performed within the sysHSI block. For the 8B/10B standard, the symbol boundaries are aligned internally but the encoding and decoding are performed outside the sysHSI block.

Each SERDES block receives a single high speed serial data input stream (with embedded clock) from an input, and provide a low speed 10-bit wide data stream and a recovered clock to the device. For transmitting, SERDES converts a 10-bit wide low-speed data stream to a single high-speed data stream with embedded clock for output.

Additionally, multiple sysHSI blocks can be grouped together to form a source synchronous interface of 1-10 channels.

Table 7 shows the clock sources available for the REFCLKs of the different sysHSI blocks. The Signal Description table in this data sheet provides the descriptions of the sysHSI block inputs and outputs.

For more information on the SERDES/CDR, refer to Lattice technical note number TN1020, *sysHSI Usage Guidelines*.

Figure 20. sysHSI Block Diagram

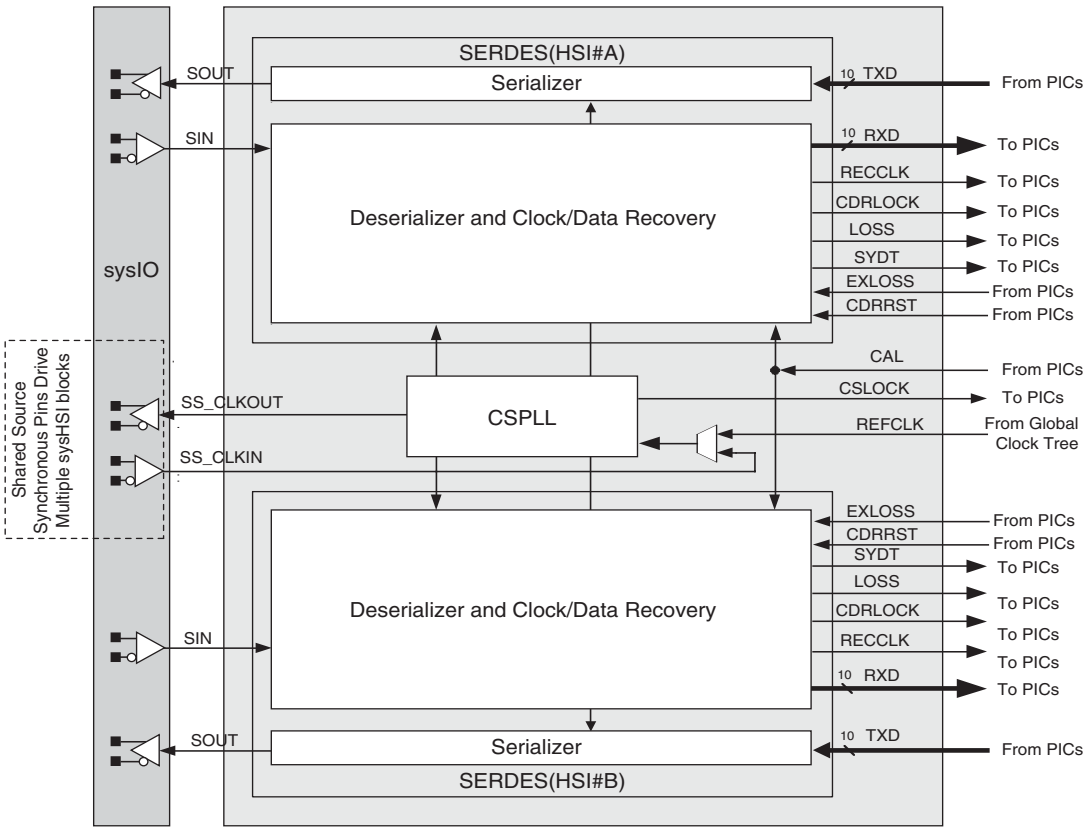


Table 7. sysHSI Block REFCLK Selections[1]

sysHSI Block	Available Global Clock Nets
0	CLK0, CLK1, CLK2, CLK3
1	CLK0, CLK1, CLK2, CLK4
2	CLK0, CLK1, CLK2, CLK5
3	CLK0, CLK1, CLK3, CLK6
4	CLK0, CLK1, CLK3, CLK7
5	CLK0, CLK3, CLK5, CLK7
6	CLK0, CLK2, CLK5, CLK7
7	CLK0, CLK1, CLK5, CLK6
8	CLK0, CLK5, CLK6
9	CLK0, CLK5, CLK6, CLK7

1. Table 6 applies to all devices. Ignore sysHSI blocks not available in a specific device.

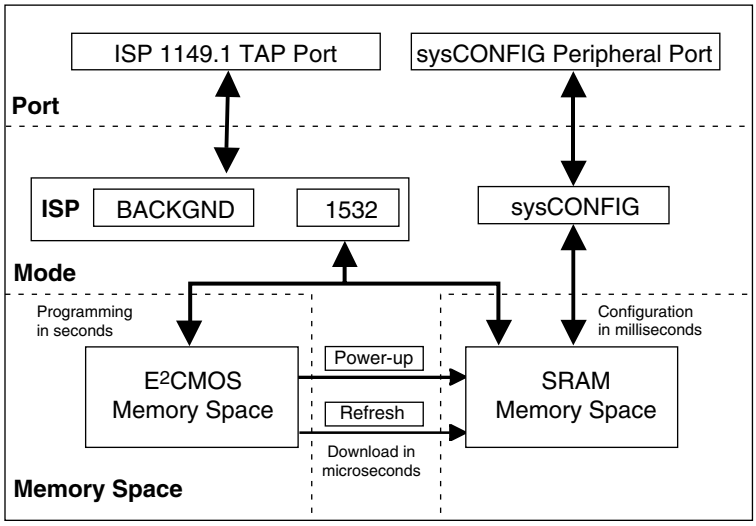
Configuration and Programming

The ispXPGA family of devices takes a unique approach to FPGA configuration memory. It contains two types of memory, Static RAM and non-volatile E^2CMOS cells. The static RAM is used to control the functionality of the device during normal operation and the E^2CMOS memory cells are used to load the SRAM. The E^2CMOS memory module can be thought of as the hard drive for the ispXPGA configuration and the SRAM as the working configuration memory. There is a one-to-one relationship between SRAM memory and the E^2CMOS cells. The SRAM can be configured either from the E^2CMOS memory or from an external source, as shown in Figure 21.

Figure 21 shows the different ports and modes that are used in the configuration and programming of the ispXPGA devices. There are two possible ports that can be used for configuration of the SRAM memory: the ISP port which is compliant to the IEEE 1149.1 Test Access Port (TAP) Std. and the ISP port which accommodates bit-wide configuration. The sysCONFIG port allows byte-wide configuration of the SRAM configuration memory. When programming the E^2CMOS memory, only the 1149.1 TAP can be used.

Configuration and programming done through the 1149.1 Test Access Port (TAP) are fully compliant to both the IEEE Std. 1149.1 Boundary Scan TAP specification and the IEEE Std. 1532 In-System Configuration specification. To configure or program the device using the 1149.1 TAP the device must be in the ISP mode. To configure the SRAM memory using the sysCONFIG Port, the device must be in the sysCONFIG mode. Upon power-up, the device's SRAM memory can be configured either from the E^2CMOS memory or from an external source through the sysCONFIG mode. Additionally, the SRAM can be re-configured from the E^2CMOS memory by executing a "REFRESH." See Lattice technical note number TN1026, *ispXP Configuration Usage Guide,* for more in depth information on the different programming modes, timing and wake-up, available at www.latticesemi.com.

Figure 21. ispXP Block Diagram



IEEE 1149.1-Compliant Boundary Scan Testability

All ispXPGA devices have boundary scan cells and are compliant with the IEEE 1149.1 standard. This allows functional testing of the circuit board on which the device is mounted through a serial scan path that can access all critical logic notes. Internal boundary scan registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test node data to be captured and shifted out for verification. In addition, these devices can be linked into a board-level serial scan path for more board level testing.

Security Scheme

A programmable security scheme is provided on the ispXPGA devices as a deterrent to unauthorized copying of the array configuration patterns. Once programmed, the security scheme prevents read-back of the programmed pattern by a device programmer, securing proprietary designs from competitors. The entire device must be erased in order to erase the security scheme.

Density Shifting

The ispXPGA family has been designed to ensure that different density devices in the same package have the same pin-out. Furthermore, the architecture ensures a high success rate when performing design migration from lower density parts to higher density parts. In many cases, it is possible to shift a lower utilization design targeted for a high-density device to a lower density device. However, the exact details of the final resource utilization will impact the likely success in each case.

Absolute Maximum Ratings[1, 2, 3]

	1.8V	2.5V/3.3V
Supply Voltage (V_{CC})	-0.5 to 2.5V	-0.5 to 5.5V
PLL Supply Voltage (V_{CCP})	-0.5 to 2.5V	-0.5 to 5.5V
Output Supply Voltage (V_{CCO})	-0.5 to 4.5V	-0.5 to 4.5V
IEEE 1149.1 TAP Supply Voltage (V_{CCJ})	-0.5 to 4.5V	-0.5 to 4.5V
Input Voltage Applied[4]	-0.5 to 4.5V	-0.5 to 4.5V
Storage Temperature	-65 to 150°C	-65 to 150°C
Junction Temperature (T_J) with Power Applied	-55 to 150°C	-55 to 150°C

1. Stress above those listed under the “Absolute Maximum Ratings” may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied (while programming, following the programming specifications).
2. Compliance with the Lattice Thermal Management technical note is required.
3. All voltages referenced to GND.
4. Overshoot and undershoot of -2V to (V_{IH} (MAX) + 2) volts is permitted for a duration of <20ns

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Units
V_{CC}	Supply Voltage for 1.8V device	1.65	1.95	V
	Supply Voltage for 2.5V device	2.3	2.7	V
	Supply Voltage for 3.3V device	3.0	3.6	V
V_{CCP}	Supply Voltage for PLL block for 1.8V device	1.65	1.95	V
	Supply Voltage for PLL block for 2.5V device	2.3	2.7	V
	Supply Voltage for PLL block for 3.3V device	3.0	3.6	V
V_{CCJ}	Supply Voltage for IEEE 1149.1 Test Access Port for LVCMOS 1.8V	1.65	1.95	V
	Supply Voltage for IEEE 1149.1 Test Access Port for LVCMOS 2.5V	2.3	2.7	V
	Supply Voltage for IEEE 1149.1 Test Access Port for LVCMOS 3.3V	3.0	3.6	V
T_J (COM)	Junction Temperature Commercial Operation	0	85	C
T_J (IND)	Junction Temperature Industrial Operation	-40	105	C

E²CMOS Erase Reprogram Specifications

Parameter	Min	Max	Units
Erase/Reprogram Cycle[1]	1,000	—	Cycles

1. Valid over commercial temperature range.

Hot Socketing Characteristics[1, 2, 3, 4]

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{DK}	Input or I/O Leakage Current	$0 \le V_{IN} \le 3.0V$	—	+/-50	+/-800	µA

1. Insensitive to sequence of V_{CC} and V_{CCO}. However, assumes monotonic rise / fall rates for V_{CC} and V_{CCO}.
2. LVTTL, LVCMOS only
3. $0 < V_{CC} \le V_{CC}$ (MAX), $0 < V_{CCO} \le V_{CCO}$ (MAX)
4. I_{DK} is additive to I_{PU}, I_{PD} or I_{BH}. Device defaults to pull-up until fuse circuitry is active.

DC Electrical Characteristics

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{IL}, I_{IH}[1]	Input or I/O Low Leakage	$0 \le V_{IN} < (V_{CCO} - 0.2V)$	—	—	10	µA
		$(V_{CCO} - 0.2V) \le V_{IN} \le 3.6V$	—	—	40	µA
I_{PU}	I/O Active Pull-up Current	$0 \le V_{IN} \le 0.7\ V_{CCO}$	30	—	150	µA
I_{PD}	I/O Active Pull-down Current	V_{IL} (MAX) $\le V_{IN} \le V_{IH}$ (MAX)	30	—	150	µA
I_{BHLS}	Bus Hold Low Sustaining Current	$V_{IN} = V_{IL}$ (MAX)	30	—	—	µA
I_{BHHS}	Bus Hold High Sustaining Current	$V_{IN} = 0.7\ V_{CCO}$	30	—	—	µA
I_{BHLO}	Bus Hold Low Overdrive Current	$0 \le V_{IN} \le V_{IH}$ (MAX)	—	—	150	µA
I_{BHHO}	Bus Hold High Overdrive Current	$0 \le V_{IN} \le V_{IH}$ (MAX)	—	—	150	µA
V_{BHT}	Bus Hold Trip Points		V_{CCO} * 0.35	—	V_{CCO} * 0.65	V
C_1	I/O Capacitance[2]	V_{CCO} = 3.3V, 2.5V, 1.8V	—	8	—	pf
		V_{CC} = 1.8V, V_{IO} = 0 to V_{IH} (MAX)	—		—	
C_2	Clock Capacitance[2]	V_{CCO} = 3.3V, 2.5V, 1.8V	—	6	—	pf
		V_{CC} = 1.8V, V_{IO} = 0 to V_{IH} (MAX)	—		—	
C_3	Global Input Capacitance[2]	V_{CCO} = 3.3V, 2.5V, 1.8V	—	6	—	pf
		V_{CC} = 1.8V, V_{IO} = 0 to V_{IH} (MAX)	—		—	

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tri-stated. It is not measured with the output driver active. Bus maintenance circuits are disabled.
2. T_A = 25°C, f = 1.0MHz.

Supply Current

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{CC}[1, 2]	Standby Core Operating Power Supply Current	V_{CC} = 3.3V	—	220	—	mA
		V_{CC} = 2.5V	—	220	—	mA
		V_{CC} = 1.8V	—	200	—	mA
I_{CCO}[3]	Standby Output Power Supply Current	V_{CCO} = 3.3V	—	2.0	—	mA
		V_{CCO} = 2.5V	—	2.0	—	mA
		V_{CCO} = 1.8V	—	2.0	—	mA
		V_{CCO} = 1.5V	—	2.0	—	mA
I_{CCP}[4]	Standby PLL Operating Supply Current	V_{CCP} = 3.3V	—	17.0	—	mA
		V_{CCP} = 2.5V	—	17.0	—	mA
		V_{CCP} = 1.8V	—	15.0	—	mA
I_{CCJ}[5]	Standby IEEE 1149.1 TAP Power Supply Current	V_{CCJ} = 3.3V	—	2.0	—	mA
		V_{CCJ} = 2.5V	—	1.5	—	mA
		V_{CCJ} = 1.8V	—	1.0	—	mA

1. T_A = 25˚C, frequency = 1.0 MHz, device configured with 16-bit counters.
2. I_{CC} varies with specific device configuration and operating frequency. For more accurate power calculation use the ispXPGA Power Estimator.
3. T_A = 25˚C, per bank, no DC load, frequency = 0 MHz.
4. T_A = 25˚C, per PLL, frequency = 10 MHz.
5. T_A = 25˚C

sysIO Recommended Operating Conditions

Standard	V_{CCO} (V)[1]			V_{REF} (V)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
LVCMOS 3.3	3.0	3.3	3.6	-	-	-
LVCMOS 2.5	2.3	2.5	2.7	-	-	-
LVCMOS 1.8[2]	1.65	1.8	1.95	-	-	-
LVTTL	3.0	3.3	3.6	-	-	-
PCI 3.3	3.0	3.3	3.6	-	-	-
AGP-1X	3.15	3.3	3.45	-	-	-
SSTL 2	2.3	2.5	2.7	1.15	1.25	1.35
SSTL 3	3.0	3.3	3.6	1.3	1.5	1.7
CTT 3.3	3.0	3.3	3.6	1.35	1.5	1.65
CTT 2.5	2.3	2.5	2.7	1.35	1.5	1.65
HSTL Class I	1.4	1.5	1.6	0.68	0.75	0.9
HSTL Class III	1.4	1.5	1.6	-	0.9	-
GTL+	-	-	-	0.882	1.0	1.122
LVDS	2.3	2.5	2.7	-	-	-
LVPECL	3.0	3.3	3.6	-	-	-
BLVDS	2.3	2.5	2.7	-	-	-

1. Inputs independent of V_{CCO}.
2. Design tool default setting.

sysIO DC Electrical Characteristics

Over Recommended Operating Conditions

Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL} (mA)	I_{OH} (mA)
	Min. (V)	Max. (V)	Min. (V)	Max. (V)	Max. (V)	Min. (V)		
LVCMOS 3.3	-0.3	0.8	2.0	3.6	0.4	V_{CCO} - 0.4	20, 16, 12, 8, 5.33, 4	-20, -16,-12, -8, -5.33, -4
					0.2	V_{CCO} - 0.2	0.1	-0.1
LVCMOS 2.5	-0.3	0.7	1.7	3.6	0.4	V_{CCO} - 0.4	16, 12, 8, 5.33, 4	-16, -12, -8, -5.33, -4
					0.2	V_{CCO} - 0.2	0.1	-0.1
LVCMOS 1.8[1]	-0.3	0.68[3]	1.07[3]	3.6	0.4	V_{CCO} - 0.4	12, 8[1], 5.33, 4	-12, -8[1], -5.33, -4
		$0.35V_{CC}$	$0.65V_{CC}$		0.2	V_{CCO} - 0.2	0.1	-0.1
LVTTL	-0.3	0.8	2.0	3.6	0.4	V_{CCO} - 0.4	20, 16, 12, 8, 5.33, 4	-20, -16,-12, -8, -5.33, -4
					0.2	V_{CCO} - 0.2	0.1	-0.1
PCI 3.3	-0.3	1.08[3]	1.5[3]	3.6	0.1 V_{CCO}	0.9 V_{CCO}	1.5	-0.5
		$0.3V_{CCO}$	0.5 V_{CCO}					
AGP-1X	-0.3	1.08[3]	1.5[3]	3.6	0.1 V_{CCO}	0.9 V_{CCO}	1.5	-0.5
		0.3 V_{CCO}	0.5 V_{CCO}					
SSTL 3 Class I	-0.3	V_{REF} - 0.2	V_{REF} + 0.2	3.6	0.7	V_{CCO} - 1.1	8	-8
SSTL 3 Class II	-0.3	V_{REF} - 0.2	V_{REF} + 0.2	3.6	0.5	V_{CCO} - 0.9	16	-16
SSTL 2 Class I	-0.3	V_{REF} - 0.18	V_{REF} + 0.18	3.6	0.54	V_{CCO} - 0.62	7.6	-7.6
SSTL 2 Class II	-0.3	V_{REF} - 0.18	V_{REF} + 0.18	3.6	0.35	V_{CCO} - 0.43	15.2	-15.2
CTT 3.3	-0.3	V_{REF} - 0.2	V_{REF} + 0.2	3.6	V_{REF} - 0.4	V_{REF} + 0.4	8	-8
CTT 2.5	-0.3	V_{REF} - 0.2	V_{REF} + 0.2	3.6	V_{REF} - 0.4	V_{REF} + 0.4	8	-8
HSTL Class I	-0.3	V_{REF} - 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCO} - 0.4	8	-8
HSTL Class III	-0.3	V_{REF} - 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCO} - 0.4	24	-8
GTL+	-0.3	V_{REF} - 0.2	V_{REF} + 0.2	3.6	0.6	N/A	36	N/A

1. Design tool default setting.
2. The average DC current drawn by I/Os between adjacent bank GND connections, or between the last GND in an I/O bank and the end of the I/O bank, as shown in the logic signals connection table, shall not exceed n*8mA. Where n is the number of I/Os between bank GND connections or between the last GND in a bank and the end of a bank
3. Applicable for ispXPGA V/B devices.

sysIO Differential Standards DC Electrical Characteristics

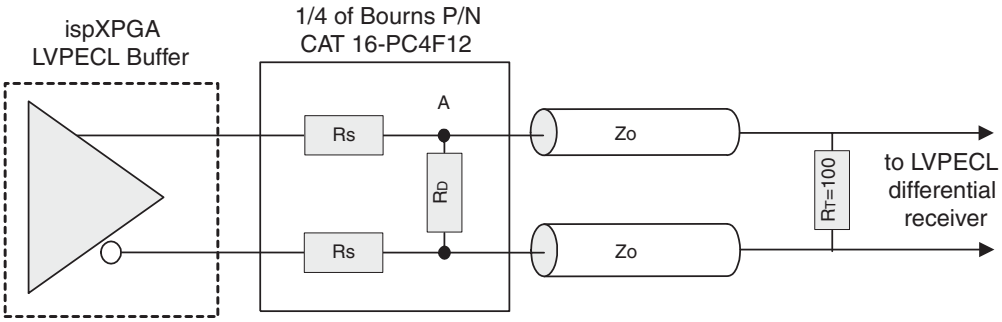
Parameter	Description	Test Conditions	Min.	Typ.	Max.
LVDS[1]					
V_{INP}, V_{INM}	Input voltage		0V	—	2.4V
V_{THD}	Differential input threshold		+/-100mV	—	—
V_{CM}	Input Common Mode voltage	Half the sum of the two inputs	0.05V	—	2.35V
I_{IN}	Input current	Power on or Power off	—	—	+/-10uA
V_{OH}	Output High Voltage for V_{OP} or V_{OM}	RT = 100 Ohm	—	1.38V	1.60V
V_{OL}	Output Low Voltage for V_{OP} or V_{OM}	RT = 100 Ohm	0.9V	1.03V	—
V_{OD}	Output Voltage Differential	$\|V_{OP} - V_{OM}\|$, R_T = 100 ohm	250mV	350mV	450mV
ΔV_{OD}	Change in V_{OD} between high and low		—	—	50mV
V_{OS}	Output Voltage Offset	$\|V_{OP} + V_{OM}\|/2$, R_T = 100 ohm	1.125V	1.25V	1.375V
ΔV_{OS}	Change in V_{OS} between H and L		—	—	50mV
I_{OSD}	Output short circuit current	V_{OD} = 0V Driver outputs shorted	—	—	24mA
BLVDS[1]					
V_{INP}, V_{INM}	Input voltage		0V	—	2.4V
V_{THD}	Differential input threshold		+/-100mV	—	—
V_{CM}	Input Common Mode voltage	Half the sum of the two inputs	0.05V	—	2.35V
I_{IN}	Input current	Power on or Power off	—	—	+/-10uA
V_{OH}	Output High Voltage for V_{OP} or V_{OM}	R_T = 27Ω	—	1.4V	1.80V
V_{OL}	Output Low Voltage for V_{OP} or V_{OM}	R_T = 27Ω	0.95V	1.1V	—
V_{OD}	Output Voltage Differential	$\|V_{OP} - V_{OM}\|$, RT = 27Ω	240mV	300mV	460mV
ΔV_{OD}	Change in V_{OD} Between H and L				27mV
V_{OS}	Output Voltage Offset	$\|V_{OP} + V_{OM}\|$ /2, RT = 27Ω	1.1V	1.3V	1.5V
ΔV_{OS}	Change in V_{OS} Between H and L				27mV
I_{OSD}	Output Short Circuit Current	V_{OD} = 0. Driver Outputs Shorted.		36mA	65mA

1. V_{OP} and V_{OM} are the two outputs of the LVDS/BLVDS output buffer.

LVPECL[1]								
DC Parameter	**Parameter Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
V_{CCO}		**3.0**		**3.3**		**3.6**		**V**
V_{IH}	Input Voltage High	1.49	2.72	1.49	2.72	1.49	2.72	V
V_{IL}	Input Voltage Low	0.86	2.125	0.86	2.125	0.86	2.125	V
V_{OH}	Output Voltage High	1.8	2.11	1.92	2.28	2.13	2.41	V
V_{OL}	Output Voltage Low	0.96	1.27	1.06	1.43	1.3	1.57	V
V_{DIFF}	Differential Input voltage	0.3	—	0.3	—	0.3	—	V

1. These values are valid at the output of the source termination pack as shown above with 100-ohm differential load only (see Figure 22). The V_{OH} levels are 200mV below the standard LVPECL levels and are compatible with devices tolerant of the lower common mode ranges.

Figure 22. LVPECL Driver with Three Resistor Pack



ispXPGA External Switching Characteristics

Over Recommended Operating Conditions

Parameter	Description	Conditions	-4		-3		Units
			Min.	Max.	Min.	Max.	
t_{CO}	Global Clock Input to Output	PIO Output Register	—	7.1	—	8.2	ns
t_{S}	Global Clock Input Setup	PIO Input Register without input delay	-2.7	—	-2.3	—	ns
t_{H}	Global Clock Input Hold	PIO Input Register without input delay	4.6	—	5.3	—	ns
t_{SINDLY}	Global Clock Input Setup	PIO Input Register with input delay	3.8	—	4.4	—	ns
t_{HINDLY}	Global Clock Input Hold	PIO Input Register with input delay	0.0	—	0.0	—	
t_{COPLL}	Global Clock Input to Output	PIO Output Register using PLL without delay	—	3.3	—	3.8	ns
t_{SPLL}	Global Clock Input Setup	PIO Input Register without input delay using PLL without delay	1.1	—	1.3	—	ns
t_{HPLL}	Global Clock Input Hold	PIO Input Register without input delay using PLL without delay	0.8	—	1.0	—	ns
$t_{SINDLYPLL}$	Global Clock Input Setup	PIO Input Register with input delay using PLL without delay	7.6	—	8.8	—	ns
$t_{HINDLYPLL}$	Global Clock Input Hold	PIO Input Register with input delay using PLL without delay	-4.6	—	-4.0	—	ns

ispXPGA PFU Timing Parameters

Over Recommended Operating Conditions

Parameter	Description	-4		-3		Units
		Min.	Max.	Min.	Max.	
Functional Delays						
LUTs						
t_{LUT4}	4-Input LUT Delay	—	0.44	—	0.51	ns
t_{LUT5}	5-Input LUT Delay	—	0.79	—	0.91	ns
t_{LUT6}	6-Input LUT Delay	—	0.93	—	1.07	ns
Shift Register (LUT)						
t_{LSR_S}	Shift Register Setup Time	-0.62	—	-0.53	—	ns
t_{LSR_H}	Shift Register Hold Time	0.63	—	0.72	—	ns
t_{LSR_CO}	Shift Register Clock to Output Delay	—	0.75	—	0.86	ns
Arithmetic Functions						
$t_{LCTHRUR}$	MC (Macro Cell) Carry In to MC Carry Out Delay (Ripple)	—	0.09	—	0.10	ns
$t_{LCTHRUL}$[1]	MC Carry In to MC Carry Out Delay (Look Ahead)	—	0.05	—	0.06	ns
t_{LSTHRU}	MC Sum In to MC Sum Out Delay	—	0.45	—	0.52	ns
$t_{LSINCOUT}$	MC Sum In to MC Carry Out Delay	—	0.31	—	0.36	ns
$t_{LCINSOUTR}$	MC Carry In to MC Sum Out Delay (Ripple)	—	0.39	—	0.45	ns
$t_{LCINSOUTL}$	MC Carry In to MC Sum Out Delay (Look Ahead)	—	0.28	—	0.32	ns
Feed-thru						
t_{LFT}	PFU Feed-Thru Delay	—	0.16	—	0.18	ns
Distributed RAM						
t_{LRAM_CO}	Clock to RAM Output	—	1.33	—	1.53	ns
t_{LRAMAD_S}	Address Setup Time	-0.40	—	-0.34	—	ns
t_{LRAMD_S}	Data Setup Time	0.22	—	0.25	—	ns
t_{LRAMWE_S}	Write Enable Setup Time	0.46	—	0.53	—	ns
t_{LRAMAD_H}	Address Hold Time	0.60	—	0.69	—	ns
t_{LRAMD_H}	Data Hold Time	0.11	—	0.13	—	ns
t_{LRAMWE_H}	Write Enable Hold Time	0.12	—	0.14	—	ns
$t_{LRAMCPW}$	Clock Pulse Width (High or Low)	3.00	—	3.45	—	ns
$t_{LRAMADO}$	Address to Output Delay	—	0.93	—	1.07	ns
Register/Latch Delays						
Registers						
t_{L_CO}	Register Clock to Output Delay	—	0.62	—	0.71	ns
t_{L_S}	Register Setup Time (Data before Clock)	0.14	—	0.16	—	ns
t_{L_H}	Register Hold Time (Data after Clock)	-0.12	—	-0.10	—	ns
t_{LCE_S}	Register Clock Enable Setup Time	-0.11	—	-0.09	—	ns
t_{LCE_H}	Register Clock Enable Hold Time	0.11	—	0.13	—	ns
Latches						
t_{L_GO}	Latch Gate to Output Delay	—	0.10	—	0.12	ns
t_{LL_S}	Latch Setup Time	0.14	—	0.16	—	ns
t_{LL_H}	Latch Hold Time	-0.12	—	-0.10	—	ns
t_{LLPD}	Latch Propagation Delay (Transparent Mode)	—	0.10	—	0.12	ns

ispXPGA PFU Timing Parameters (Continued)

Over Recommended Operating Conditions

Parameter	Description	-4		-3		Units
		Min.	Max.	Min.	Max.	
Reset/Set						
t_{LASSRO}	Asynchronous Set/Reset to Output	—	1.17	—	1.35	ns
$t_{LASSRPW}$	Asynchronous Set/Reset Pulse Width	—	4.50	—	5.18	ns
t_{LASSRR}	Asynchronous Set/Reset Recovery	—	0.55	—	0.63	ns
t_{LSSR_S}	Synchronous Set/Reset Setup Time	-0.03	—	-0.03	—	ns
t_{LSSR_H}	Synchronous Set/Reset Hold Time	0.03	—	0.03	—	ns

1. $t_{LCTHRUL}$ quoted bit by bit.

Timing v.2.0

ispXPGA PIC Timing Parameters

Parameter	Description	-4		-3		Units
		Min.	Max.	Min.	Max.	
Register/Latch Delays						
t_{IO_CO}	Register Clock to Output Delay	—	1.09	—	1.25	ns
t_{IO_S}	Register Setup Time (Data before Clock)	0.05	—	0.06	—	ns
t_{IO_H}	Register Hold Time (Data after Clock)	0.06	—	0.07	—	ns
t_{IOCE_S}	Register Clock Enable Setup Time	-0.03	—	-0.03	—	ns
t_{IOCE_H}	Register Clock Enable Hold Time	0.13	—	0.15	—	ns
t_{IO_GO}	Latch Gate to Output Delay	—	0.91	—	1.05	ns
t_{IOL_S}	Latch Setup Time	0.05	—	0.06	—	ns
t_{IOL_H}	Latch Hold Time	0.06	—	0.07	—	ns
t_{IOLPD}	Latch Propagation Delay (Transparent Mode)	—	0.10	—	0.12	ns
t_{IOASRO}	Asynchronous Set/Reset to Output	—	1.26	—	1.45	ns
$t_{IOASRPW}$	Asynchronous Set/Reset Pulse Width	—	4.50	—	5.18	ns
t_{IOASRR}	Asynchronous Set/Reset Recovery Time	—	0.25	—	0.29	ns
Input/Output Delays						
t_{IOBUF}	Output Buffer Delay	—	1.06	—	1.22	ns
t_{IOIN}	Input Buffer Delay	—	0.76	—	0.87	ns
t_{IOEN}	Output Enable Delay	—	0.56	—	0.64	ns
t_{IODIS}	Output Disable Delay	—	-0.10	—	-0.09	ns
t_{IOFT}	Feed-thru Delay	—	0.20	—	0.23	ns

Timing v.2.0

ispXPGA EBR Timing Parameters

Parameter	Description	-4		-3		Units
		Min.	Max.	Min.	Max.	
Synchronous Write						
t_{EBSWAD_S}	Address Setup Delay	0.61	—	0.70	—	ns
t_{EBSWAD_H}	Address Hold Delay	-0.39	—	-0.33	—	ns
$t_{EBSWCPW}$	Clock Pulse Width	—	3.40	—	3.91	ns
t_{EBSWWE_S}	Write Enable Setup Time	-0.12	—	-0.10	—	ns
t_{EBSWWE_H}	Write Enable Hold Time	0.16	—	0.18	—	ns
t_{EBSWD_S}	Data Setup Time	0.28	—	0.32	—	ns
t_{EBSWD_H}	Data Hold Time	-0.26	—	-0.22	—	ns
Synchronous Read						
t_{EBSR_CO}	Clock to Data Delay	—	2.19	—	2.52	ns
t_{EBSRAD_S}	Address Setup Delay	0.10	—	0.12	—	ns
t_{EBSRAD_H}	Address Hold Delay	-0.07	—	-0.06	—	ns
$t_{EBSRCPW}$	Clock Pulse Width	—	3.40	—	3.91	ns
t_{EBSRCE_S}	Clock Enable Setup Time	-1.71	—	-1.45	—	ns
t_{EBSRCE_H}	Clock Enable Hold Time	1.69	—	1.94	—	ns
t_{EBSRWE_S}	Write Enable Setup Time	-0.17	—	-0.14	—	ns
t_{EBSRWE_H}	Write Enable Hold Time	0.12	—	0.14	—	ns
$t_{EBSRWEEN}$	Write Enable to Data Enable Time	—	1.05	—	1.21	ns
$t_{EBSRWEDIS}$	Write Enable to Data Disable Time	—	1.02	—	1.17	ns
t_{EBSREN}	Output Enable to Data Enable Time	—	1.05	—	1.21	ns
$t_{EBSRDIS}$	Output Enable to Data Disable Time	—	0.86	—	0.99	ns
Asynchronous Read						
$t_{EBARADO}$	Address to New Valid Data Delay	—	2.46	—	2.83	ns
t_{EBARAD_H}	Address to Previous Valid Data Delay	—	2.17	—	2.50	ns
$t_{EBARWEEN}$	Write Enable to Data Enable Time	—	1.04	—	1.20	ns
$t_{EBARWEDIS}$	Write Enable to Data Disable Time	—	1.01	—	1.16	ns
t_{EBAREN}	Output Enable to Data Enable Time	—	1.05	—	1.21	ns
$t_{EBARDIS}$	Output Enable to Data Disable Time	—	0.86	—	0.99	ns

Timing v.2.0

ispXPGA Family Timing Adders

Parameter	Description	Base Parameter	-4		-3		Units
			Min.	Max.	Min.	Max.	
Optional Adders							
t_{INDIO}	Input Delay	—	—	6.0	—	6.9	ns
t_{IOI} Input Adjusters							
LVTTL_in	Using 3.3V TTL	t_{IOIN}	—	0.5	—	0.5	ns
LVCMOS_18_in	Using 1.8V CMOS	t_{IOIN}	—	0.0	—	0.0	ns
LVCMOS_25_in	Using 2.5V CMOS	t_{IOIN}	—	0.3	—	0.3	ns
LVCMOS_33_in	Using 3.3V CMOS	t_{IOIN}	—	0.5	—	0.5	ns
AGP_1X_in	Using AGP 1x	t_{IOIN}	—	1.0	—	1.0	ns
CTT25_in	Using CTT 2.5V	t_{IOIN}	—	1.0	—	1.0	ns
CTT33_in	Using CTT 3.3V	t_{IOIN}	—	1.0	—	1.0	ns
GTL+_in	Using GTL+	t_{IOIN}	—	0.5	—	0.5	ns
HSTL_I_in	Using HSTL 2.5V, Class I	t_{IOIN}	—	0.5	—	0.5	ns
HSTL_III_in	Using HSTL 2.5V, Class III	t_{IOIN}	—	0.5	—	0.5	ns
LVDS_in	Using Low Voltage Differential Signaling (LVDS)	t_{IOIN}	—	0.8	—	0.8	ns
BLVDS_in	Using Bus Low Voltage Differential Signaling (BLVDS)	t_{IOIN}	—	0.8	—	0.8	ns
LVPECL_in	Using Low Voltage PECL	t_{IOIN}	—	0.8	—	0.8	ns
PCI_in	Using PCI	t_{IOIN}	—	1.0	—	1.0	ns
SSTL2_I_in	Using SSTL 2.5V, Class I	t_{IOIN}	—	0.8	—	0.8	ns
SSTL2_II_in	Using SSTL 2.5V, Class II	t_{IOIN}	—	0.5	—	0.5	ns
SSTL3_I_in	Using SSTL 3.3V, Class I	t_{IOIN}	—	0.8	—	0.8	ns
SSTL3_II_in	Using SSTL 3.3V, Class II	t_{IOIN}	—	0.8	—	0.8	ns
t_{IOO} Output Adjusters							
Slow Slew	Using Slow Slew (LVTTL and LVCMOS Outputs only)	t_{IOBUF}, t_{IOEN}	—	0.7	—	0.7	ns
LVTTL_out	Using 3.3V TTL Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	1.0	—	1.0	ns
LVCMOS_18_4mA_out	Using 1.8V CMOS Standard, 4mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.8	—	0.8	ns
LVCMOS_18_5.33mA_out	Using 1.8V CMOS Standard, 5.33mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.6	—	0.6	ns
LVCMOS_18_8mA_out	Using 1.8V CMOS Standard, 8mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.0	—	0.0	ns
LVCMOS_18_12mA_out	Using 1.8V CMOS Standard, 12mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.2	—	0.2	ns
LVCMOS_25_4mA_out	Using 2.5V CMOS Standard, 4mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.7	—	0.7	ns
LVCMOS_25_5.33mA_out	Using 2.5V CMOS Standard, 5.33 mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	ns
LVCMOS_25_8mA_out	Using 2.5V CMOS Standard, 8mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	ns
LVCMOS_25_12mA_out	Using 2.5V CMOS Standard, 12mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	ns
LVCMOS_25_16mA_out	Using 2.5V CMOS Standard, 16mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	ns

ispXPGA Family Timing Adders (Continued)

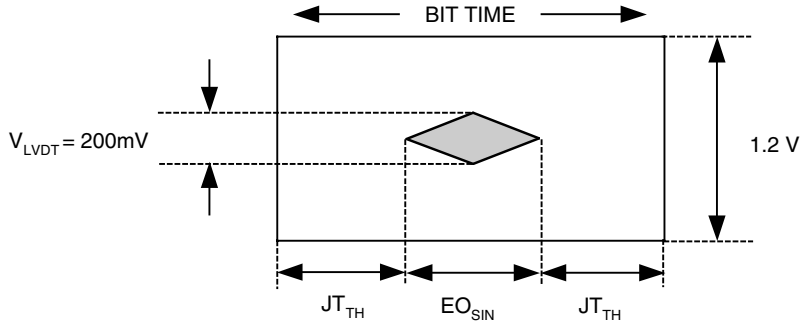
Parameter	Description	Base Parameter	-4		-3		Units
			Min.	Max.	Min.	Max.	
LVCMOS_33_4mA_out	Using 3.3V CMOS Standard, 4mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	1.0	—	1.0	ns
LVCMOS_33_5.33mA_out	Using 3.3V CMOS Standard, 5.33mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	1.0	—	1.0	ns
LVCMOS_33_8mA_out	Using 3.3V CMOS Standard, 8mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.7	—	0.7	ns
LVCMOS_33_12mA_out	Using 3.3V CMOS Standard, 12mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	ns
LVCMOS_33_16mA_out	Using 3.3V CMOS Standard, 16mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	ns
LVCMOS_33_24mA_out	Using 3.3V CMOS Standard, 24mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	ns
AGP_1X_out	Using AGP 1x Standard	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	ns
CTT25_out	Using CTT 2.5V	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	ns
CTT33_out	Using CTT 3.3V	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	ns
GTL+_out	Using GTL+	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	ns
HSTL_I_out	Using HSTL 2.5V, Class I	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	ns
HSTL_III_out	Using HSTL 2.5V, Class III	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	ns
LVDS_out	Using Low Voltage Differential Signaling (LVDS)	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	1.0	—	1.0	ns
BLVDS_out	Using Bus Low Voltage Differential Signaling (BLVDS)	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	1.0	—	1.0	ns
LVPECL_out	Using Low Voltage PECL	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	1.0	—	1.0	ns
PCI_out	Using PCI Standard	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	ns
SSTL2_I_out	Using SSTL 2.5V, Class I	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	ns
SSTL2_II_out	Using SSTL 2.5V, Class II	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	ns
SSTL3_I_out	Using SSTL 3.3V, Class I	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	ns
SSTL3_II_out	Using SSTL 3.3V, Class II	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	ns

Timing v.2.0

sysHSI Block Timing

Figure 23 provides a graphical representation of the SERDES receiver input requirements. It provides guidance on a number of input parameters, including signal amplitude and rise time limits, noise and jitter limits, and P and N input skew tolerance.

Figure 23. Receive Data Eye Diagram Template (Differential)



JT_{TH} : Optimum Threshold Crossing Jitter

The data pattern eye opening at the receive end of a link is considered the ultimate measure of received signal quality. Almost all detrimental characteristics of a transmit signal and the interconnection link design result in eye closure. This combined with the eye-opening limitations of the line receiver can provide a good indication of a link's ability to transfer error-free data.

Signal jitter is of special interest to system designers. It is often the primary limiting characteristic of long digital links and of systems with high noise level environments. An interesting characteristics of the clock and data recovery (CDR) portion of the ispXPGA SERDES receiver is its ability to filter incoming signal jitter that is below the clock recovery PLL bandwidth. For signals with high levels of low frequency jitter, the receiver can detect incoming data error free, with eye openings significantly less than that shown in Figure 23.

sysHSI Block AC Specifications

Operating Frequency Ranges

Symbol	Description	Mode	Test Condition	Min	Max	Unit
f_{CLK}	REFCLK, SS_CLKIN, SS_CLKOUT	All		40	250	MHz
f_{SIN}	Serial Input	SS: no CAL	with eo_{SIN}	400	750[1]	Mbps
		SS: CAL	with eo_{SIN}	400	800[1]	Mbps
		10B12B	with eo_{SIN}	400	850[1]	Mbps
		8B10B	with eo_{SIN}	400	850[1]	Mbps
f_{SOUT}	Serial Out	LVDS	C_L=5 pF, R_L=100 Ohm	400	850	Mbps

1. These max. numbers apply to the -4 speed grade only. For the -3 speed grade, the corresponding numbers are:
   SS: no CAL 650
   SS: CAL 700
   10B12B 800
   8B10B 800

LOCKIN Time

Symbol	Description	Mode	Condition	Min.	Max.	Units
t_{SCLOCK}	CSPLL Lock Time	All	After Input is Stabilized	—	25	µS
$t_{CDRLOCK}$	CDRPLL Lock-in Time	SS	With SS mode Sync Pattern	—	1024	t_{RCP}[1]
		10B12B	With 10B12B Sync Pattern	—	1024	t_{RCP}
		8B10B	With 8B10B Idle Pattern	—	480	t_{RCP}
t_{SYNC}	SyncPat Length	SS		1200	—	t_{RCP}
t_{CAL}	CAL Duration	SS		1100	—	t_{RCP}
t_{SUSYNC}	SyncPat Set-up Time to CAL	SS		50	—	t_{RCP}
t_{HDSYNC}	SyncPat Hold Time from CAL	SS		50	—	t_{RCP}

1. REFCLK clock period.

REFCLK and SS_CLKIN Timing

Symbol	Description	Mode	Condition	Min.	Max.	Units
$f_{DREFCLK}$	Frequency Deviation Between TX REFCLK and CDRX REFCLK on one link.	8B10B, 10B12B		-100	100	ppm
$t_{JPPREFCLK}$	REFCLK, SS_CLKIN Peak-to-Peak Period Jitter	All	40-250 (MHz)	-0.005	0.005	UIPP
$t_{PWREFCLK}$	REFCLK, SS_CLKIN Pulse Width, (80% to 80% or 20% to 20%).	All		1	—	ns
$t_{RFREFCLK}$	REFCLK, SS_CLKIN Rise/Fall Time. (20% to 80% or 80% to 20%)	All		—	2	ns

SERIALIZER Timing[1]

Symbol	Description	Mode	Condition	Min.	Max.	Units
$t_{JPPSOUT}$	SOUT Peak-to-Peak Output Data Jitter	All		—	0.25	UIPP
$t_{JPP8B10B}$	SOUT Peak-to-Peak Random Jitter	8B10B	900 Mbps w/k28.7-	—	130	ps
	SOUT Peak-to-Peak Deterministic Jitter	8B10B	900 Mbps w/k28.5+	—	110	ps
t_{RFSOUT}	SOUT Output Data Rise/Fall Time (20%, 80%)	LVDS		—	700	ps
		BLVDS		—	900	ps
t_{COSOUT}	REFCLK to SOUT Delay	SS/8B10B		$2Bt^2 + 2$	$2Bt^2 + 10$	ns
		10B12B		$1Bt^2 + 2$	$1Bt^2 + 10$	ns
t_{SKTX}	Skew of SOUT with Respect to SS_CLKOUT	SS		—	250	ps
$t_{CKOSOUT}$	SS_CLKOUT to bit0 of SOUT	SS		$2Bt^2 + t_{SKTX}$	$2Bt^2 + t_{SKTX}$	ns
$t_{HSITXDDATAS}$	TXD Data Setup Time	All	Note 3	1.5	—	ns
$t_{HSITXDDATAH}$	TXD Data Hold Time	All	Note 3	—	1.0	ns

1. The SIN and SOUT jitter specifications listed above are under the condition that the clock tree that drives the REFCLK to sysHSI Block is in sysCLOCK PLL BYPASS mode.
2. Bt = bit time period. High speed serial bit time.
3. Internal timing for reference only.

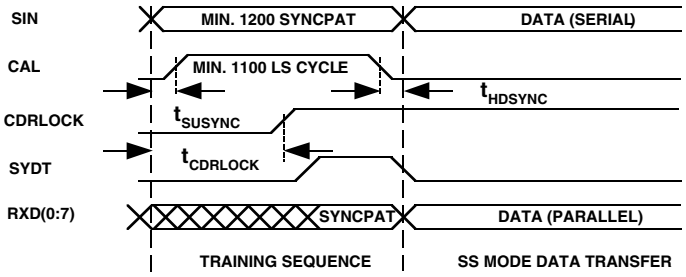
DESERIALIZER Timing[1]

Symbol	Description	Mode	Conditions	Min.	Max.	Units
f_{DSIN}	SIN Frequency Deviation from REFCLK	8B10B/ 10B12B		-100	+100	ppm
eo_{SIN}	SIN Eye Opening Tolerance	All CDR		0.4	—	UIPP
		SS (Note 1)		0.65	—	UIPP
ber	Bit Error Rate	All		—	10^{-12}	Bits
t_{SKRX}	Skew Margin Between SIN and SS_CLKIN	SS	Note 2	—	0.125	UIPP
t_{CKISIN}	SS_CLKIN to bit0 of SIN	SS	Note 2	2Bt - t_{SKRX}	2Bt + t_{SKRX}	ns
$t_{HSIOUTVALIDPRE}$	RXD, LOSS, CDRLOCK, SYDT Valid Time Before RECCLK Falling Edge	All	Note 3	t_{RCP} / 2-0.7	—	ns
$t_{HSIOUTVALIDPOST}$	RXD, LOSS, CDRLOCK, SYDT Valid Time After RECCLK Falling Edge	All	Note 3	t_{RCP} / 2-0.7	—	ns
t_{DSIN}	Bit 0 of SIN Delay to RXD Valid at RECCLK Falling edge	All CDR		$1.5t_{RCP}$ + 4.5Bt + 2	$1.5t_{RCP}$ + 4.5Bt + 10	ns
		SS	Note 2	$1.5t_{RCP}$ + 1.5Bt + 3	$1.5t_{RCP}$ + 1.5Bt + 15	ns

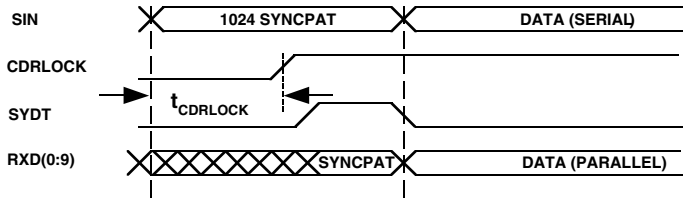
1. ispXPGA only. RX_SS mode only. This limit is increased if EO is increased.
2. SS Normal Receive Mode (no de-skew option).
3. Internal timing for reference only.

Lock-in Timing

CDRX_SS LOCK-IN (DE-SKEW) TIMING

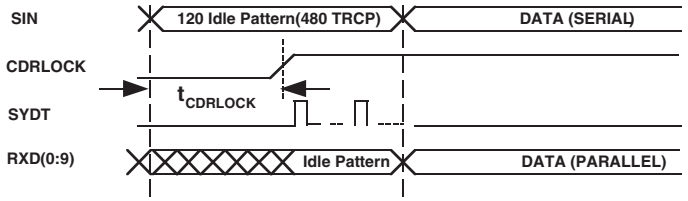


CDR_10B12B LOCK-IN TIMING



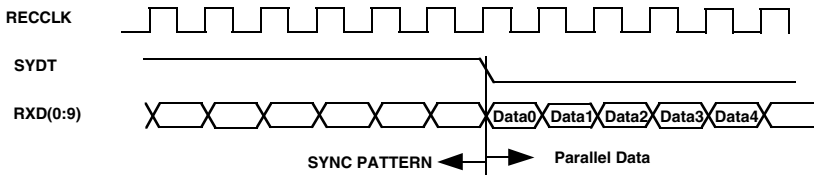
Lock-in Timing (Continued)

CDR_8B10B LOCK-IN TIMING

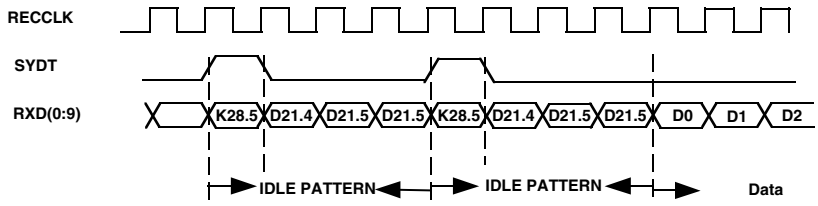


SYDT Timing

SYDT TIMING FOR CDRX_10B12B

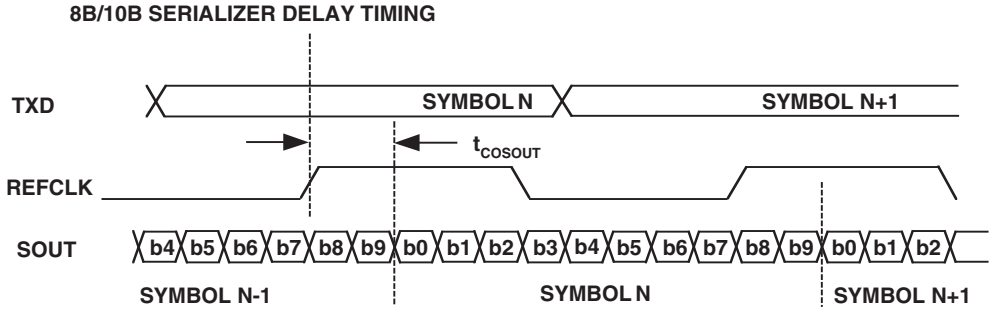


SYDT TIMING FOR CDRX_8B10B



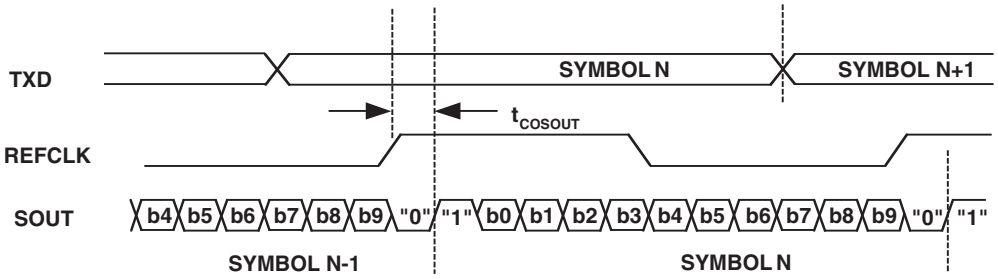
Serializer Timing

8B/10B SERIALIZER DELAY TIMING

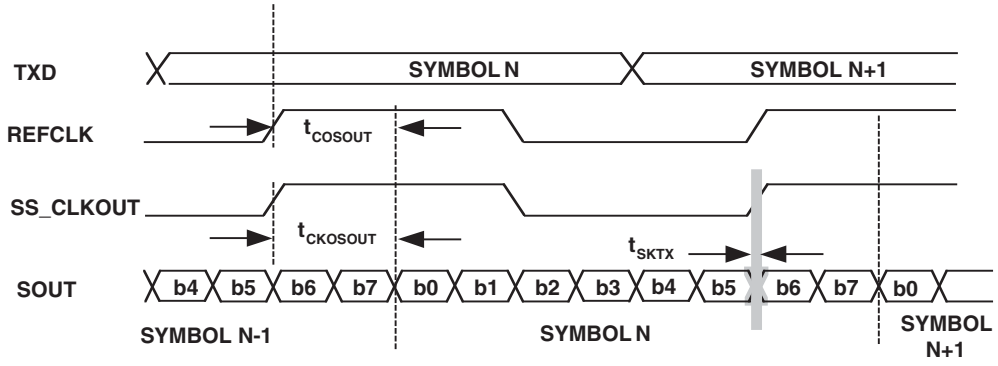


Serializer Timing (Continued)

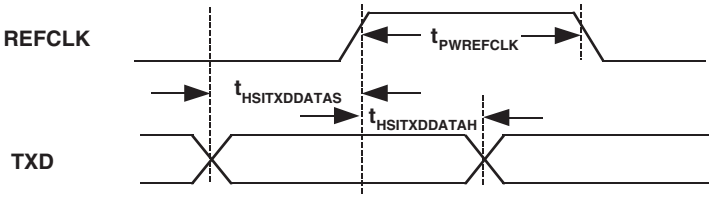
10B/12B SERIALIZER DELAY TIMING



SS Mode SERIALIZER DELAY TIMING

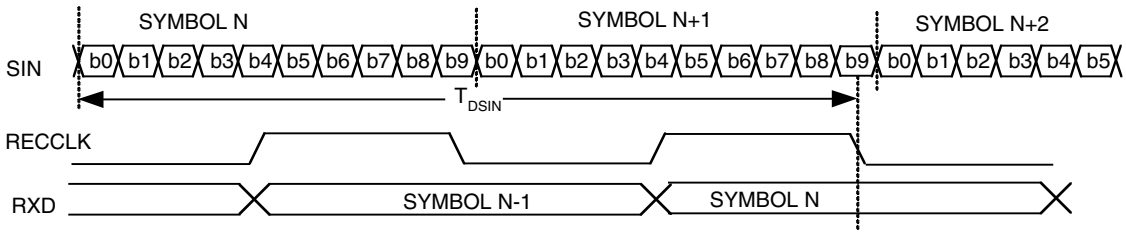


INTERNAL TIMING FOR sysHSI BLOCK



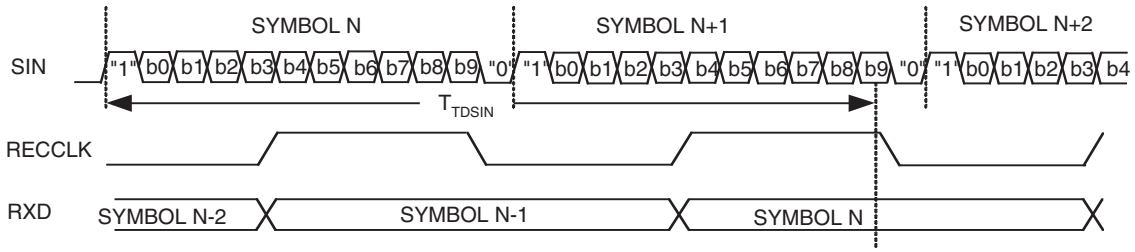
Deserializer Timing

8B/10B DESERIALIZER DELAY TIMING

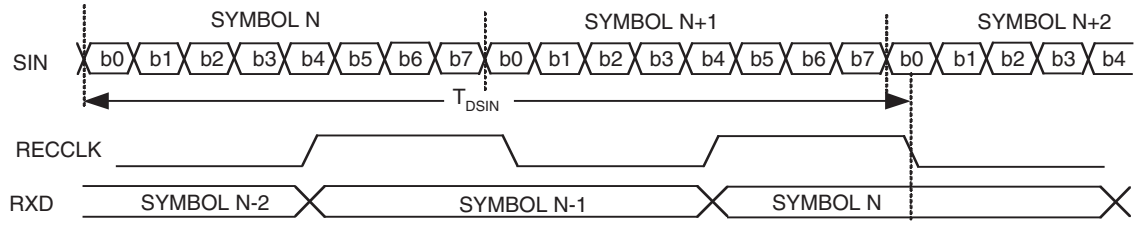


Deserializer Timing (Continued)

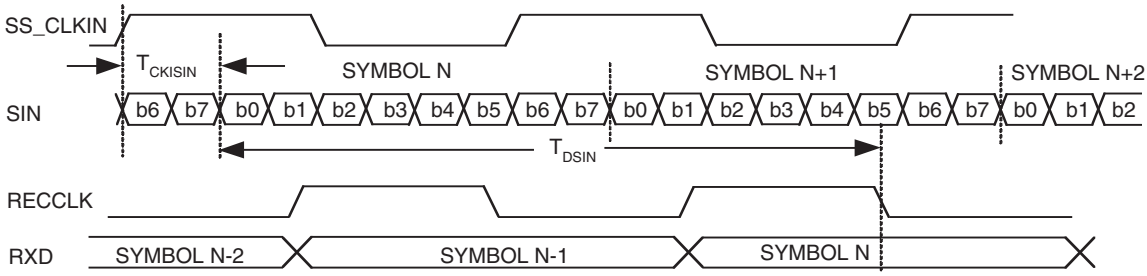
10B/12B DESERIALIZER DELAY TIMING



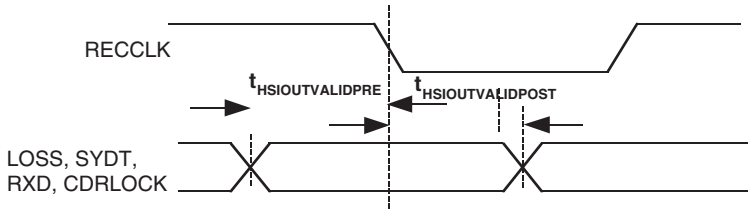
CDRX_SS DESERIALIZER DELAY TIMING



RX_SS DESERIALIZER DELAY TIMING



INTERNAL TIMING FOR sysHSI BLOCK



sysCLOCK PLL Timing

Over Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Units
t_{PWH}	Input clock, high time	80% to 80%	1.2	—	ns
t_{PWL}	Input clock, low time	20% to 20%	1.2	—	ns
t_R, t_F	Input Clock, rise and fall time	20% to 80%	—	3.0	ns
t_{INSTB}	Input clock stability, cycle to cycle (peak)		—	+/- 250	ps
f_{MDIVIN}	M Divider input, frequency range		10	320	MHz
$f_{MDIVOUT}$	M Divider output, frequency range		10	320	MHz
f_{NDIVIN}	N Divider input, frequency range		10	320	MHz
$f_{NDIVOUT}$	N Divider output, frequency range		10	320	MHz
f_{VDIVIN}	V Divider input, frequency range		100	400	MHz
$f_{VDIVOUT}$	V Divider output, frequency range		10	320	MHz
$t_{OUTDUTY}$	output clock, duty cycle		40	60	%
$t_{JIT(CC)}$	Output clock, cycle to cycle jitter (peak)	Clean reference. 10 MHz < $f_{MDIVOUT}$ < 20 MHz or 100MHz < f_{VDIVIN} < 160 MHz	—	+/- 250	ps
		Clean reference. 20 MHz < $f_{MDIVOUT}$ < 320 MHz and 160MHz < f_{VDIVIN} < 320 MHz	—	+/- 150	ps
$T_{JIT(PERIOD)}$	Output clock, period jitter (peak)	Clean reference. 10 MHz < $f_{MDIVOUT}$ < 20 MHz or 100MHz < f_{VDIVIN} < 160 MHz	—	+/- 300	ps
		Clean reference. 20 MHz < $f_{MDIVOUT}$ < 320 MHz and 160MHz < f_{VDIVIN} < 320 MHz	—	+/- 150	ps
$t_{CLK\_OUT\_DELAY}$	Input clock to CLK_OUT delay	Internal feedback	—	3.0	ns
t_{PHASE}	Input clock to external feedback delta	External feedback	—	600	ps
t_{LOCK}	Time to acquire phase lock after input stable		—	25	us
t_{PLL_DELAY}	Delay increment (Lead/Lag)	Typical = +/- 250ps	+/- 120	+/- 550	ps
t_{RANGE}	Total output delay range (lead/lag)		+/- 0.84	+/- 3.85	ns
t_{PLL_RSTW}	Minimum reset pulse width		—	1.8	ns
t_{CLK_IN}[3]	Global clock input delay		—	1.0	ns
$t_{PLL\_SEC\_DELAY}$	Secondary PLL output delay (t_{PLL_DELAY})		—	1.5	ns

1. This condition assures that the output phase jitter will remain within specification
2. Accumulated jitter measured over 10,000 waveform samples
3. Internal timing for reference only.

ispXP sysCONFIG Port Timing Specifications

Symbol	Timing Parameter	Min.	Typ.	Max.	Units
sysCONFIG Write Cycle Timing					
t_{SUCS}	Input setup time of CS to CCLK rise	12	—	—	ns
t_{HCS}	Hold time of CS to CCLK Rise	0	—	—	ns
t_{SUWD}	Input setup time of write data to CCLK rise	12	—	—	ns
t_{HWD}	Hold time of write data to CCLK rise	0	—	—	ns
t_{PRGM}	Low time to reset device SRAM	5	—	50	ns
t_{WINIT}	INIT pulse width	4	—	—	ms
t_{IODISS}	User I/O disable	—	—	30	ns
t_{WRDY}	Time to write data into SRAM	—	—	4	ms
t_{IOENSS}	User I/O enable	—	—	30	ns
t_{WH}	Write clock High pulse width	12	—	—	ns
t_{WL}	Write clock Low pulse width	12	—	—	ns
f_{MAXW}	Write f_{MAX}	—	—	25	MHz
sysCONFIG Read Cycle Timing					
t_{HREAD}	Hold time of READ to CCLK rise	0	—	—	ns
t_{SUREAD}	Input setup time of READ High to CCLK rise	30	—	—	ns
t_{RH}	READ clock high pulse width	12	—	—	ns
t_{RL}	READ clock low pulse width	15	—	—	ns
f_{MAXR}	Read f_{MAX}	—	—	25	MHz
t_{CORD}	Clock to out for read data	—	—	25	ns

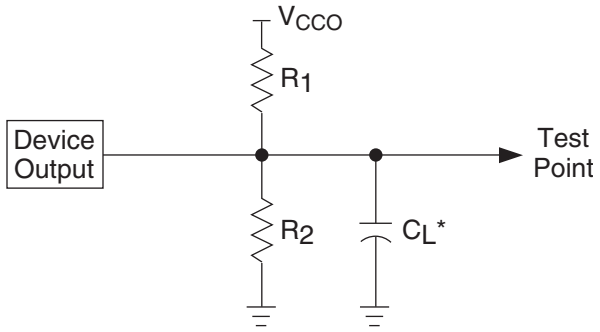
Boundary Scan Timing

Parameter	Description	Min.	Max.	Units
t_{BTCP}	TCK [BSCAN] Clock Pulse Width	40	—	ns
t_{BTCPH}	TCK [BSCAN] Clock Pulse Width High	20	—	ns
t_{BTCPL}	TCK [BSCAN] Clock Pulse Width Low	20	—	ns
t_{BTS}	TCK [BSCAN] Setup Time	8	—	ns
t_{BTH}	TCK [BSCAN] Hold Time	10	—	ns
t_{BTRF}	TCK [BSCAN] Rise/Fall Time	50	—	mV/ns
t_{BTCO}	TAP Controller Falling Edge of Clock to Valid Output	—	18	ns
$t_{BTCODIS}$	TAP Controller Falling Edge of Clock to Valid Disable	—	18	ns
t_{BTCOEN}	TAP Controller Falling Edge of Clock to Valid Enable	—	18	ns
t_{BTCRS}	BSCAN Test Capture Register Setup Time	8	—	ns
t_{BTCRH}	BSCAN Test Capture Register Hold Time	25	—	ns
t_{BUTCO}	BSCAN Test Update Register, Falling Edge of Clock to Valid Output	—	45	ns
$t_{BTUODIS}$	BSCAN Test Update Register, Falling Edge of Clock to Valid Disable	—	20	ns
$t_{BTUPOEN}$	BSCAN Test Update Register, Falling Edge of Clock to Valid Enable	—	20	ns

Switching Test Conditions

Figure 24 shows the output test load that is used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Table 8.

Figure 24. Output Test Load, LVTTL and LVCMOS Standards



*C_L includes test fixture and probe capacitance.

Table 8. Text Fixture Required Components

Test Condition	R_1	R_2	C_L	Timing Reference	VCCO
LVCMOS I/O, (L -> H, H -> L)	106	106	35pF	LVCMOS 3.3 = V_{CCO}/2	LVCMOS 3.3 = 3.0V
				LVCMOS 2.5 = V_{CCO}/2	LVCMOS 2.5 = 2.3V
				LVCMOS 1.8 = V_{CCO}/2	LVCMOS 1.8 = 1.65V
Default LVCMOS 1.8 I/O (Z -> H)	∞	106	35pF	0.9V	1.65V
Default LVCMOS 1.8 I/O (Z -> L)	106	∞	35pF	0.9V	1.65V
Default LVCMOS 1.8 I/O (H -> Z)	∞	106	5pF	V_{OH} - 0.3	1.65V
Default LVCMOS 1.8 I/O (L -> Z)	106	∞	5pF	V_{OL} + 0.3	1.65V

Note: Output test conditions for all other interfaces are determined by the respective standards.

Signal Descriptions[1]

Signal Name	Signal Type	Description
General Purpose		
BK*y*_IO*x*[1,2]	Input/Output	General purpose I/O number x in I/O Bank y
GCLK*n*/I*n*[7]	Input	Global clock/input[8]
GSR	Input	Global Set/Reset
NC	—	No Connect
GND	GND	Ground
V_{CC}	VCC	Core logic power supply
V_{CCJ}	VCC	IEEE 1149.1 TAP power supply
V_{CCOy}[2]	VCC	I/O Bank y power supply
V_{REFy}[2]	Input	I/O Bank y reference voltage
D_{XN}, D_{XP}	Output	Temperature Sensing Diodes, provide a differential voltage, which corresponds to the temperature of the device.
Test and Program/Configuration		
TMS	Input	Test Mode Select
TCK	Input	Test Clock
TDI	Input	Test Data In
TDO	Output	Test Data Out
TOE	Input	Test Output Enable tri-states all I/O pins
CFG0	Input	Selects the SRAM memory configuration type (Peripheral or E^2CMOS Refresh)
PROGRAMb	Input	Initiates download from E^2CMOS or the peripheral port to SRAM memory (active low)
DONE	Bi-directional	Indicates when configuration is complete
INITb	Bi-directional	Indicates the device is ready for programming (active low)
READ	Input	Selects the READ operation when in sysCONFIG mode
CCLK	Input	sysCONFIG Configuration Clock
CSb	Input	sysCONFIG Chip Select (active low)
DATA[0:7]	Bi-directional	sysCONFIG Peripheral Port Data I/O
sysCLOCK PLL[3]		
PLL_FBK*z*	Input	Optional external feedback
PLL_RST*z*	Input	Optional external M divider reset
CLK_OUT*z*	Internal Signal	Clock output (routable to any I/O)
PLL_LOCK*z*	Internal Signal	Lock output (routable to any I/O)
GND_P	GND	PLL Ground
V_{CCP}	VCC	PLL power supply
sysHSI Block[4, 5]		
HSI*m*A_SINP, HSI*m*B_SINP	Input	P-side of differential serial data input
HSI*m*A_SINN, HSI*m*B_SINN	Input	N-side of differential serial data input
HSI*m*A_SOUTP, HSI*m*B_SOUTP	Output	P-side of differential serial data output
HSI*m*A_SOUTN, HSI*m*B_SOUTN	Output	N-side of differential serial data output
HSI*m*A_LOSS, HSI*m*B_LOSS	Internal Signal	Detects loss of signal
HSI*m*A_SYDT, HSI*m*B_SYDT	Internal Signal	Symbol alignment detect
HSI*m*A_RECCLK, HSI*m*B_RECCLK	Internal Signal	Recovered clock
HSI*m*A_CDRLOCK, HSI*m*B_CDRLOCK	Internal Signal	Indicates when the CDR circuit is locked

Signal Descriptions[1] (Continued)

Signal Name	Signal Type	Description
HSI*m*A_CDRRST, HSI*m*B_CDRRST	Input	CDR Reset
HSI*m*A_EXLOSS, HSI*m*B_EXLOSS	Input	External loss indicates data on SIN is invalid, forces LOSS to “1”
HSI*m*_CSLOCK, HSI*m*_CSLOCK	Internal Signal	Indicates when the CSPLL circuit is locked
sysHSI Block (Source Synchronous Mode)[6]		
SS_CLKIN0P, SS_CLKIN1P	Input	P-side of differential clock input
SS_CLKIN0N, SS_CLKIN1N	Input	N-side of differential clock input
SS_CLKOUT0P, SS_CLKOUT1P	Output	P-side of differential clock output
SS_CLKOUT0N, SS_CLKOUT1N	Output	N-side of differential clock output
CAL0, CAL1	Input	Initiates source synchronous calibration sequence

1. x is a variable for the I/O number.
2. y is a variable for the I/O Bank.
3. z is a variable for the PLL number.
4. m is a variable for the sysHSI block number.
5. A and B refer to the sysHSI block channels.
6. 0 and 1 refer to Source Synchronous group 0 and 1
7. n is a variable for the GCLK and Input number
8. See Logic Signal Connections Table for differential pairing.

ispXPGA Power Supply and NC Connections[1]

Signal	256-Ball fpBGA[3]	516-Ball fpBGA[3]
V_{CC}	C3, C14, D4, D13, E5, E12, F6, F11, L6, L11, M5, M12, N4, N13, P3, P14	A9, A22, D4, D27, J1, J30, L11, L12, L15, L16, L19, L20, M11, M20, R11, R20, T11, T20, W11, W20, Y11, Y12, Y15, Y16, Y19, Y20, AB1, AB30, AG4, AG27, AK9, AK22
V_{CCO0}	F5, G5	F4, J4, M4, N11, P4, P11
V_{CCO1}	K5, L5	U4, U11, V11, W4, AB4, AE4
V_{CCO2}	M6, M7	Y13, Y14, AG6, AG9, AG12, AG14
V_{CCO3}	M10, M11	Y17, Y18, AG17, AG19, AG22, AG25
V_{CCO4}	K12, L12	U20, U27, V20, W27, AB27, AE27
V_{CCO5}	G12, F12	F27, J27, M27, N20, P20, P27
V_{CCO6}	E10, E11	D17, D19, D22, D25, L17, L18
V_{CCO7}	E6, E7	D6, D9, D12, D14, L13, L14
V_{CCP}	H3, J15	R4, T30
V_{CCJ}	A2	C4
GND	A1, A16, B2, B15, F7, F8, F9, F10, G6, G7, G8, G9, G10, G11, H6, H7, H8, H9, H10, H11, J6, J7, J8, J9, J10, J11, K6, K7, K8, K9, K10, K11, L7, L8, L9, L10, R2, R15, T1, T16	A1, A30, B2, B29, C3, C28, M12, M13, M14, M15, M16, M17, M18, M19, N12, N13, N14, N15, N16, N17, N18, N19, P12, P13, P14, P15, P16, P17, P18, P19, R12, R13, R14, R15, R16, R17, R18, R19, T12, T13, T14, T15, T16, T17, T18, T19, U12, U13, U14, U15, U16, U17, U18, U19, V12, V13, V14, V15, V16, V17, V18, V19, W12, W13, W14, W15, W16, W17, W18, W19, AH3, AH28, AJ2, AJ29, AK1, AK30
GND_P	H15, J4	R29, T4
NC[2]	—	**LFX125:** A10, A13, A16, A17, A24, A25, A26, A4, A5, A6, A7, AA1, AA2, AA28, AA29, AA3, AB28, AC1, AC28, AD1, AD27, AD4, AE28, AE29, AE3, AE30, AF27, AF28, AF29, AF3, AF4, AG1, AG10, AG11, AG15, AG2, AG20, AG23, AG24, AG29, AG3, AG8, AH1, AH15, AH19, AH2, AH20, AH23, AH24, AH30, AH7, AH8, AH9, AJ1, AJ12, AJ14, AJ15, AJ19, AJ20, AJ21, AJ23, AJ24, AJ25, AJ27, AJ30, AJ6, AJ7, AJ8, AK11, AK14, AK15, AK20, AK21, AK23, AK24, AK25, AK27, AK5, AK6, AK7, B10, B13, B16, B17, B18, B23, B24, B25, B5, B6, B7, C11, C13, C14, C16, C17, C22, C23, C24, C25, C6, C7, C8, D11, D16, D23, D24, D28, D29, D3, D7, D8, E30, E4, F1, F29, F30, G1, G2, G27, G28, G29, G30, H1, H2, H27, H28, H29, H30, J2, J28, J29, J3, K1, K2, K27, K28, K3, K4, L1, L2, L27, L3, L4, M1, M2, M29, M3, M30, V27, V28, V3, V4, W1, W30, Y1, Y27, Y28, Y3, Y30 **LFX200:** A26, A25, A24, A17, A10, A7, A6, A5, A4, B25, B24, B23, B17, B10, B7, B6, B5, C25, C24, C23, C22, C16, C11, C8, C7, C6, D24, D23, D16, D11, D8, D7, E30, F30, F29, F1, G30, G29, G28, G27, G2, G1, H30, H29, H28, H27, H2, H1, J29, J28, J3, J2, K28, K27, K4, K3, K2, K1, L27, L4, L3, L2, L1, M3, V28, V27, V4, V3, W30, W1, Y30, Y28, Y27, Y3, Y1, AA29, AA28, AA3, AA2, AA1, AD27, AD4, AE28, AE3, AF29, AF28, AF27, AF3, AG29, AG24, AG23, AG20, AG11, AG10, AG8, AG2, AG1, AH30, AH24, AH23, AH20, AH9, AH8, AH7, AH2, AH1, AJ30, AJ27, AJ25, AJ24, AJ23, AJ21, AJ15, AJ12, AJ8, AJ7, AJ6, AJ1, AK27, AK25, AK24, AK23, AK21, AK15, AK11, AK7, AK6, AK5

1. All grounds must be electrically connected at the board level.
2. NC pins should not be connected to any active signals, V_{CC} or GND.
3. Balls for GND, V_{CC} and V_{CCOx} are connected within the substrate to their respective common signals. Pin orientation A1 starts from the upper left corner of the top side view with alphabetical order ascending vertically and numerical order ascending horizontally.

ispXPGA Power Supply and NC Connections[1] (Continued)

Signal	680-Ball fpBGA[3]	900-Ball fpBGA[3]
V_{CC}	AE35, AE5, AL5, AR15, AR25, AR31, AR35, AR5, AT36, AT4, AU3, AU37, C3, C37, D36, D4, E15, E25, E35, E5, E9, J35, R35, R5	L11, L20, M12, M13, M14, M17, M18, M19, N12, N19, P12, P19, U12, U19, V12, V19, W12, W13, W14, W17, W18, W19, Y11, Y20
V_{CCO0}	E11, E12, E13, E17, E18, E7	K3, L10, M11, N11, N5, P11, R11, R12
V_{CCO1}	E22, E23, E27, E29, E31, E33	AA3, T11, T12, U11, V11, V5, W11, Y10
V_{CCO2}	G35, L35, M35, N35, U35, V35	AA11, AF13, AH10, W15, Y12, Y13, Y14, Y15
V_{CCO3}	AB35, AC35, AG35, AJ35, AL35, AN35	AA20, AF18, AH21, W16, Y16, Y17, Y18, Y19
V_{CCO4}	AR22, AR23, AR27, AR28, AR29, AR33	AA28, T19, T20, U20, V20, V26, W20, Y21
V_{CCO5}	AR11, AR13, AR17, AR18, AR7, AR9	K28, L21, M20, N20, N26, P20, R19, R20
V_{CCO6}	AB5, AC5, AG5, AH5, AJ5, AN5	C21, E18, K20, L16, L17, L18, L19, M16
V_{CCO7}	G5, J5, L5, N5, U5, V5	C10, E13, K11, L12, L13, L14, L15, M15
V_{CCP}	E20, AW22	R5, T26
V_{CCJ}	D3	B3
GND	A1, A2, A20, A38, A39, AE3, AE37, AK3, AK37, AR36, AR4, AT20, AT35, AT5, AU10, AU14, AU20, AU26, AU30, AV1, AV2, AV20, AV38, AV39, AW1, AW2, AW20, AW38, AW39, B1, B2, B20, B38, B39, C10, C14, C20, C26, C30, D20, D35, D5, E36, E4, K3, K37, P37, R3, Y1, Y2, Y3, Y36, Y37, Y38, Y39, Y4	A1, A2, A29, A30, AB28, AB3, AG27, AG4, AH22, AH28, AH3, AH9, AJ1, AJ2, AJ29, AJ30, AK1, AK2, AK29, AK30, B1, B2, B29, B30, C22, C28, C3, C9, D27, D4, J28, J3, N13, N14, N15, N16, N17, N18, P13, P14, P15, P16, P17, P18, R13, R14, R15, R16, R17, R18, T13, T14, T15, T16, T17, T18, U13, U14, U15, U16, U17, U18, V13, V14, V15, V16, V17, V18
GND_P	AR20, A21	R28, T3
NC[2]	A3, B29, AW3, AV3, AW11, AV11, AV29, AW29, AW37, B3, AV37, C39, C38, AU39, AU38, AJ39, AJ38, N38, N39, C2, C1, AU1, AU2, AJ2, AJ1, N2, N1, B11, A11, A37, B37, A29	**LFX500:** A8, A9, A10, A11, A19, A20, A21, A22, B8, B9, B10, B11, B19, B20, B21, B22, C1, C2, C11, C12, C19, C20, C23, D3, D10, D11, D12, D19, D20, D21, D22, D23, E3, E10, E11, E12, E21, E22, E28, E29, E30, F1, F2, F10, F11, F12, F21, F26, F29, F30, G1, G2, G3, G4, G10, G25, G26, G27, G28, G29, G30, H1, H2, H3, H4, H27, H28, H29, H30, J1, J2, J4, J5, J6, J7, J24, J25, J26, J27, W25, W26, Y3, Y4, Y5, Y6, Y25, Y26, Y27, Y28, AA4, AA5, AA16, AA17, AA18, AA19, AA21, AA26, AA27, AB1, AB2, AB4, AB5, AB6, AB7, AB24, AB25, AB26, AB27, AC1, AC2, AC3, AC4, AC5, AC6, AC27, AC28, AC29, AC30, AD1, AD2, AD10, AD21, AD29, AD30, AE10, AE11, AE12, AE19, AE20, AE21, AE29, AE30, AF10, AF11, AF12, AF19, AF20, AF21, AF22, AG10, AG11, AG12, AG19, AG20, AG21, AG22, AH11, AH12, AH19, AH20, AJ8, AJ9, AJ10, AJ11, AJ20, AJ21, AJ22, AK8, AK9, AK10, AK11, AK20, AK21, AK22 **LFX1200:** AA22, AA23, AA24, AA25, AB23, AC24, T21, T22, T23, T24, T25, U21, U22, U23, U24, V21, V22, V23, W21, W22, W23, W24, Y22, Y23, Y24, AA16, AA17, AA18, AA19, AA21, AB16, AB17, AB18, AB19, AB20, AB21, AB22, AC16, AC17, AC18, AC19, AC20, AC21, AC22, AC23, AD16, AD17, AD19, AD20, AD22, AD23, AD24, AE22, AE25, AF25, AF26, AA10, AA12, AA13, AA14, AA15, AB10, AB11, AB12, AB13, AB14, AB15, AB9, AC10, AC11, AC12, AC13, AC14, AC15, AC8, AC9, AD11, AD12, AD14, AD15, AD7, AD8, AD9, AE6, AE9, AF5, AF6, H24, J23, K22, K23, K24, K25, L22, L23, L24, M21, M22, M23, M24, N21, N22, N23, P21, P22, P23, P24, R21, R22, R23, R24, R25, AA6, AA7, AA8, AA9, AB8, AC7, T10, T6, T7, T8, T9, U10, U7, U8, U9, V10, V8, V9, W10, W7, W8, W9, Y7, Y8, Y9, H5, H6, H7, J8, K6, K7, K8, K9, L7, L8, L9, M10, M7, M8, M9, N10, N8, N9, P10, P7, P8, P9, R10, R8, R9, E25, E26, F22, F25, G16, G17, G19, G20, G22, G23, G24, H16, H17, H18, H19, H20, H21, H22, H23, J16, J17, J18, J19, J20, J21, J22, K16, K17, K18, K19, K21, E5, E6, F6, F9, G11, G12, G14, G15, G7, G8, G9, H10, H11, H12, H13, H14, H15, H8, H9, J10, J11, J12, J13, J14, J15, J9, K10, K12, K13, K14, K15

1. All grounds must be electrically connected at the board level.
2. NC pins should not be connected to any active signals, V_{CC} or GND.
3. Balls for GND, V_{CC} and V_{CCOx} are connected within the substrate to their respective common signals. Pin orientation A1 starts from the upper left corner of the top side view with alphabetical order ascending vertically and numerical order ascending horizontally.

ispXPGA Logic Signal Connections: 256-Ball fpBGA

	LFX200			LFX125		
256-fpBGA Ball	Signal Name	Second Function	LVDS Pair/ Polarity	Signal Name	Second Function	LVDS Pair/ Polarity
C2	BK0_IO2	HSI0A_SOUTP	1P	BK0_IO0	HSI0A_SOUTP	0P
-	GND (Bank 0)	-	-	-	-	-
D2	BK0_IO3	HSI0A_SOUTN	1N	BK0_IO1	HSI0A_SOUTN	0N
B1	BK0_IO6	HSI0A_SINP	3P	BK0_IO4	HSI0A_SINP	2P
-	-	-	-	GND (Bank 0)	-	-
C1	BK0_IO7	HSI0A_SINN	3N	BK0_IO5	HSI0A_SINN	2N
D3	BK0_IO8	-	4P	BK0_IO6	-	3P
E3	BK0_IO9	VREF0	4N	BK0_IO7	VREF0	3N
D1	BK0_IO10	HSI0B_SOUTP	5P	BK0_IO8	HSI0B_SOUTP	4P
-	GND (Bank 0)	-	-	-	-	-
E1	BK0_IO11	HSI0B_SOUTN	5N	BK0_IO9	HSI0B_SOUTN	4N
E2	BK0_IO12	-	6P	BK0_IO10	-	5P
F2	BK0_IO13	-	6N	BK0_IO11	-	5N
F1	BK0_IO14	HSI0B_SINP	7P	BK0_IO12	HSI0B_SINP	6P
-	-	-	-	GND (Bank 0)	-	-
G1	BK0_IO15	HSI0B_SINN	7N	BK0_IO13	HSI0B_SINN	6N
F3	BK0_IO18	PLL_FBK0	9P	BK0_IO14	PLL_FBK0	7P
-	GND (Bank 0)	-	-	-	-	-
G2	BK0_IO19	PLL_RST1	9N	BK0_IO15	PLL_RST1	7N
E4	BK0_IO20	-	10P	BK0_IO16	-	8P
F4	BK0_IO21	PLL_FBK1	10N	BK0_IO17	PLL_FBK1	8N
H1	BK0_IO22	PLL_RST0	11P	BK0_IO18	PLL_RST0	9P
-	-	-	-	GND (Bank 0)	-	-
J1	BK0_IO23	-	11N	BK0_IO19	-	9N
H2	BK0_IO24	CLK_OUT0	12P	BK0_IO20	CLK_OUT0	10P
G3	BK0_IO25	CLK_OUT1	12N	BK0_IO21	CLK_OUT1	10N
-	GND (Bank 0)	-	-	-	-	-
G4	GCLK0	-	LVDSCLK0	GCLK0	-	LVDSCLK0
H4	GCLK1	-	LVDSCLK0	GCLK1	-	LVDSCLK0
H3	VCCP0	-	-	VCCP0	-	-
J4	GNDP0	-	-	GNDP0	-	-
J2	GCLK2	-	LVDSCLK1	GCLK2	-	LVDSCLK1
J3	GCLK3	-	LVDSCLK1	GCLK3	-	LVDSCLK1
-	GND (Bank 1)	-	-	-	-	-
H5	BK1_IO0	CLK_OUT2	13P	BK1_IO0	CLK_OUT2	11P
J5	BK1_IO1	CLK_OUT3	13N	BK1_IO1	CLK_OUT3	11N
K1	BK1_IO2	SS_CLKOUT0P	14P	BK1_IO2	SS_CLKOUT0P	12P
-	-	-	-	GND (Bank 1)	-	-
L1	BK1_IO3	SS_CLKOUT0N	14N	BK1_IO3	SS_CLKOUT0N	12N
K4	BK1_IO4	PLL_FBK2	15P	BK1_IO4	PLL_FBK2	13P
L4	BK1_IO5	PLL_FBK3	15N	BK1_IO5	PLL_FBK3	13N
K3	BK1_IO6	SS_CLKIN0P	16P	BK1_IO6	SS_CLKIN0P	14P

ispXPGA Logic Signal Connections: 256-Ball fpBGA (Continued)

256-fpBGA Ball	LFX200			LFX125		
	Signal Name	Second Function	LVDS Pair/ Polarity	Signal Name	Second Function	LVDS Pair/ Polarity
-	GND (Bank 1)	-	-	-	-	-
L3	BK1_IO7	SS_CLKIN0N	16N	BK1_IO7	SS_CLKIN0N	14N
K2	BK1_IO8	-	17P	BK1_IO8	-	15P
-	-	-	-	GND (Bank 1)	-	-
L2	BK1_IO9	-	17N	BK1_IO9	-	15N
M1	BK1_IO10	HSI1A_SOUTP	18P	BK1_IO10	-	16P
N1	BK1_IO11	HSI1A_SOUTN	18N	BK1_IO11	-	16N
M3	BK1_IO12	PLL_RST2	19P	BK1_IO12	PLL_RST2	17P
M4	BK1_IO13	PLL_RST3	19N	BK1_IO13	PLL_RST3	17N
-	GND (Bank 1)	-	-	-	-	-
M2	BK1_IO16[1]	VREF1	-	BK1_IO14[1]	VREF1	-
P1	BK1_IO18	HSI1B_SOUTP	22P	BK1_IO16	-	19P
-	-	-	-	GND (Bank 1)	-	-
R1	BK1_IO19	HSI1B_SOUTN	22N	BK1_IO17	-	19N
N3	BK1_IO20[1]	-	-	BK1_IO18[1]	-	-
N2	BK1_IO22	HSI1B_SINP	24P	BK1_IO20	-	21P
-	GND (Bank 1)	-	-	-	-	-
P2	BK1_IO23	HSI1B_SINN	24N	BK1_IO21	-	21N
P4	TCK	-	-	TCK	-	-
T2	TMS	-	-	TMS	-	-
T3	TOE	-	-	TOE	-	-
R3	BK2_IO0	-	26P	BK2_IO0	-	22P
R4	BK2_IO1	-	26N	BK2_IO1	-	22N
N5	BK2_IO2	-	27P	BK2_IO2	-	23P
-	GND (Bank 2)	-	-	-	-	-
P5	BK2_IO3	-	27N	BK2_IO3	-	23N
-	-	-	-	GND (Bank 2)	-	-
T4	BK2_IO6	-	29P	BK2_IO6	-	25P
T5	BK2_IO7	-	29N	BK2_IO7	-	25N
N6	BK2_IO8	-	30P	BK2_IO8	-	26P
P6	BK2_IO9	VREF2	30N	BK2_IO9	VREF2	26N
R5	BK2_IO10	-	31P	BK2_IO10	-	27P
-	GND (Bank 2)	-	-	-	-	-
R6	BK2_IO11	-	31N	BK2_IO11	-	27N
N7	BK2_IO12	-	32P	BK2_IO12	-	28P
-	-	-	-	GND (Bank 2)	-	-
P7	BK2_IO13	-	32N	BK2_IO13	-	28N
T6	BK2_IO14	-	33P	BK2_IO14	-	29P
T7	BK2_IO15	-	33N	BK2_IO15	-	29N
M8	BK2_IO16	-	34P	BK2_IO16	-	30P
M9	BK2_IO17	-	34N	BK2_IO17	-	30N
R7	BK2_IO18	-	35P	BK2_IO18	-	31P

ispXPGA Logic Signal Connections: 256-Ball fpBGA (Continued)

	LFX200			LFX125		
256-fpBGA Ball	Signal Name	Second Function	LVDS Pair/ Polarity	Signal Name	Second Function	LVDS Pair/ Polarity
-	GND (Bank 2)	-	-	GND (Bank 2)	-	-
R8	BK2_IO19	-	35N	BK2_IO19	-	31N
N8	BK2_IO20	-	36P	BK2_IO20	-	32P
P8	BK2_IO21	-	36N	BK2_IO21	-	32N
-	GND (Bank 2)	-	-	-	-	-
-	GND (Bank 3)	-	-	-	-	-
T8	BK3_IO0	-	39P	BK3_IO0	-	33P
T9	BK3_IO1	-	39N	BK3_IO1	-	33N
R9	BK3_IO2	-	40P	BK3_IO2	-	34P
-	-	-	-	GND (Bank 3)	-	-
R10	BK3_IO3	-	40N	BK3_IO3	-	34N
P9	BK3_IO4	-	41P	BK3_IO4	-	35P
N9	BK3_IO5	-	41N	BK3_IO5	-	35N
T10	BK3_IO6	-	42P	BK3_IO6	-	36P
-	GND (Bank 3)	-	-	-	-	-
T11	BK3_IO7	-	42N	BK3_IO7	-	36N
P10	BK3_IO8	-	43P	BK3_IO8	-	37P
-	-	-	-	GND (Bank 3)	-	-
N10	BK3_IO9	-	43N	BK3_IO9	-	37N
R11	BK3_IO14	-	46P	BK3_IO10	-	38P
-	GND (Bank 3)	-	-	-	-	-
R12	BK3_IO15	-	46N	BK3_IO11	-	38N
P11	BK3_IO16	VREF3	47P	BK3_IO12	VREF3	39P
N11	BK3_IO17	-	47N	BK3_IO13	-	39N
T12	BK3_IO18	-	48P	BK3_IO14	-	40P
T13	BK3_IO19	-	48N	BK3_IO15	-	40N
R13	BK3_IO20	-	49P	BK3_IO16	-	41P
-	-	-	-	GND (Bank 3)	-	-
R14	BK3_IO21	-	49N	BK3_IO17	-	41N
P12	BK3_IO22	-	50P	BK3_IO18	-	42P
-	GND (Bank 3)	-	-	-	-	-
N12	BK3_IO23	-	50N	BK3_IO19	-	42N
T14	RESET	-	-	RESET	-	-
T15	DXP	-	-	DXP	-	-
P13	DXN	-	-	DXN	-	-
P15	BK4_IO0	-	52P	BK4_IO0	-	44P
N14	BK4_IO1	-	52N	BK4_IO1	-	44N
R16	BK4_IO2	HSI2A_SINP	53P	BK4_IO2	-	45P
-	GND (Bank 4)	-	-	-	-	-
P16	BK4_IO3	HSI2A_SINN	53N	BK4_IO3	-	45N
N15	BK4_IO4	-	54P	BK4_IO4	-	46P
-	-	-	-	GND (Bank 4)	-	-

ispXPGA Logic Signal Connections: 256-Ball fpBGA (Continued)

	LFX200			LFX125		
256-fpBGA Ball	Signal Name	Second Function	LVDS Pair/ Polarity	Signal Name	Second Function	LVDS Pair/ Polarity
M15	BK4_IO5	-	54N	BK4_IO5	-	46N
M14	BK4_IO8	-	56P	BK4_IO6	-	47P
M13	BK4_IO9	VREF4	56N	BK4_IO7	VREF4	47N
-	GND (Bank 4)	-	-	-	-	-
L13	BK4_IO12	PLL_RST4	58P	BK4_IO8	PLL_RST4	48P
L14	BK4_IO13	PLL_RST5	58N	BK4_IO9	PLL_RST5	48N
N16	BK4_IO14	HSI2B_SOUTP	59P	BK4_IO10	-	49P
M16	BK4_IO15	HSI2B_SOUTN	59N	BK4_IO11	-	49N
-	-	-	-	GND (Bank 4)	-	-
L15	BK4_IO18	SS_CLKIN1P	61P	BK4_IO14	SS_CLKIN1P	51P
-	GND (Bank 4)	-	-	-	-	-
K15	BK4_IO19	SS_CLKIN1N	61N	BK4_IO15	SS_CLKIN1N	51N
K14	BK4_IO20	PLL_FBK4	62P	BK4_IO16	PLL_FBK4	52P
K13	BK4_IO21	PLL_FBK5	62N	BK4_IO17	PLL_FBK5	52N
L16	BK4_IO22	SS_CLKOUT1P	63P	BK4_IO18	SS_CLKOUT1P	53P
-	-	-	-	GND (Bank 4)	-	-
K16	BK4_IO23	SS_CLKOUT1N	63N	BK4_IO19	SS_CLKOUT1N	53N
J13	BK4_IO24	CLK_OUT4	64P	BK4_IO20	CLK_OUT4	54P
J12	BK4_IO25	CLK_OUT5	64N	BK4_IO21	CLK_OUT5	54N
-	GND (Bank 4)	-	-	-	-	-
J14	GCLK4	-	LVDSCLK2	GCLK4	-	LVDSCLK2
H14	GCLK5	-	LVDSCLK2	GCLK5	-	LVDSCLK2
J15	VCCP1	-	-	VCCP1	-	-
H15	GNDP1	-	-	GNDP1	-	-
J16	GCLK6	-	LVDSCLK3	GCLK6	-	LVDSCLK3
H16	GCLK7	-	LVDSCLK3	GCLK7	-	LVDSCLK3
-	GND (Bank 5)	-	-	-	-	-
H12	BK5_IO0	CLK_OUT6	65P	BK5_IO0	CLK_OUT6	55P
H13	BK5_IO1	CLK_OUT7	65N	BK5_IO1	CLK_OUT7	55N
G14	BK5_IO2	-	66P	BK5_IO2	-	56P
-	-	-	-	GND (Bank 5)	-	-
G15	BK5_IO3	PLL_RST7	66N	BK5_IO3	PLL_RST7	56N
G13	BK5_IO6	PLL_RST6	68P	BK5_IO6	PLL_RST6	58P
-	GND (Bank 5)	-	-	-	-	-
F13	BK5_IO7	-	-	BK5_IO7	PLL_FBK7	58N
G16	BK5_IO10	HSI3A_SINP	70P	BK5_IO8	HSI1A_SINP	59P
-	-	-	-	GND (Bank 5)	-	-
F16	BK5_IO11	HSI3A_SINN	70N	BK5_IO9	HSI1A-SINN	59N
F14	BK5_IO12	-	71P	BK5_IO10	-	60P
F15	BK5_IO13	-	71N	BK5_IO11	-	60N
E16	BK5_IO14	HSI3A_SOUTP	72P	BK5_IO12	HSI1A_OUTP	61P
-	GND (Bank 5)	-	-	-	-	-

ispXPGA Logic Signal Connections: 256-Ball fpBGA (Continued)

	LFX200			LFX125		
256-fpBGA Ball	Signal Name	Second Function	LVDS Pair/ Polarity	Signal Name	Second Function	LVDS Pair/ Polarity
D16	BK5_IO15	HSI3A_SOUTN	72N	BK5_IO13	HSI1A_OUTN	61N
E13	BK5_IO16	VREF5	73P	BK5_IO14	VREF5	62P
E14	BK5_IO17	-	73N	BK5_IO15	-	62N
E15	BK5_IO18	HSI3B_SINP	74P	BK5_IO16	HSI1B_SINP	63P
-	-	-	-	GND (Bank 5)	-	-
D15	BK5_IO19	HSI3B_SINN	74N	BK5_IO17	HSI1B_SINN	63N
C16	BK5_IO22	HSI3B_SOUTP	76P	BK5_IO20	HSI1B_OUTP	65P
-	GND (Bank 5)	-	-	-	-	-
B16	BK5_IO23	HSI3B_SOUTN	76N	BK5_IO21	HSI1B_OUTN	65N
D14	BK5_IO24	-	77P	BK5_IO18	-	64P
C15	BK5_IO25	-	77N	BK5_IO19	-	64N
C13	CFG0	-	-	CFG0	-	-
A15	DONE	-	-	DONE	-	-
A14	PROGRAMb	-	-	PROGRAMb	-	-
D12	BK6_IO0	INITb	78P	BK6_IO0	INITb	66P
C12	BK6_IO1	CCLK	78N	BK6_IO1	CCLK	66N
B14	BK6_IO2	-	79P	BK6_IO2	-	67P
-	GND (Bank 6)	-	-	-	-	-
B13	BK6_IO3	-	79N	BK6_IO3	-	67N
A13	BK6_IO4	CSb	80P	BK6_IO4	CSb	68P
-	-	-	-	GND (Bank 6)	-	-
A12	BK6_IO5	Read	80N	BK6_IO5	READ	68N
D11	BK6_IO6	DATA7	81P	BK6_IO6	DATA7	69P
C11	BK6_IO7	DATA6	81N	BK6_IO7	DATA6	69N
B12	BK6_IO8	-	82P	BK6_IO8	-	70P
B11	BK6_IO9	VREF6	82N	BK6_IO9	VREF6	70N
D10	BK6_IO10	DATA5	83P	BK6_IO10	DATA5	71P
-	GND (Bank 6)	-	-	-	-	-
C10	BK6_IO11	DATA4	83N	BK6_IO11	DATA4	71N
-	-	-	-	GND (Bank 6)	-	-
A11	BK6_IO14	DATA3	85P	BK6_IO14	DATA3	73P
A10	BK6_IO15	DATA2	85N	BK6_IO15	DATA2	73N
D9	BK6_IO16	-	86P	BK6_IO16	-	74P
C9	BK6_IO17	-	86N	BK6_IO17	-	74N
B10	BK6_IO18	DATA1	87P	BK6_IO18	DATA1	75P
-	GND (Bank 6)	-	-	GND (Bank 6)	-	-
B9	BK6_IO19	DATA0	87N	BK6_IO19	DATA0	75N
E9	BK6_IO20	-	88P	BK6_IO20	-	76P
E8	BK6_IO21	-	88N	BK6_IO21	-	76N
-	GND (Bank 6)	-	-	-	-	-
-	GND (Bank 7)	-	-	-	-	-
D8	BK7_IO0	-	91P	BK7_IO0	-	77P

ispXPGA Logic Signal Connections: 256-Ball fpBGA (Continued)

	LFX200			LFX125		
256-fpBGA Ball	Signal Name	Second Function	LVDS Pair/ Polarity	Signal Name	Second Function	LVDS Pair/ Polarity
C8	BK7_IO1	-	91N	BK7_IO1	-	77N
B8	BK7_IO2	-	92P	BK7_IO2	-	78P
B7	BK7_IO3	-	92N	BK7_IO3	-	78N
A9	BK7_IO6	-	94P	BK7_IO4	-	79P
-	GND (Bank 7)	-	-	-	-	-
A8	BK7_IO7	-	94N	BK7_IO5	-	79N
C7	BK7_IO10	-	96P	BK7_IO6	-	80P
D7	BK7_IO11	-	96N	BK7_IO7	-	80N
D6	BK7_IO12	-	97P	BK7_IO8	-	81P
-	-	-	-	GND (Bank 7)	-	-
C6	BK7_IO13	-	97N	BK7_IO9	-	81N
B6	BK7_IO14	-	98P	BK7_IO10	-	82P
-	GND (Bank 7)	-	-	-	-	-
B5	BK7_IO15	-	98N	BK7_IO11	-	82N
A7	BK7_IO16	VREF7	99P	BK7_IO12	VREF7	83P
A6	BK7_IO17	-	99N	BK7_IO13	-	83N
D5	BK7_IO18	-	100P	BK7_IO14	-	84P
C5	BK7_IO19	-	100N	BK7_IO15	-	84N
A5	BK7_IO20	-	101P	BK7_IO16	-	85P
-	-	-	-	GND (Bank 7)	-	-
A4	BK7_IO21	-	101N	BK7_IO17	-	85N
B4	BK7_IO22	-	102P	BK7_IO18	-	86P
-	GND (Bank 7)	-	-	-	-	-
B3	BK7_IO23	-	102N	BK7_IO19	-	86N
A3	TDO	-	-	TDO	-	-
A2	VCCJ	-	-	VCCJ	-	-
C4	TDI	-	-	TDI	-	-

1. Not available for differential pairs.

ispXPGA Logic Signal Connections: 516-Ball fpBGA

516-Ball BGA Ball	LFX500			LFX200			LFX125		
	Signal Name	Second Function	LVDS Pair/ Polarity	Signal Name	Second Function	LVDS Pair/ Polarity	Signal Name	Second Function	LVDS Pair/ Polarity
E4	BK0_IO0	-	0P	BK0_IO0	-	0P	NC	-	-
D3	BK0_IO1	-	0N	BK0_IO1	-	0N	NC	-	-
E3	BK0_IO2	HSI0A_SOUTP	1P	BK0_IO2	HSI0A_SOUTP	1P	BK0_IO0	HSI0A_SOUTP	0P
-	GND (Bank 0)	-	-	GND (Bank 0)	-	-	-	-	-
F3	BK0_IO3	HSI0A_SOUTN	1N	BK0_IO3	HSI0A_SOUTN	1N	BK0_IO1	HSI0A_SOUTN	0N
C2	BK0_IO4	-	2P	BK0_IO4	-	2P	BK0_IO2	-	1P
B1	BK0_IO5	-	2N	BK0_IO5	-	2N	BK0_IO3	-	1N
G4	BK0_IO6	HSI0A_SINP	3P	BK0_IO6	HSI0A_SINP	3P	BK0_IO4	HSI0A_SINP	2P
-	-	-	-	-	-	-	GND (Bank 0)	-	-
G3	BK0_IO7	HSI0A_SINN	3N	BK0_IO7	HSI0A_SINN	3N	BK0_IO5	HSI0A_SINN	2N
C1	BK0_IO8	-	4P	BK0_IO8	-	4P	BK0_IO6	-	3P
D2	BK0_IO9	VREF0	4N	BK0_IO9	VREF0	4N	BK0_IO7	VREF0	3N
H4	BK0_IO10	HSI0B_SOUTP	5P	BK0_IO10	HSI0B_SOUTP	5P	BK0_IO8	HSI0B_SOUTP	4P
-	GND (Bank 0)	-	-	GND (Bank 0)	-	-	-	-	-
H3	BK0_IO11	HSI0B_SOUTN	5N	BK0_IO11	HSI0B_SOUTN	5N	BK0_IO9	HSI0B_SOUTN	4N
D1	BK0_IO12	-	6P	BK0_IO12		6P	BK0_IO10	-	5P
E1	BK0_IO13	-	6N	BK0_IO13	-	6N	BK0_IO11	-	5N
E2	BK0_IO14	HSI0B_SINP	7P	BK0_IO14	HSI0B_SINP	7P	BK0_IO12	HSI0B_SINP	6P
-	-	-	-	-	-	-	GND (Bank 0)	-	-
F2	BK0_IO15	HSI0B_SINN	7N	BK0_IO15	HSI0B_SINN	7N	BK0_IO13	HSI0B_SINN	6N
G2	BK0_IO16	-	8P	NC	-	-	NC	-	-
F1	BK0_IO17	-	8N	NC	-	-	NC	-	-
J3	BK0_IO18	HSI1A_SOUTP	9P	NC	-	-	NC	-	-
-	GND (Bank 0)	-	-	-	-	-	-	-	-
K3	BK0_IO19	HSI1A_SOUTN	9N	NC	-	-	NC	-	-
K4	BK0_IO20	-	10P	NC	-	-	NC	-	-
L4	BK0_IO21	-	10N	NC	-	-	NC	-	-
H2	BK0_IO22	HSI1A_SINP	11P	NC	-	-	NC	-	-
J2	BK0_IO23	HSI1A_SINN	11N	NC	-	-	NC	-	-
G1	BK0_IO24	-	12P	NC	-	-	NC	-	-
H1	BK0_IO25	-	12N	NC	-	-	NC	-	-
L3	BK0_IO26	HSI1B_SOUTP	13P	NC	-	-	NC	-	-
-	GND (Bank 0)	-	-	-	-	-	-	-	-
M3	BK0_IO27	HSI1B_SOUTN	13N	NC	-	-	NC	-	-
K2	BK0_IO28	-	14P	NC	-	-	NC	-	-
L2	BK0_IO29	-	14N	NC	-	-	NC	-	-
K1	BK0_IO30	HSI1B_SINP	15P	NC	-	-	NC	-	-
L1	BK0_IO31	HSI1B_SINN	15N	NC	-	-	NC	-	-
M2	BK0_IO32	-	16P	BK0_IO16	-	8P	NC	-	-
M1	BK0_IO33	-	16N	BK0_IO17	-	8N	NC	-	-
N3	BK0_IO34	PLL_FBK0	17P	BK0_IO18	PLL_FBK0	9P	BK0_IO14	PLL_FBK0	7P
-	GND (Bank 0)	-	-	GND (Bank 0)	-	-	-	-	-
N4	BK0_IO35	PLL_RST1	17N	BK0_IO19	PLL_RST1	9N	BK0_IO15	PLL_RST1	7N
N2	BK0_IO36	-	18P	BK0_IO20	-	10P	BK0_IO16	-	8P
N1	BK0_IO37	PLL_FBK1	18N	BK0_IO21	PLL_FBK1	10N	BK0_IO17	PLL_FBK1	8N
P1	BK0_IO38	PLL_RST0	19P	BK0_IO22	PLL_RST0	11P	BK0_IO18	PLL_RST0	9P
-	-	-	-	-	-	-	GND (Bank 0)	-	-
R1	BK0_IO39	-	19N	BK0_IO23	-	11N	BK0_IO19	-	9N
P3	BK0_IO40	CLK_OUT0	20P	BK0_IO24	CLK_OUT0	12P	BK0_IO20	CLK_OUT0	10P
-	GND (Bank 0)	-	-	-	-	-	-	-	-
P2	BK0_IO41	CLK_OUT1	20N	BK0_IO25	CLK_OUT1	12N	BK0_IO21	CLK_OUT1	10N

ispXPGA Logic Signal Connections: 516-Ball fpBGA (Continued)

516-Ball BGA Ball	LFX500			LFX200			LFX125		
	Signal Name	Second Function	LVDS Pair/ Polarity	Signal Name	Second Function	LVDS Pair/ Polarity	Signal Name	Second Function	LVDS Pair/ Polarity
-	-	-	-	GND (Bank 0)	-	-	-	-	-
R2	GCLK0	-	LVDSCLK0	GCLK0	-	LVDSCLK0	GCLK0	-	LVDSCLK0
R3	GCLK1	-	LVDSCLK0	GCLK1	-	LVDSCLK0	GCLK1	-	LVDSCLK0
R4	VCCP0	-	-	VCCP0	-	-	VCCP0	-	-
T4	GNDP0	-	-	GNDP0	-	-	GNDP0	-	-
T3	GCLK2	-	LVDSCLK1	GCLK2	-	LVDSCLK1	GCLK2	-	LVDSCLK1
T2	GCLK3	-	LVDSCLK1	GCLK3	-	LVDSCLK1	GCLK3	-	LVDSCLK1
-	-	-	-	GND (Bank 1)	-	-	-	-	-
T1	BK1_IO0	CLK_OUT2	21P	BK1_IO0	CLK_OUT2	13P	BK1_IO0	CLK_OUT2	11P
-	GND (Bank 1)	-	-	-	-	-	-	-	-
U1	BK1_IO1	CLK_OUT3	21N	BK1_IO1	CLK_OUT3	13N	BK1_IO1	CLK_OUT3	11N
U2	BK1_IO2	SS_CLKOUT0P	22P	BK1_IO2	SS_CLKOUT0P	14P	BK1_IO2	SS_CLKOUT0P	12P
-	-	-	-	-	-	-	GND (Bank 1)	-	-
U3	BK1_IO3	SS_CLKOUT0N	22N	BK1_IO3	SS_CLKOUT0 N	14N	BK1_IO3	SS_CLKOUT0 N	12N
V1	BK1_IO4	PLL_FBK2	23P	BK1_IO4	PLL_FBK2	15P	BK1_IO4	PLL_FBK2	13P
V2	BK1_IO5	PLL_FBK3	23N	BK1_IO5	PLL_FBK3	15N	BK1_IO5	PLL_FBK3	13N
V3	BK1_IO6	-	24P	NC	-	-	NC	-	-
-	GND (Bank 1)	-	-	-	-	-	-	-	-
V4	BK1_IO7	-	24N	NC	-	-	NC	-	-
W1	BK1_IO8	-	25P	NC	-	-	NC	-	-
Y1	BK1_IO9	-	25N	NC	-	-	NC	-	-
W2	BK1_IO10	SS_CLKINOP	26P	BK1_IO6	SS_CLKIN0P	16P	BK1_IO6	SS_CLKIN0P	14P
-	-	-	-	GND (Bank 1)	-	-	-	-	-
W3	BK1_IO11	SS_CLKINON	26N	BK1_IO7	SS_CLKIN0N	16N	BK1_IO7	SS_CLKIN0N	14N
Y2	BK1_IO12	PLL_RST2	27P	BK1_IO8	-	17P	BK1_IO8	-	15P
-	-	-	-	-	-	-	GND (Bank 1)	-	-
Y4	BK1_IO13	PLL_RST3	27N	BK1_IO9	-	17N	BK1_IO9	-	15N
Y3	BK1_IO14	-	28P	NC	-	-	NC	-	-
-	GND (Bank 1)	-	-	-	-	-	-	-	-
AA1	BK1_IO15	-	28N	NC	-	-	NC	-	-
AA2	BK1_IO16	-	29P	NC	-	-	NC	-	-
AA3	BK1_IO17	-	29N	NC	-	-	NC	-	-
AB2	BK1_IO18	HSI2A_SOUTP	30P	BK1_IO10	HSI1A_SOUTP	18P	BK1_IO10	-	16P
AC2	BK1_IO19	HSI2A_SOUTN	30N	BK1_IO11	HSI1A_SOUTN	18N	BK1_IO11	-	16N
AB3	BK1_IO20	PLL_RST2	31P	BK1_IO12	PLL_RST2	19P	BK1_IO12	PLL_RST2	17P
AA4	BK1_IO21	PLL_RST3	31N	BK1_IO13	PLL_RST3	19N	BK1_IO13	PLL_RST3	17N
AC1	BK1_IO22	HSI2A_SINP	32P	BK1_IO14	HSI1A_SINP	20P	NC	-	-
-	GND (Bank 1)	-	-	GND (Bank 1)	-	-	-	-	-
AD1	BK1_IO23	HSI2A_SINN	32N	BK1_IO15	HSI1A_SINN	20N	NC	-	-
AE1	BK1_IO24	VREF1	33P	BK1_IO16	VREF1	21P	BK1_IO14	VREF1	18P
AF1	BK1_IO25	-	33N	BK1_IO17	-	21N	BK1_IO15	-	18N
AC3	BK1_IO26	HSI2B_SOUTP	34P	BK1_IO18	HSI1B_SOUTP	22P	BK1_IO16	-	19P
-	-	-	-	-	-	-	GND (Bank 1)	-	-
AC4	BK1_IO27	HSI2B_SOUTN	34N	BK1_IO19	HSI1B_SOUTN	22N	BK1_IO17	-	19N
AD2	BK1_IO28	-	35P	BK1_IO20	-	23P	BK1_IO18	-	20P
AD3	BK1_IO29	-	35N	BK1_IO21	-	23N	BK1_IO19	-	20N
AE2	BK1_IO30	HSI2B_SINP	36P	BK1_IO22	HSI1B_SINP	24P	BK1_IO20	-	21P
-	GND (Bank 1)	-	-	GND (Bank 1)	-	-	-	-	-
AF2	BK1_IO31	HSI2B_SINN	36N	BK1_IO23	HSI1B_SINN	24N	BK1_IO21	-	21N
AD4	BK1_IO32	-	37P	NC	-	-	NC	-	-

ispXPGA Logic Signal Connections: 516-Ball fpBGA (Continued)

516-Ball BGA Ball	LFX500			LFX200			LFX125		
	Signal Name	Second Function	LVDS Pair/ Polarity	Signal Name	Second Function	LVDS Pair/ Polarity	Signal Name	Second Function	LVDS Pair/ Polarity
AE3	BK1_IO33	-	37N	NC	-	-	NC	-	-
AG1	BK1_IO34	-	38P	NC	-	-	NC	-	-
AH1	BK1_IO35	-	38N	NC	-	-	NC	-	-
AG2	BK1_IO36	-	39P	NC	-	-	NC	-	-
AF3	BK1_IO37	-	39N	NC	-	-	NC	-	-
AJ1	BK1_IO38	-	40P	NC	-	-	NC	-	-
-	GND (Bank 1)	-	-	-	-	-	-	-	-
AH2	BK1_IO39	-	40N	NC	-	-	NC	-	-
AG3	BK1_IO40	-	41P	BK1_IO24	-	25P	NC	-	-
AF4	BK1_IO41	-	41N	BK1_IO25	-	25N	NC	-	-
AK2	TCK	-	-	TCK	-	-	TCK	-	-
AJ3	TMS	-	-	TMS	-	-	TMS	-	-
AG5	TOE	-	-	TOE	-	-	TOE	-	-
AH4	BK2_IO0	-	42P	BK2_IO0	-	26P	BK2_IO0	-	22P
AK3	BK2_IO1	-	42N	BK2_IO1	-	26N	BK2_IO1	-	22N
AJ4	BK2_IO2	-	43P	BK2_IO2	-	27P	BK2_IO2	-	23P
-	GND (Bank 2)	-	-	GND (Bank 2)	-	-	-	-	-
AH5	BK2_IO3	-	43N	BK2_IO3	-	27N	BK2_IO3	-	23N
AK4	BK2_IO4	-	44P	BK2_IO4	-	28P	BK2_IO4	-	24P
-	-	-	-	-	-	-	GND (Bank 2)	-	-
AJ5	BK2_IO5	-	44N	BK2_IO5	-	28N	BK2_IO5	-	24N
AG7	BK2_IO6	-	45P	BK2_IO6	-	29P	BK2_IO6	-	25P
AH6	BK2_IO7	-	45N	BK2_IO7	-	29N	BK2_IO7	-	25N
AK5	BK2_IO8	-	46P	NC	-	-	NC	-	-
AJ6	BK2_IO9	-	46N	NC	-	-	NC	-	-
AG8	BK2_IO10	-	47P	NC	-	-	NC	-	-
-	GND (Bank 2)	-	-	-	-	-	-	-	-
AH7	BK2_IO11	-	47N	NC	-	-	NC	-	-
AK6	BK2_IO12	-	48P	NC	-	-	NC	-	-
AJ7	BK2_IO13	-	48N	NC	-	-	NC	-	-
AH8	BK2_IO14	-	49P	NC	-	-	NC	-	-
AG10	BK2_IO15	-	49N	NC	-	-	NC	-	-
AK7	BK2_IO16	-	50P	NC	-	-	NC	-	-
AJ8	BK2_IO17	-	50N	NC	-	-	NC	-	-
AH9	BK2_IO18	-	51P	NC	-	-	NC	-	-
-	GND (Bank 2)	-	-	-	-	-	-	-	-
AG11	BK2_IO19	-	51N	NC	-	-	NC	-	-
AK8	BK2_IO20	-	52P	BK2_IO8	-	30P	BK2_IO8	-	26P
AJ9	BK2_IO21	VREF2	52N	BK2_IO9	VREF2	30N	BK2_IO9	VREF2	26N
AH10	BK2_IO22	-	53P	BK2_IO10	-	31P	BK2_IO10	-	27P
-	-	-	-	GND (Bank 2)	-	-	-	-	-
AH11	BK2_IO23	-	53N	BK2_IO11	-	31N	BK2_IO11	-	27N
AJ10	BK2_IO24	-	54P	BK2_IO12		32P	BK2_IO12	-	28P
AK10	BK2_IO25	-	54N	BK2_IO13	-	32N	BK2_IO13	-	28N
AH12	BK2_IO26	-	55P	BK2_IO14	-	33P	BK2_IO14	-	29P
-	GND (Bank 2)	-	-	-	-	-	-	-	-
AJ11	BK2_IO27	-	55N	BK2_IO15	-	33N	BK2_IO15	-	29N
AK11	BK2_IO28	-	56P	NC	-	-	NC	-	-
AJ12	BK2_IO29	-	56N	NC	-	-	NC	-	-
AG13	BK2_IO30	-	57P	BK2_IO16	-	34P	BK2_IO16	-	30P
AH13	BK2_IO31	-	57N	BK2_IO17	-	34N	BK2_IO17	-	30N

ispXPGA Logic Signal Connections: 516-Ball fpBGA (Continued)

516-Ball BGA Ball	LFX500			LFX200			LFX125		
	Signal Name	Second Function	LVDS Pair/ Polarity	Signal Name	Second Function	LVDS Pair/ Polarity	Signal Name	Second Function	LVDS Pair/ Polarity
AJ13	BK2_IO32	-	58P	BK2_IO18	-	35P	BK2_IO18	-	31P
-	-	-	-	GND (Bank 2)	-	-	GND (Bank 2)	-	-
AK12	BK2_IO33	-	58N	BK2_IO19	-	35N	BK2_IO19	-	31N
AK13	BK2_IO34	-	59P	BK2_IO20	-	36P	BK2_IO20	-	32P
-	GND (Bank 2)	-	-	-	-	-	-	-	-
AH14	BK2_IO35	-	59N	BK2_IO21	-	36N	BK2_IO21	-	32N
AJ14	BK2_IO36	-	60P	BK2_IO22	-	37P	NC	-	-
AK14	BK2_IO37	-	60N	BK2_IO23	-	37N	NC	-	-
AG15	BK2_IO38	-	61P	BK2_IO24	-	38P	NC	-	-
AH15	BK2_IO39	-	61N	BK2_IO25	-	38N	NC	-	-
AJ15	BK2_IO40	-	62P	NC	-	-	NC	-	-
AK15	BK2_IO41	-	62N	NC	-	-	NC	-	-
-	GND (Bank 2)	-	-	GND (Bank 2)	-	-	-	-	-
-	GND (Bank 3)	-	-	GND (Bank 3)	-	-	-	-	-
AK16	BK3_IO0	-	63P	BK3_IO0	-	39P	BK3_IO0	-	33P
AJ16	BK3_IO1	-	63N	BK3_IO1	-	39N	BK3_IO1	-	33N
AH16	BK3_IO2	-	64P	BK3_IO2	-	40P	BK3_IO2	-	34P
AG16	BK3_IO3	-	64N	BK3_IO3	-	40N	BK3_IO3	-	34N
AK17	BK3_IO4	-	65P	BK3_IO4	-	41P	BK3_IO4	-	35P
AJ17	BK3_IO5	-	65N	BK3_IO5	-	41N	BK3_IO5	-	35N
AH17	BK3_IO6	-	66P	BK3_IO6	-	42P	BK3_IO6	-	36P
-	GND (Bank 3)	-	-	GND (Bank 3)	-	-	-	-	-
AJ18	BK3_IO7	-	66N	BK3_IO7	-	42N	BK3_IO7	-	36N
AH18	BK3_IO8	-	67P	BK3_IO8	-	43P	BK3_IO8	-	37P
-	-	-	-	-	-	-	GND (Bank 3)	-	-
AG18	BK3_IO9	-	67N	BK3_IO9	-	43N	BK3_IO9	-	37N
AK18	BK3_IO10	-	68P	BK3_IO10	-	44P	BK3_IO10	-	38P
AK19	BK3_IO11	-	68N	BK3_IO11	-	44N	BK3_IO11	-	38N
AJ19	BK3_IO12	-	69P	BK3_IO12	-	45P	NC	-	-
AH19	BK3_IO13	-	69N	BK3_IO13		45N	NC	-	-
AK20	BK3_IO14	-	70P	BK3_IO14	-	46P	NC	-	-
-	GND (Bank 3)	-	-	GND (Bank 3)	-	-	-	-	-
AJ20	BK3_IO15	-	70N	BK3_IO15	-	46N	NC	-	-
AH20	BK3_IO16	-	71P	NC	-	-	NC	-	-
AG20	BK3_IO17	-	71N	NC	-	-	NC	-	-
AK21	BK3_IO18	-	72P	NC	-	-	NC	-	-
AJ21	BK3_IO19	-	72N	NC	-	-	NC	-	-
AH21	BK3_IO20	VREF3	73P	BK3_IO16	VREF3	47P	BK3_IO12	VREF3	39P
AG21	BK3_IO21	-	73N	BK3_IO17	-	47N	BK3_IO13	-	39N
AJ22	BK3_IO22	-	74P	BK3_IO18	-	48P	BK3_IO14	-	40P
-	GND (Bank 3)	-	-	-	-	-	-	-	-
AH22	BK3_IO23	-	74N	BK3_IO19	-	48N	BK3_IO15	-	40N
AK23	BK3_IO24	-	75P	NC	-	-	NC	-	-
AJ23	BK3_IO25	-	75N	NC	-	-	NC	-	-
AH23	BK3_IO26	-	76P	NC	-	-	NC	-	-
AK24	BK3_IO27	-	76N	NC	-	-	NC	-	-
AJ24	BK3_IO28	-	77P	NC	-	-	NC	-	-
AG23	BK3_IO29	-	77N	NC	-	-	NC	-	-
AH24	BK3_IO30	-	78P	NC	-	-	NC	-	-
-	GND (Bank 3)	-	-		-	-	-	-	-
AK25	BK3_IO31	-	78N	NC	-	-	NC	-	-

ispXPGA Logic Signal Connections: 516-Ball fpBGA (Continued)

516-Ball BGA Ball	LFX500			LFX200			LFX125		
	Signal Name	Second Function	LVDS Pair/ Polarity	Signal Name	Second Function	LVDS Pair/ Polarity	Signal Name	Second Function	LVDS Pair/ Polarity
AJ25	BK3_IO32	-	79P	NC	-	-	NC	-	-
AG24	BK3_IO33	-	79N	NC	-	-	NC	-	-
AK26	BK3_IO34	-	80P	BK3_IO20	-	49P	BK3_IO16	-	41P
-	-	-	-	-	-	-	GND (Bank 3)	-	-
AH25	BK3_IO35	-	80N	BK3_IO21	-	49N	BK3_IO17	-	41N
AJ26	BK3_IO36	-	81P	BK3_IO22	-	50P	BK3_IO18	-	42P
-	-	-	-	GND (Bank 3)	-	-	-	-	-
AH26	BK3_IO37	-	81N	BK3_IO23	-	50N	BK3_IO19	-	42N
AK27	BK3_IO38	-	82P	NC	-	-	NC	-	-
-	GND (Bank 3)	-	-	-	-	-	-	-	-
AJ27	BK3_IO39	-	82N	NC	-	-	NC	-	-
AG26	BK3_IO40	-	83P	BK3_IO24	-	51P	BK3_IO20	-	43P
AH27	BK3_IO41	-	83N	BK3_IO25	-	51N	BK3_IO21	-	43N
AK28	RESET	-	-	RESET	-	-	RESET	-	-
AJ28	DXP	-	-	DXP	-	-	DXP	-	-
AK29	DXN	-	-	DXN	-	-	DXN	-	-
AH29	BK4_IO0	-	84P	BK4_IO0	-	52P	BK4_IO0	-	44P
AG28	BK4_IO1	-	84N	BK4_IO1	-	52N	BK4_IO1	-	44N
AF27	BK4_IO2	-	85P	NC	-	-	NC	-	-
-	GND (Bank 4)	-	-	-	-	-	-	-	-
AF28	BK4_IO3	-	85N	NC	-	-	NC	-	-
AJ30	BK4_IO4	-	86P	NC	-	-	NC	-	-
AH30	BK4_IO5	-	86N	NC	-	-	NC	-	-
AG29	BK4_IO6	-	87P	NC	-	-	NC	-	-
AF29	BK4_IO7	-	87N	NC	-	-	NC	-	-
AE28	BK4_IO8	-	88P	NC	-	-	NC	-	-
AD27	BK4_IO9	-	88N	NC	-	-	NC	-	-
AG30	BK4_IO10	HSI3A_SINP	89P	BK4_IO2	HSI2A_SINP	53P	BK4_IO2	-	45P
-	GND (Bank 4)	-	-	GND (Bank 4)	-	-	-	-	-
AF30	BK4_IO11	HSI3A_SINN	89N	BK4_IO3	HSI2A_SINN	53N	BK4_IO3	-	45N
AD28	BK4_IO12	-	90P	BK4_IO4	-	54P	BK4_IO4	-	46P
-	-	-	-	-	-	-	GND (Bank 4)	-	-
AC27	BK4_IO13	-	90N	BK4_IO5	-	54N	BK4_IO5	-	46N
AE29	BK4_IO14	HSI3A_SOUTP	91P	BK4_IO6	HSI2A_SOUTP	55P	NC	-	-
AE30	BK4_IO15	HSI3A_SOUTN	91N	BK4_IO7	HSI2A_SOUTN	55N	NC	-	-
AD29	BK4_IO16	-	92P	BK4_IO8	-	56P	BK4_IO6	-	47P
AD30	BK4_IO17	VREF4	92N	BK4_IO9	VREF4	56N	BK4_IO7	VREF4	47N
AC28	BK4_IO18	HSI3B_SINP	93P	BK4_IO10	HSI2B_SINP	57P	NC	-	-
-	GND (Bank 4)	-	-	GND (Bank 4)	-	-	-	-	-
AB28	BK4_IO19	HSI3B_SINN	93N	BK4_IO11	HSI2B_SINN	57N	NC	-	-
AA27	BK4_IO20	PLL_RST4	94P	BK4_IO12	PLL_RST4	58P	BK4_IO8	PLL_RST4	48P
AB29	BK4_IO21	PLL_RST5	94N	BK4_IO13	PLL_RST5	58N	BK4_IO9	PLL_RST5	48N
AC29	BK4_IO22	HSI3B_SOUTP	95P	BK4_IO14	HSI2B_SOUTP	59P	BK4_IO10	-	49P
AC30	BK4_IO23	HSI3B_SOUTN	95N	BK4_IO15	HSI2B_SOUTN	59N	BK4_IO11	-	49N
AA28	BK4_IO24	-	96P	NC	-	-	NC	-	-
Y27	BK4_IO25	-	96N	NC	-	-	NC	-	-
Y28	BK4_IO26	-	97P	NC	-	-	NC	-	-
-	GND (Bank 4)	-	-	-	-	-	-	-	-
AA29	BK4_IO27	-	97N	NC	-	-	NC	-	-
Y29	BK4_IO28	-	98P	BK4_IO16	-	60P	BK4_IO12	-	50P
-	-	-	-	-	-	-	GND (Bank 4)	-	-

ispXPGA Logic Signal Connections: 516-Ball fpBGA (Continued)

516-Ball BGA Ball	LFX500			LFX200			LFX125		
	Signal Name	Second Function	LVDS Pair/ Polarity	Signal Name	Second Function	LVDS Pair/ Polarity	Signal Name	Second Function	LVDS Pair/ Polarity
AA30	BK4_IO29	-	98N	BK4_IO17	-	60N	BK4_IO13	-	50N
W28	BK4_IO30	SS_CLKIN1P	99P	BK4_IO18	SS_CLKIN1P	61P	BK4_IO14	SS_CLKIN1P	51P
-	-	-	-	GND (Bank 4)	-	-	-	-	-
W29	BK4_IO31	SS_CLKIN1N	99N	BK4_IO19	SS_CLKIN1N	61N	BK4_IO15	SS_CLKIN1N	51N
Y30	BK4_IO32	-	100P	NC	-	-	NC	-	-
W30	BK4_IO33	-	100N	NC	-	-	NC	-	-
V27	BK4_IO34	-	101P	NC	-	-	NC	-	-
-	GND (Bank 4)	-	-	-	-	-	-	-	-
V28	BK4_IO35	-	101N	NC	-	-	NC	-	-
V29	BK4_IO36	PLL_FBK4	102P	BK4_IO20	PLL_FBK4	62P	BK4_IO16	PLL_FBK4	52P
V30	BK4_IO37	PLL_FBK5	102N	BK4_IO21	PLL_FBK5	62N	BK4_IO17	PLL_FBK5	52N
U30	BK4_IO38	SS_CLKOUT1P	103P	BK4_IO22	SS_CLKOUT1P	63P	BK4_IO18	SS_CLKOUT1P	53P
U29	BK4_IO39	SS_CLKOUT1N	103N	BK4_IO23	SS_CLKOUT1N	63N	BK4_IO19	SS_CLKOUT1N	53N
U28	BK4_IO40	CLK_OUT4	104P	BK4_IO24	CLK_OUT4	64P	BK4_IO20	CLK_OUT4	54P
-	GND (Bank 4)	-	-	-	-	-	-	-	-
T27	BK4_IO41	CLK_OUT5	104N	BK4_IO25	CLK_OUT5	64N	BK4_IO21	CLK_OUT5	54N
-	-	-	-	GND (Bank 4)	-	-	-	-	-
T28	GCLK4	-	LVDSCLK2	GCLK4	-	LVDSCLK2	GCLK4	-	LVDSCLK2
T29	GCLK5	-	LVDSCLK2	GCLK5	-	LVDSCLK2	GCLK5	-	LVDSCLK2
T30	VCCP1	-	-	VCCP1	-	-	VCCP1	-	-
R29	GNDP1	-	-	GNDP1	-	-	GNDP1	-	-
R28	GCLK6	-	LVDSCLK3	GCLK6	-	LVDSCLK3	GCLK6	-	LVDSCLK3
R27	GCLK7	-	LVDSCLK3	GCLK7	-	LVDSCLK3	GCLK7	-	LVDSCLK3
-	-	-	-	GND (Bank 5)	-	-	-	-	-
R30	BK5_IO0	CLK_OUT6	105P	BK5_IO0	CLK_OUT6	65P	BK5_IO0	CLK_OUT6	55P
-	GND (Bank 5)	-	-	-	-	-	-	-	-
P30	BK5_IO1	CLK_OUT7	105N	BK5_IO1	CLK_OUT7	65N	BK5_IO1	CLK_OUT7	55N
P29	BK5_IO2	-	106P	BK5_IO2	-	66P	BK5_IO2	-	56P
-	-	-	-	-	-	-	GND (Bank 5)	-	-
P28	BK5_IO3	PLL_RST7	106N	BK5_IO3	PLL_RST7	66N	BK5_IO3	PLL_RST7	56N
N30	BK5_IO4	PLL_FBK6	107P	BK5_IO4	PLL_FBK6	67P	BK5_IO4	PLL_FBK6	57P
N29	BK5_IO5	-	107N	BK5_IO5	-	67N	BK5_IO5	-	57N
N28	BK5_IO6	PLL-RST6	108P	BK5_IO6	PLL_RST6	68P	BK5_IO6	PLL_RST6	58P
-	GND (Bank 5)	-	-	GND (Bank 5)	-	-	-	-	-
N27	BK5_IO7	PLL_FBK7	108N	BK5_IO7	PLL_FBK7	68N	BK5_IO7	PLL_FBK7	58N
M30	BK5_IO8	-	109P	BK5_IO8	-	69P	NC	-	-
M29	BK5_IO9	-	109N	BK5_IO9	-	69N	NC	-	-
L30	BK5_IO10	HSI4A_SINP	110P	BK5_IO10	HSI3A_SINP	70P	BK5_IO8	HSI1A_SINP	59P
-	-	-	-	-	-	-	GND (Bank 5)	-	-
L29	BK5_IO11	HSI4A_SINN	110N	BK5_IO11	HSI3A_SINN	70N	BK5_IO9	HSI1A_SINN	59N
M28	BK5_IO12	-	111P	BK5_IO12	-	71P	BK5_IO10	-	60P
L28	BK5_IO13	-	111N	BK5_IO13		71N	BK5_IO11	-	60N
K30	BK5_IO14	HSI4A_SOUTP	112P	BK5_IO14	HSI3A_SOUTP	72P	BK5_IO12	HSI1A_SOUTP	61P
-	GND (Bank 5)	-	-	GND (Bank 5)	-	-	-	-	-
K29	BK5_IO15	HSI4A_SOUTN	112N	BK5_IO15	HSI3A_SOUTN	72N	BK5_IO13	HSI1A_SOUTN	61N
L27	BK5_IO16	-	113P	NC	-	-	NC	-	-
K28	BK5_IO17	-	113N	NC	-	-	NC	-	-
H30	BK5_IO18	HSI4B_SINP	114P	NC	-	-	NC	-	-
G30	BK5_IO19	HSI4B_SINN	114N	NC	-	-	NC	-	-
J28	BK5_IO20	-	115P	NC	-	-	NC	-	-
K27	BK5_IO21	-	115N	NC	-	-	NC	-	-

ispXPGA Logic Signal Connections: 516-Ball fpBGA (Continued)

516-Ball BGA Ball	LFX500			LFX200			LFX125		
	Signal Name	Second Function	LVDS Pair/ Polarity	Signal Name	Second Function	LVDS Pair/ Polarity	Signal Name	Second Function	LVDS Pair/ Polarity
J29	BK5_IO22	HSI4B_SOUTP	116P	NC	-	-	NC	-	-
-	GND (Bank 5)	-	-	-	-	-	-	-	-
H29	BK5_IO23	HSI4B_SOUTN	116N	NC	-	-	NC	-	-
F30	BK5_IO24	-	117P	NC	-	-	NC	-	-
G29	BK5_IO25	-	117N	NC	-	-	NC	-	-
H28	BK5_IO26	HSI5A_SINP	118P	NC	-	-	NC	-	-
H27	BK5_IO27	HSI5A_SINN	118N	NC	-	-	NC	-	-
E30	BK5_IO28	-	119P	NC	-	-	NC	-	-
F29	BK5_IO29	-	119N	NC	-	-	NC	-	-
G28	BK5_IO30	HSI5A_SOUTP	120P	NC	-	-	NC	-	-
-	GND (Bank 5)	-	-	-	-	-	-	-	-
G27	BK5_IO31	HSI5A_SOUTN	120N	NC	-	-	NC	-	-
E29	BK5_IO32	VREF5	121P	BK5_IO16	VREF5	73P	BK5_IO14	VREF5	62P
F28	BK5_IO33	-	121N	BK5_IO17	-	73N	BK5_IO15	-	62N
D30	BK5_IO34	HSI5B_SINP	122P	BK5_IO18	HSI3B_SINP	74P	BK5_IO16	HSI1B_SINP	63P
-	-	-	-	-	-	-	GND (Bank 5)	-	-
C30	BK5_IO35	HSI5B_SINN	122N	BK5_IO19	HSI3B_SINN	74N	BK5_IO17	HSI1B_SINN	63N
D29	BK5_IO36	-	123P	BK5_IO20		75P	NC	-	-
D28	BK5_IO37	-	123N	BK5_IO21		75N	NC	-	-
E28	BK5_IO38	HSI5B_SOUTP	124P	BK5_IO22	HSI3B_SOUTP	76P	BK5_IO20	HSI1B_SOUTP	65P
-	GND (Bank 5)	-	-	GND (Bank 5)	-	-	-	-	-
E27	BK5_IO39	HSI5B_SOUTN	124N	BK5_IO23	HSI3B_SOUTN	76N	BK5_IO21	HSI1B_SOUTN	65N
C29	BK5_IO40	-	125P	BK5_IO24	-	77P	BK5_IO18	-	64P
B30	BK5_IO41	-	125N	BK5_IO25	-	77N	BK5_IO19	-	64N
A29	CFG0	-	-	CFG0	-	-	CFG0	-	-
B28	DONE	-	-	DONE	-	-	DONE	-	-
A28	PROGRAMb	-	-	PROGRAMb	-	-	PROGRAMb	-	-
D26	BK6_IO0	INITb	126P	BK6_IO0	INITb	78P	BK6_IO0	INITb	66P
C27	BK6_IO1	CCLK	126N	BK6_IO1	CCLK	78N	BK6_IO1	CCLK	66N
B27	BK6_IO2	-	127P	BK6_IO2	-	79P	BK6_IO2	-	67P
-	GND (Bank 6)	-	-	GND (Bank 6)	-	-	-	-	-
A27	BK6_IO3	-	127N	BK6_IO3	-	79N	BK6_IO3	-	67N
C26	BK6_IO4	CSb	128P	BK6_IO4	CSb	80P	BK6_IO4	CSb	68P
-	-	-	-	-	-	-	GND (Bank 6)	-	-
B26	BK6_IO5	Read	128N	BK6_IO5	Read	80N	BK6_IO5	Read	68N
A26	BK6_IO6	-	129P	NC	-	-	NC	-	-
C25	BK6_IO7	-	129N	NC	-	-	NC	-	-
D24	BK6_IO8	-	130P	NC	-	-	NC	-	-
B25	BK6_IO9	-	130N	NC	-	-	NC	-	-
A25	BK6_IO10	-	131P	NC	-	-	NC	-	-
-	GND (Bank 6)	-	-	-	-	-	-	-	-
C24	BK6_IO11	-	131N	NC	-	-	NC	-	-
D23	BK6_IO12	-	132P	NC	-	-	NC	-	-
B24	BK6_IO13	-	132N	NC	-	-	NC	-	-
C23	BK6_IO14	-	133P	NC	-	-	NC	-	-
A24	BK6_IO15	-	133N	NC	-	-	NC	-	-
C22	BK6_IO16	-	134P	NC	-	-	NC	-	-
B23	BK6_IO17	-	134N	NC	-	-	NC	-	-
B22	BK6_IO18	DATA7	135P	BK6_IO6	DATA7	81P	BK6_IO6	DATA7	69P
-	GND (Bank 6)	-	-	-	-	-	-	-	-
A23	BK6_IO19	DATA6	135N	BK6_IO7	DATA6	81N	BK6_IO7	DATA6	69N

ispXPGA Logic Signal Connections: 516-Ball fpBGA (Continued)

516-Ball BGA Ball	LFX500			LFX200			LFX125		
	Signal Name	Second Function	LVDS Pair/ Polarity	Signal Name	Second Function	LVDS Pair/ Polarity	Signal Name	Second Function	LVDS Pair/ Polarity
D21	BK6_IO20	-	136P	BK6_IO8	-	82P	BK6_IO8	-	70P
C21	BK6_IO21	VREF6	136N	BK6_IO9	VREF6	82N	BK6_IO9	VREF6	70N
B21	BK6_IO22	DATA5	137P	BK6_IO10	DATA5	83P	BK6_IO10	DATA5	71P
-	-	-	-	GND (Bank 6)	-	-	-	-	-
A21	BK6_IO23	DATA4	137N	BK6_IO11	DATA4	83N	BK6_IO11	DATA4	71N
D20	BK6_IO24	-	138P	BK6_IO12	-	84P	BK6_IO12	-	72P
-	-	-	-	-	-	-	GND (Bank 6)	-	-
C20	BK6_IO25	-	138N	BK6_IO13	-	84N	BK6_IO13	-	72N
B20	BK6_IO26	DATA3	139P	BK6_IO14	DATA3	85P	BK6_IO14	DATA3	73P
-	GND (Bank 6)	-	-	-	-	-	-	-	-
A20	BK6_IO27	DATA2	139N	BK6_IO15	DATA2	85N	BK6_IO15	DATA2	73N
C19	BK6_IO28	-	140P	BK6_IO16		86P	BK6_IO16	-	74P
B19	BK6_IO29	-	140N	BK6_IO17		86N	BK6_IO17	-	74N
A19	BK6_IO30	DATA1	141P	BK6_IO18	DATA1	87P	BK6_IO18	DATA1	75P
-	-	-	-	GND (Bank 6)	-	-	GND (Bank 6)	-	-
A18	BK6_IO31	DATA0	141N	BK6_IO19	DATA0	87N	BK6_IO19	DATA0	75N
D18	BK6_IO32	-	142P	BK6_IO20		88P	BK6_IO20	-	76P
C18	BK6_IO33	-	142N	BK6_IO21		88N	BK6_IO21	-	76N
B18	BK6_IO34	-	143P	BK6_IO22		89P	NC	-	-
-	GND (Bank 6)	-	-	-	-	-	-	-	-
C17	BK6_IO35	-	143N	BK6_IO23		89N	NC	-	-
B17	BK6_IO36	-	144P	NC	-	-	NC	-	-
A17	BK6_IO37	-	144N	NC	-	-	NC	-	-
D16	BK6_IO38	-	145P	NC	-	-	NC	-	-
C16	BK6_IO39	-	145N	NC	-	-	NC	-	-
B16	BK6_IO40	-	146P	BK6_IO24	-	90P	NC	-	-
A16	BK6_IO41	-	146N	BK6_IO25	-	90N	NC	-	-
-	GND (Bank 6)	-	-	GND (Bank 6)	-	-	-	-	-
-	GND (Bank 7)	-	-	GND (Bank 7)	-	-	-	-	-
A15	BK7_IO0	-	147P	BK7_IO0	-	91P	BK7_IO0	-	77P
B15	BK7_IO1	-	147N	BK7_IO1	-	91N	BK7_IO1	-	77N
C15	BK7_IO2	-	148P	BK7_IO2	-	92P	BK7_IO2	-	78P
-	-	-	-	-	-	-	GND (Bank 7)	-	-
D15	BK7_IO3	-	148N	BK7_IO3	-	92N	BK7_IO3	-	78N
A14	BK7_IO4	-	149P	BK7_IO4	-	93P	BK7_IO4	-	79P
B14	BK7_IO5	-	149N	BK7_IO5	-	93N	BK7_IO5	-	79N
C14	BK7_IO6	-	150P	BK7_IO6	-	94P	NC	-	-
-	GND (Bank 7)	-	-	GND (Bank 7)	-	-	-	-	-
A13	BK7_IO7	-	150N	BK7_IO7	-	94N	NC	-	-
B13	BK7_IO8	-	151P	BK7_IO8	-	95P	NC	-	-
C13	BK7_IO9	-	151N	BK7_IO9	-	95N	NC	-	-
D13	BK7_IO10	-	152P	BK7_IO10	-	96P	BK7_IO6	-	80P
B12	BK7_IO11	-	152N	BK7_IO11	-	96N	BK7_IO7	-	80N
C12	BK7_IO12	-	153P	BK7_IO12	-	97P	BK7_IO8	-	81P
-	-	-	-	-	-	-	GND (Bank 7)	-	-
A12	BK7_IO13	-	153N	BK7_IO13		97N	BK7_IO9	-	81N
A11	BK7_IO14	-	154P	BK7_IO14	-	98P	BK7_IO10	-	82P
-	GND (Bank 7)	-	-	GND (Bank 7)	-	-	-	-	-
B11	BK7_IO15	-	154N	BK7_IO15	-	98N	BK7_IO11	-	82N
C11	BK7_IO16	-	155P	NC	-	-	NC	-	-
D11	BK7_IO17	-	155N	NC	-	-	NC	-	-

ispXPGA Logic Signal Connections: 516-Ball fpBGA (Continued)

516-Ball BGA Ball	LFX500			LFX200			LFX125		
	Signal Name	Second Function	LVDS Pair/ Polarity	Signal Name	Second Function	LVDS Pair/ Polarity	Signal Name	Second Function	LVDS Pair/ Polarity
A10	BK7_IO18	-	156P	NC	-	-	NC	-	-
B10	BK7_IO19	-	156N	NC	-	-	NC	-	-
C10	BK7_IO20	VREF7	157P	BK7_IO16	VREF7	99P	BK7_IO12	VREF7	83P
D10	BK7_IO21	-	157N	BK7_IO17	-	99N	BK7_IO13	-	83N
B9	BK7_IO22	-	158P	BK7_IO18	-	100P	BK7_IO14	-	84P
-	GND (Bank 7)	-	-	-	-	-	-	-	-
C9	BK7_IO23	-	158N	BK7_IO19	-	100N	BK7_IO15	-	84N
A8	BK7_IO24	-	159P	BK7_IO20	-	101P	BK7_IO16	-	85P
-	-	-	-	-	-	-	GND (Bank 7)	-	-
B8	BK7_IO25	-	159N	BK7_IO21	-	101N	BK7_IO17	-	85N
C8	BK7_IO26	-	160P	NC	-	-	NC	-	-
D8	BK7_IO27	-	160N	NC	-	-	NC	-	-
A7	BK7_IO28	-	161P	NC	-	-	NC	-	-
B7	BK7_IO29	-	161N	NC	-	-	NC	-	-
C7	BK7_IO30	-	162P	NC	-	-	NC	-	-
-	GND (Bank 7)	-	-	-	-	-	-	-	-
D7	BK7_IO31	-	162N	NC	-	-	NC	-	-
A6	BK7_IO32	-	163P	NC	-	-	NC	-	-
B6	BK7_IO33	-	163N	NC	-	-	NC	-	-
B5	BK7_IO34	-	164P	NC	-	-	NC	-	-
C6	BK7_IO35	-	164N	NC	-	-	NC	-	-
A5	BK7_IO36	-	165P	NC	-	-	NC	-	-
A4	BK7_IO37	-	165N	NC	-	-	NC	-	-
B4	BK7_IO38	-	166P	BK7_IO22	-	102P	BK7_IO18	-	86P
-	GND (Bank 7)	-	-	GND (Bank 7)	-	-	-	-	-
C5	BK7_IO39	-	166N	BK7_IO23	-	102N	BK7_IO19	-	86N
A3	BK7_IO40	-	167P	BK7_IO24	-	103P	BK7_IO20	-	87P
A2	BK7_IO41	-	167N	BK7_IO25	-	103N	BK7_IO21	-	87N
D5	TDO	-	-	TDO	-	-	TDO	-	-
C4	VCCJ	-	-	VCCJ	-	-	VCCJ	-	-
B3	TDI	-	-	TDI	-	-	TDI	-	-

ispXPGA Logic Signal Connections: 680-Ball fpBGA

LFX1200			
680-Ball fpBGA	**Signal Name**	**Second Function**	**LVDS Pair Polarity**
C4	BK0_IO0	-	0P
B4	BK0_IO1	-	0N
E6	BK0_IO2	-	1P
-	GND (Bank 0)	-	
D6	BK0_IO3	-	1N
A4	BK0_IO4	-	2P
E8	BK0_IO5	-	2N
C5	BK0_IO6	HSI0A_SOUTP	3P
C6	BK0_IO7	HSI0A_SOUTN	3N
A6	BK0_IO8	-	4P
A5	BK0_IO9	-	4N
B6	BK0_IO10	HSI0A_SINP	5P
-	GND (Bank 0)	-	-
B5	BK0_IO11	HSI0A_SINN	5N
B7	BK0_IO12	VREF0	6P
A7	BK0_IO13	-	6N
D8	BK0_IO14	HSI0B_SOUTP	7P
D7	BK0_IO15	HSI0B_SOUTN	7N
D9	BK0_IO16	-	8P
E10	BK0_IO17	-	8N
C8	BK0_IO18	HSI0B_SINP	9P
-	GND (Bank 0)	-	-
C7	BK0_IO19	HSI0B_SINN	9N
A8	BK0_IO20	-	10P
A9	BK0_IO21	-	10N
C9	BK0_IO22	HSI1A_SOUTP	11P
B8	BK0_IO23	HSI1A_SOUTN	11N
B9	BK0_IO24	-	12P
B10	BK0_IO25	-	12N
D11	BK0_IO26	HSI1A_SINP	13P
-	GND (Bank 0)	-	-
D10	BK0_IO27	HSI1A_SINN	13N
A10	BK0_IO28	-	14P
C12	BK0_IO29	-	14N
D12	BK0_IO30	HSI1B_SOUTP	15P
C11	BK0_IO31	HSI1B_SOUTN	15N
A12	BK0_IO32	-	16P
A13	BK0_IO33	-	16N
B13	BK0_IO34	HSI1B_SINP	17P
-	GND (Bank 0)	-	-
B12	BK0_IO35	HSI1B_SINN	17N
E14	BK0_IO36	-	18P

ispXPGA Logic Signal Connections: 680-Ball fpBGA (Continued)

LFX1200			
680-Ball fpBGA	**Signal Name**	**Second Function**	**LVDS Pair Polarity**
D14	BK0_IO37	-	18N
C13	BK0_IO38	HSI2A_SOUTP	19P
D13	BK0_IO39	HSI2A_SOUTN	19N
B14	BK0_IO40	-	20P
A14	BK0_IO41	-	20N
C15	BK0_IO42	HSI2A_SINP	21P
-	GND (Bank 0)	-	-
D15	BK0_IO43	HSI2A_SINN	21N
A15	BK0_IO44	-	22P
C16	BK0_IO45	-	22N
B15	BK0_IO46	HSI2B_SOUTP	23P
B16	BK0_IO47	HSI2B_SOUTN	23N
A16	BK0_IO48	-	24P
B17	BK0_IO49	-	24N
D16	BK0_IO50	HSI2B_SINP	25P
-	GND (Bank 0)	-	-
E16	BK0_IO51	HSI2B_SINN	25N
D17	BK0_IO52	-	26P
C17	BK0_IO53	-	26N
A18	BK0_IO54	PLL_RST0	27P
D18	BK0_IO55	PLL_RST1	27N
A17	BK0_IO56	-	28P
E19	BK0_IO57	-	28N
A19	BK0_IO58	PLL_FBK0	29P
-	GND (Bank 0)	-	-
B19	BK0_IO59	PLL_FBK1	29N
C18	BK0_IO60	CLK_OUT0	30P
B18	BK0_IO61	CLK_OUT1	30N
-	GND (Bank 0)	-	-
D19	GCLK0	-	LVDSCLK0
C19	GCLK1	-	LVDSCLK0
E20	VCCP0	-	-
A21	GNDP0	-	-
B21	GCLK2	-	LVDSCLK1
C21	GCLK3	-	LVDSCLK1
B23	BK1_IO0	CLK_OUT2	31P
C23	BK1_IO1	CLK_OUT3	31N
B22	BK1_IO2	SS_CLKOUT0P	32P
-	GND (Bank 1)	-	-
C22	BK1_IO3	SS_CLKOUT0N	32N
D21	BK1_IO4	PLL_FBK2	33P
E21	BK1_IO5	PLL_FBK3	33N
B24	BK1_IO6	SS_CLKIN0P	34P

ispXPGA Logic Signal Connections: 680-Ball fpBGA (Continued)

LFX1200			
680-Ball fpBGA	**Signal Name**	**Second Function**	**LVDS Pair Polarity**
C24	BK1_IO7	SS_CLKIN0N	34N
A22	BK1_IO8	-	35P
D22	BK1_IO9	-	35N
A23	BK1_IO10	-	36P
-	GND (Bank 1)	-	-
B25	BK1_IO11	-	36N
D23	BK1_IO12	PLL_RST2	37P
A24	BK1_IO13	PLL_RST3	37N
A25	BK1_IO14	-	38P
E24	BK1_IO15	-	38N
D24	BK1_IO16	-	39P
A26	BK1_IO17	-	39N
D25	BK1_IO18	-	40P
-	GND (Bank 1)	-	-
C25	BK1_IO19	-	40N
B26	BK1_IO20	-	41P
B27	BK1_IO21	-	41N
D26	BK1_IO22	-	42P
A27	BK1_IO23	-	42N
A28	BK1_IO24	-	43P
E26	BK1_IO25	-	43N
C27	BK1_IO26	HSI3A_SOUTP	44P
-	GND (Bank 1)	-	-
D27	BK1_IO27	HSI3A_SOUTN	44N
B28	BK1_IO28	-	45P
A30	BK1_IO29	-	45N
C28	BK1_IO30	HSI3A_SINP	46P
D28	BK1_IO31	HSI3A_SINN	46N
A31	BK1_IO32	-	47P
B30	BK1_IO33	-	47N
E28	BK1_IO34	HSI3B_SOUTP	48P
-	GND (Bank 1)	-	-
D29	BK1_IO35	HSI3B_SOUTN	48N
C29	BK1_IO36	-	49P
B31	BK1_IO37	-	49N
D30	BK1_IO38	HSI3B_SINP	50P
E30	BK1_IO39	HSI3B_SINN	50N
A32	BK1_IO40	-	51P
C31	BK1_IO41	-	51N
D31	BK1_IO42	HSI4A_SOUTP	52P
-	GND (Bank 1)	-	-
C32	BK1_IO43	HSI4A_SOUTN	52N
B32	BK1_IO44	-	53P

ispXPGA Logic Signal Connections: 680-Ball fpBGA (Continued)

LFX1200			
680-Ball fpBGA	**Signal Name**	**Second Function**	**LVDS Pair Polarity**
A33	BK1_IO45	-	53N
C33	BK1_IO46	HSI4A_SINP	54P
B33	BK1_IO47	HSI4A_SINN	54N
A34	BK1_IO48	-	55P
A35	BK1_IO49	VREF1	55N
D32	BK1_IO50	HSI4B_SOUTP	56P
-	GND (Bank 1)	-	-
D33	BK1_IO51	HSI4B_SOUTN	56N
E32	BK1_IO52	-	57P
C34	BK1_IO53	-	57N
B34	BK1_IO54	HSI4B_SINP	58P
B35	BK1_IO55	HSI4B_SINN	58N
A36	BK1_IO56	-	59P
D34	BK1_IO57	-	59N
C35	BK1_IO58	-	60P
-	GND (Bank 1)	-	-
E34	BK1_IO59	-	60N
B36	BK1_IO60	-	61P
C36	BK1_IO61	-	61N
D39	TCK	-	-
D37	TMS	-	-
D38	TOE	-	-
E37	BK2_IO0	-	62P
F35	BK2_IO1	-	62N
E39	BK2_IO2	-	63P
-	GND (Bank 2)	-	-
F39	BK2_IO3	-	63N
F36	BK2_IO4	-	64P
E38	BK2_IO5	-	64N
G38	BK2_IO6	-	65P
F37	BK2_IO7	-	65N
G36	BK2_IO8	-	66P
G39	BK2_IO9	-	66N
H35	BK2_IO10	-	67P
-	GND (Bank 2)	-	-
F38	BK2_IO11	-	67N
J37	BK2_IO12	VREF2	68P
H36	BK2_IO13	-	68N
G37	BK2_IO14	-	69P
H37	BK2_IO15	-	69N
H39	BK2_IO16	-	70P
K35	BK2_IO17	-	70N
J36	BK2_IO18	-	71P

ispXPGA Logic Signal Connections: 680-Ball fpBGA (Continued)

LFX1200			
680-Ball fpBGA	**Signal Name**	**Second Function**	**LVDS Pair Polarity**
-	GND (Bank 2)	-	-
K36	BK2_IO19	-	71N
H38	BK2_IO20	-	72P
J38	BK2_IO21	-	72N
J39	BK2_IO22	-	73P
L36	BK2_IO23	-	73N
K38	BK2_IO24	-	74P
M36	BK2_IO25	-	74N
L37	BK2_IO26	-	75P
-	GND (Bank 2)	-	-
K39	BK2_IO27	-	75N
L38	BK2_IO28	-	76P
P35	BK2_IO29	-	76N
N36	BK2_IO30	-	77P
M37	BK2_IO31	-	77N
L39	BK2_IO32	-	78P
M38	BK2_IO33	-	78N
M39	BK2_IO34	-	79P
-	GND (Bank 2)	-	-
P36	BK2_IO35	-	79N
R36	BK2_IO36	-	80P
N37	BK2_IO37	-	80N
P38	BK2_IO38	-	81P
T35	BK2_IO39	-	81N
R37	BK2_IO40	-	82P
R38	BK2_IO41	-	82N
P39	BK2_IO42	-	83P
-	GND (Bank 2)	-	-
R39	BK2_IO43	-	83N
T38	BK2_IO44	-	84P
T36	BK2_IO45	-	84N
T37	BK2_IO46	-	85P
U36	BK2_IO47	-	85N
U37	BK2_IO48	-	86P
T39	BK2_IO49	-	86N
V36	BK2_IO50	-	87P
-	GND (Bank 2)	-	-
U38	BK2_IO51	-	87N
U39	BK2_IO52	-	88P
V38	BK2_IO53	-	88N
V37	BK2_IO54	-	89P
W36	BK2_IO55	-	89N
W35	BK2_IO56	-	90P

ispXPGA Logic Signal Connections: 680-Ball fpBGA (Continued)

LFX1200			
680-Ball fpBGA	**Signal Name**	**Second Function**	**LVDS Pair Polarity**
V39	BK2_IO57	-	90N
W37	BK2_IO58	-	91P
-	GND (Bank 2)	-	-
W38	BK2_IO59	-	91N
W39	BK2_IO60	-	92P
AA39	BK2_IO61	-	92N
-	GND (Bank 2)	-	-
-	GND (Bank 3)	-	-
AA38	BK3_IO0	-	93P
Y35	BK3_IO1	-	93N
AA37	BK3_IO2	-	94P
-	GND (Bank 3)	-	-
AA35	BK3_IO3	-	94N
AB39	BK3_IO4	-	95P
AB38	BK3_IO5	-	95N
AA36	BK3_IO6	-	96P
AB37	BK3_IO7	-	96N
AC39	BK3_IO8	-	97P
AC38	BK3_IO9	-	97N
AB36	BK3_IO10	-	98P
-	GND (Bank 3)	-	-
AC37	BK3_IO11	-	98N
AC36	BK3_IO12	-	99P
AD39	BK3_IO13	-	99N
AD37	BK3_IO14	-	100P
AD36	BK3_IO15	-	100N
AD35	BK3_IO16	-	101P
AE38	BK3_IO17	-	101N
AD38	BK3_IO18	-	102P
-	GND (Bank 3)	-	-
AE39	BK3_IO19	-	102N
AF38	BK3_IO20	-	103P
AF37	BK3_IO21	-	103N
AF39	BK3_IO22	-	104P
AE36	BK3_IO23	-	104N
AF36	BK3_IO24	-	105P
AG38	BK3_IO25	-	105N
AG39	BK3_IO26	-	106P
-	GND (Bank 3)	-	-
AG37	BK3_IO27	-	106N
AH37	BK3_IO28	-	107P
AH38	BK3_IO29	-	107N
AG36	BK3_IO30	-	108P

ispXPGA Logic Signal Connections: 680-Ball fpBGA (Continued)

LFX1200			
680-Ball fpBGA	**Signal Name**	**Second Function**	**LVDS Pair Polarity**
AH39	BK3_IO31	-	108N
AK39	BK3_IO32	-	109P
AK38	BK3_IO33	-	109N
AF35	BK3_IO34	-	110P
-	GND (Bank 3)	-	-
AJ37	BK3_IO35	-	110N
AH36	BK3_IO36	-	111P
AM39	BK3_IO37	-	111N
AL38	BK3_IO38	-	112P
AL39	BK3_IO39	-	112N
AJ36	BK3_IO40	-	113P
AH35	BK3_IO41	-	113N
AL37	BK3_IO42	-	114P
-	GND (Bank 3)	-	-
AN38	BK3_IO43	-	114N
AM38	BK3_IO44	-	115P
AK36	BK3_IO45	-	115N
AM37	BK3_IO46	-	116P
AN37	BK3_IO47	-	116N
AN39	BK3_IO48	-	117P
AL36	BK3_IO49	VREF3	117N
AK35	BK3_IO50	-	118P
-	GND (Bank 3)	-	-
AP39	BK3_IO51	-	118N
AM36	BK3_IO52	-	119P
AP38	BK3_IO53	-	119N
AR39	BK3_IO54	-	120P
AN36	BK3_IO55	-	120N
AM35	BK3_IO56	-	121P
AR38	BK3_IO57	-	121N
AP37	BK3_IO58	-	122P
-	GND (Bank 3)	-	-
AT39	BK3_IO59	-	122N
AR37	BK3_IO60	-	123P
AP36	BK3_IO61	-	123N
AT38	RESET	-	-
AP35	DXP	-	-
AT37	DXN	-	-
AU36	BK4_IO0	-	124P
AV36	BK4_IO1	-	124N
AR34	BK4_IO2	-	125P
-	GND (Bank 4)	-	-
AW36	BK4_IO3	-	125N

ispXPGA Logic Signal Connections: 680-Ball fpBGA (Continued)

LFX1200			
680-Ball fpBGA	**Signal Name**	**Second Function**	**LVDS Pair Polarity**
AW35	BK4_IO4	-	126P
AV35	BK4_IO5	-	126N
AV34	BK4_IO6	HSI5A_SINP	127P
AU34	BK4_IO7	HSI5A_SINN	127N
AT34	BK4_IO8	-	128P
AU35	BK4_IO9	-	128N
AT33	BK4_IO10	HSI5A_SOUTP	129P
-	GND (Bank 4)	-	-
AU33	BK4_IO11	HSI5A_SOUTN	129N
AW34	BK4_IO12	VREF4	130P
AV33	BK4_IO13	-	130N
AR32	BK4_IO14	HSI5B_SINP	131P
AT32	BK4_IO15	HSI5B_SINN	131N
AU32	BK4_IO16	-	132P
AW33	BK4_IO17	-	132N
AV32	BK4_IO18	HSI5B_SOUTP	133P
-	GND (Bank 4)	-	-
AV31	BK4_IO19	HSI5B_SOUTN	133N
AU31	BK4_IO20	-	134P
AW32	BK4_IO21	-	134N
AR30	BK4_IO22	HSI6A_SINP	135P
AT31	BK4_IO23	HSI6A_SINN	135N
AW31	BK4_IO24	-	136P
AV30	BK4_IO25	-	136N
AT30	BK4_IO26	HSI6A_SOUTP	137P
-	GND (Bank 4)	-	-
AT29	BK4_IO27	HSI6A_SOUTN	137N
AW30	BK4_IO28	-	138P
AU29	BK4_IO29	-	138N
AT28	BK4_IO30	HSI6B_SINP	139P
AU28	BK4_IO31	HSI6B_SINN	139N
AV28	BK4_IO32	-	140P
AT27	BK4_IO33	-	140N
AU27	BK4_IO34	HSI6B_SOUTP	141P
-	GND (Bank 4)	-	-
AV27	BK4_IO35	HSI6B_SOUTN	141N
AW28	BK4_IO36	-	142P
AR26	BK4_IO37	-	142N
AW27	BK4_IO38	-	143P
AT26	BK4_IO39	-	143N
AV26	BK4_IO40	-	144P
AR24	BK4_IO41	-	144N
AT25	BK4_IO42	-	145P

ispXPGA Logic Signal Connections: 680-Ball fpBGA (Continued)

LFX1200			
680-Ball fpBGA	**Signal Name**	**Second Function**	**LVDS Pair Polarity**
-	GND (Bank 4)	-	-
AW26	BK4_IO43	-	145N
AV25	BK4_IO44	-	146P
AT24	BK4_IO45	-	146N
AU24	BK4_IO46	-	147P
AU25	BK4_IO47	-	147N
AW25	BK4_IO48	PLL_RST4	148P
AW24	BK4_IO49	PLL_RST5	148N
AU23	BK4_IO50	-	149P
-	GND (Bank 4)	-	-
AT23	BK4_IO51	-	149N
AV24	BK4_IO52	-	150P
AW23	BK4_IO53	-	150N
AV23	BK4_IO54	SS_CLKIN1P	151P
AU22	BK4_IO55	SS_CLKIN1N	151N
AR21	BK4_IO56	PLL_FBK4	152P
AT22	BK4_IO57	PLL_FBK5	152N
AV22	BK4_IO58	SS_CLKOUT1P	153P
-	GND (Bank 4)	-	-
AV21	BK4_IO59	SS_CLKOUT1N	153N
AT21	BK4_IO60	CLK_OUT4	154P
AU21	BK4_IO61	CLK_OUT5	154N
-	GND (Bank 4)	-	-
AT19	GCLK4	-	LVDSCLK2
AU19	GCLK5	-	LVDSCLK2
AW22	VCCP1	-	-
AR20	GNDP1	-	-
AU18	GCLK6	-	LVDSCLK3
AT18	GCLK7	-	LVDSCLK3
-	GND (Bank 5)	-	-
AV17	BK5_IO0	CLK_OUT6	155P
AV18	BK5_IO1	CLK_OUT7	155N
AW21	BK5_IO2	PLL_FBK6	156P
-	GND (Bank 5)	-	-
AV19	BK5_IO3	PLL_FBK7	156N
AR19	BK5_IO4	-	157P
AW19	BK5_IO5	-	157N
AW18	BK5_IO6	PLL_RST6	158P
AW17	BK5_IO7	PLL_RST7	158N
AT17	BK5_IO8	-	159P
AV16	BK5_IO9	-	159N
AU17	BK5_IO10	HSI7A_SINP	160P
-	GND (Bank 5)	-	-

ispXPGA Logic Signal Connections: 680-Ball fpBGA (Continued)

LFX1200			
680-Ball fpBGA	**Signal Name**	**Second Function**	**LVDS Pair Polarity**
AT16	BK5_IO11	HSI7A_SINN	160N
AW16	BK5_IO12	-	161P
AU16	BK5_IO13	-	161N
AV14	BK5_IO14	HSI7A_SOUTP	162P
AV15	BK5_IO15	HSI7A_SOUTN	162N
AU15	BK5_IO16	-	163P
AW15	BK5_IO17	-	163N
AT15	BK5_IO18	HSI7B_SINP	164P
-	GND (Bank 5)	-	-
AR16	BK5_IO19	HSI7B_SINN	164N
AW14	BK5_IO20	-	165P
AW13	BK5_IO21	-	165N
AR14	BK5_IO22	HSI7B_SOUTP	166P
AT14	BK5_IO23	HSI7B_SOUTN	166N
AT13	BK5_IO24	-	167P
AV13	BK5_IO25	-	167N
AU12	BK5_IO26	HSI8A_SINP	168P
-	GND (Bank 5)	-	-
AU13	BK5_IO27	HSI8A_SINN	168N
AV12	BK5_IO28	-	169P
AT12	BK5_IO29	-	169N
AR12	BK5_IO30	HSI8A_SOUTP	170P
AT11	BK5_IO31	HSI8A_SOUTN	170N
AW12	BK5_IO32	-	171P
AU11	BK5_IO33	-	171N
AV9	BK5_IO34	HSI8B_SINP	172P
-	GND (Bank 5)	-	-
AV10	BK5_IO35	HSI8B_SINN	172N
AW10	BK5_IO36	-	173P
AW9	BK5_IO37	-	173N
AT10	BK5_IO38	HSI8B_SOUTP	174P
AU9	BK5_IO39	HSI8B_SOUTN	174N
AT9	BK5_IO40	-	175P
AR10	BK5_IO41	-	175N
AU8	BK5_IO42	HSI9A_SINP	176P
-	GND (Bank 5)	-	-
AV8	BK5_IO43	HSI9A_SINN	176N
AW8	BK5_IO44	-	177P
AW7	BK5_IO45	-	177N
AU7	BK5_IO46	HSI9A_SOUTP	178P
AT8	BK5_IO47	HSI9A_SOUTN	178N
AV7	BK5_IO48	-	179P
AW6	BK5_IO49	VREF5	179N

ispXPGA Logic Signal Connections: 680-Ball fpBGA (Continued)

LFX1200			
680-Ball fpBGA	**Signal Name**	**Second Function**	**LVDS Pair Polarity**
AU6	BK5_IO50	HSI9B_SINP	180P
-	GND (Bank 5)	-	-
AV6	BK5_IO51	HSI9B_SINN	180N
AR8	BK5_IO52	-	181P
AT7	BK5_IO53	-	181N
AU5	BK5_IO54	HSI9B_SOUTP	182P
AV5	BK5_IO55	HSI9B_SOUTN	182N
AW5	BK5_IO56	-	183P
AW4	BK5_IO57	-	183N
AT6	BK5_IO58	-	184P
-	GND (Bank 5)	-	-
AV4	BK5_IO59	-	184N
AR6	BK5_IO60	-	185P
AU4	BK5_IO61	-	185N
AT1	CFG0	-	-
AT3	DONE	-	-
AT2	PROGRAMb	-	-
AP4	BK6_IO0	INITb	186P
AP5	BK6_IO1	CCLK	186N
AR3	BK6_IO2	-	187P
-	GND (Bank 6)	-	-
AR2	BK6_IO3	-	187N
AP3	BK6_IO4	CSb	188P
AR1	BK6_IO5	Read	188N
AP2	BK6_IO6	-	189P
AP1	BK6_IO7	-	189N
AN4	BK6_IO8	-	190P
AM5	BK6_IO9	-	190N
AN3	BK6_IO10	-	191P
-	GND (Bank 6)	-	-
AN2	BK6_IO11	-	191N
AM4	BK6_IO12	VREF6	192P
AM3	BK6_IO13	-	192N
AN1	BK6_IO14	-	193P
AM2	BK6_IO15	-	193N
AL4	BK6_IO16	-	194P
AK5	BK6_IO17	-	194N
AM1	BK6_IO18	-	195P
-	GND (Bank 6)	-	-
AK4	BK6_IO19	-	195N
AL3	BK6_IO20	-	196P
AL2	BK6_IO21	-	196N
AL1	BK6_IO22	-	197P

ispXPGA Logic Signal Connections: 680-Ball fpBGA (Continued)

LFX1200			
680-Ball fpBGA	**Signal Name**	**Second Function**	**LVDS Pair Polarity**
AK2	BK6_IO23	-	197N
AK1	BK6_IO24	-	198P
AJ4	BK6_IO25	-	198N
AJ3	BK6_IO26	-	199P
-	GND (Bank 6)	-	-
AH4	BK6_IO27	-	199N
AH3	BK6_IO28	-	200P
AH2	BK6_IO29	-	200N
AH1	BK6_IO30	-	201P
AG4	BK6_IO31	-	201N
AF5	BK6_IO32	DATA7	202P
AG3	BK6_IO33	DATA6	202N
AG2	BK6_IO34	-	203P
-	GND (Bank 6)	-	-
AF4	BK6_IO35	-	203N
AF3	BK6_IO36	DATA5	204P
AG1	BK6_IO37	DATA4	204N
AE2	BK6_IO38	-	205P
AF1	BK6_IO39	-	205N
AF2	BK6_IO40	-	206P
AE1	BK6_IO41	-	206N
AE4	BK6_IO42	-	207P
-	GND (Bank 6)	-	-
AD4	BK6_IO43	-	207N
AD5	BK6_IO44	-	208P
AD3	BK6_IO45	-	208N
AD2	BK6_IO46	-	209P
AD1	BK6_IO47	-	209N
AC4	BK6_IO48	-	210P
AC3	BK6_IO49	-	210N
AC2	BK6_IO50	DATA3	211P
-	GND (Bank 6)	-	-
AC1	BK6_IO51	DATA2	211N
AB3	BK6_IO52	-	212P
AB4	BK6_IO53	-	212N
AB2	BK6_IO54	DATA1	213P
AB1	BK6_IO55	DATA0	213N
AA3	BK6_IO56	-	214P
AA4	BK6_IO57	-	214N
AA5	BK6_IO58	-	215P
-	GND (Bank 6)	-	-
AA2	BK6_IO59	-	215N
AA1	BK6_IO60	-	216P

ispXPGA Logic Signal Connections: 680-Ball fpBGA (Continued)

LFX1200			
680-Ball fpBGA	**Signal Name**	**Second Function**	**LVDS Pair Polarity**
Y5	BK6_IO61	-	216N
-	GND (Bank 6)	-	-
-	GND (Bank 7)	-	-
W3	BK7_IO0	-	217P
W1	BK7_IO1	-	217N
W2	BK7_IO2	-	218P
-	GND (Bank 7)	-	-
W4	BK7_IO3	-	218N
V1	BK7_IO4	-	219P
V2	BK7_IO5	-	219N
V3	BK7_IO6	-	220P
V4	BK7_IO7	-	220N
W5	BK7_IO8	-	221P
U1	BK7_IO9	-	221N
U2	BK7_IO10	-	222P
-	GND (Bank 7)	-	-
U3	BK7_IO11	-	222N
U4	BK7_IO12	-	223P
T1	BK7_IO13	-	223N
T2	BK7_IO14	-	224P
T3	BK7_IO15	-	224N
R1	BK7_IO16	-	225P
R2	BK7_IO17	-	225N
T4	BK7_IO18	-	226P
-	GND (Bank 7)	-	-
P1	BK7_IO19	-	226N
P2	BK7_IO20	-	227P
P3	BK7_IO21	-	227N
R4	BK7_IO22	-	228P
T5	BK7_IO23	-	228N
M1	BK7_IO24	-	229P
M2	BK7_IO25	-	229N
N3	BK7_IO26	-	230P
-	GND (Bank 7)	-	-
P4	BK7_IO27	-	230N
L1	BK7_IO28	-	231P
M3	BK7_IO29	-	231N
L2	BK7_IO30	-	232P
N4	BK7_IO31	-	232N
K1	BK7_IO32	-	233P
K2	BK7_IO33	-	233N
P5	BK7_IO34	-	234P
-	GND (Bank 7)	-	-

ispXPGA Logic Signal Connections: 680-Ball fpBGA (Continued)

LFX1200			
680-Ball fpBGA	**Signal Name**	**Second Function**	**LVDS Pair Polarity**
L3	BK7_IO35	-	234N
J1	BK7_IO36	-	235P
J2	BK7_IO37	-	235N
M4	BK7_IO38	-	236P
H1	BK7_IO39	-	236N
J3	BK7_IO40	-	237P
L4	BK7_IO41	-	237N
M5	BK7_IO42	-	238P
-	GND (Bank 7)	-	-
H2	BK7_IO43	-	238N
K4	BK7_IO44	-	239P
G1	BK7_IO45	-	239N
H3	BK7_IO46	-	240P
J4	BK7_IO47	VREF7	240N
K5	BK7_IO48	-	241P
G3	BK7_IO49	-	241N
H4	BK7_IO50	-	242P
-	GND (Bank 7)	-	-
F2	BK7_IO51	-	242N
G2	BK7_IO52	-	243P
H5	BK7_IO53	-	243N
F3	BK7_IO54	-	244P
F1	BK7_IO55	-	244N
G4	BK7_IO56	-	245P
E1	BK7_IO57	-	245N
F4	BK7_IO58	-	246P
-	GND (Bank 7)	-	-
E2	BK7_IO59	-	246N
F5	BK7_IO60	-	247P
E3	BK7_IO61	-	247N
D2	TDO	-	-
D3	VCCJ	-	-
D1	TDI	-	-

ispXPGA Logic Signal Connections: 900-Ball fpBGA

900 fpBGA Ball	LFX1200			LFX500		
	Signal Name	Second Function	LVDS Pair/ Polarity	Signal Name	Second Function	LVDS Pair/ Polarity
D3	BK0_IO0	-	0P	NC	-	-
E3	BK0_IO1	-	0N	NC	-	-
C2	BK0_IO2	-	1P	NC	-	-
-	GND (Bank 0)	-	-	-	-	-
C1	BK0_IO3	-	1N	NC	-	-
E4	BK0_IO4	-	2P	BK0_IO0	-	0P
F5	BK0_IO5	-	2N	BK0_IO1	-	0N
D2	BK0_IO6	HSI0A_SOUTP	3P	BK0_IO2	HSI0A_SOUTP	1P
-	-	-	-	GND (Bank 0)	-	-
D1	BK0_IO7	HSI0A_SOUTN	3N	BK0_IO3	HSI0A_SOUTN	1N
F4	BK0_IO8	-	4P	BK0_IO4	-	2P
F3	BK0_IO9	-	4N	BK0_IO5	-	2N
E2	BK0_IO10	HSI0A_SINP	5P	BK0_IO6	HSI0A_SINP	3P
-	GND (Bank 0)	-	-	-	-	-
E1	BK0_IO11	HSI0A_SINN	5N	BK0_IO7	HSI0A_SINN	3N
G6	BK0_IO12	VREF0	6P	BK0_IO9	VREF0	4N
G5	BK0_IO13	-	6N	BK0_IO8	-	4P
F1	BK0_IO14	HSI0B_SOUTP	7P	NC	-	-
F2	BK0_IO15	HSI0B_SOUTN	7N	NC	-	-
G4	BK0_IO16	-	8P	NC	-	-
G3	BK0_IO17	-	8N	NC	-	-
G2	BK0_IO18	HSI0B_SINP	9P	NC	-	-
-	GND (Bank 0)	-	-	-	-	-
G1	BK0_IO19	HSI0B_SINN	9N	NC	-	-
H3	BK0_IO20	-	10P	NC	-	-
H4	BK0_IO21	-	10N	NC	-	-
H1	BK0_IO22	HSI1A_SOUTP	11P	NC	-	-
H2	BK0_IO23	HSI1A_SOUTN	11N	NC	-	-
J7	BK0_IO24	-	12P	NC	-	-
J6	BK0_IO25	-	12N	NC	-	-
J1	BK0_IO26	HSI1A_SINP	13P	NC	-	-
-	GND (Bank 0)	-	-	-	-	-
J2	BK0_IO27	HSI1A_SINN	13N	NC	-	-
J4	BK0_IO28	-	14P	NC	-	-
J5	BK0_IO29	-	14N	NC	-	-
K1	BK0_IO30	HSI1B_SOUTP	15P	BK0_IO10	HSI0B_SOUTP	5P
-	-	-	-	GND (Bank 0)	-	-
K2	BK0_IO31	HSI1B_SOUTN	15N	BK0_IO11	HSI0B_SOUTN	5N
K5	BK0_IO32	-	16P	BK0_IO12	-	6P
K4	BK0_IO33	-	16N	BK0_IO13	-	6N
L1	BK0_IO34	HSI1B_SINP	17P	BK0_IO14	HSI0B_SINP	7P
-	GND (Bank 0)	-	-	-	-	-

ispXPGA Logic Signal Connections: 900-Ball fpBGA (Continued)

900 fpBGA Ball	LFX1200			LFX500		
	Signal Name	Second Function	LVDS Pair/ Polarity	Signal Name	Second Function	LVDS Pair/ Polarity
L2	BK0_IO35	HSI1B_SINN	17N	BK0_IO15	HSI0B_SINN	7N
L6	BK0_IO36	-	18P	BK0_IO16	-	8P
L5	BK0_IO37	-	18N	BK0_IO17	-	8N
M1	BK0_IO38	HSI2A_SOUTP	19P	BK0_IO18	HSI1A_SOUTP	9P
-	-	-	-	GND (Bank 0)	-	-
M2	BK0_IO39	HSI2A_SOUTN	19N	BK0_IO19	HSI1A_SOUTN	9N
L3	BK0_IO40	-	20P	BK0_IO20	-	10P
L4	BK0_IO41	-	20N	BK0_IO21	-	10N
M6	BK0_IO42	HSI2A_SINP	21P	BK0_IO22	HSI1A_SINP	11P
-	GND (Bank 0)	-	-	-	-	-
M5	BK0_IO43	HSI2A_SINN	21N	BK0_IO23	HSI1A_SINN	11N
M4	BK0_IO44	-	22P	BK0_IO24	-	12P
M3	BK0_IO45	-	22N	BK0_IO25	-	12N
N1	BK0_IO46	HSI2B_SOUTP	23P	BK0_IO26	HSI1B_SOUTP	13P
-	-	-	-	GND (Bank 0)	-	-
N2	BK0_IO47	HSI2B_SOUTN	23N	BK0_IO27	HSI1B_SOUTN	13N
N7	BK0_IO48	-	24P	BK0_IO28	-	14P
N6	BK0_IO49	-	24N	BK0_IO29	-	14N
P1	BK0_IO50	HSI2B_SINP	25P	BK0_IO30	HSI1B_SINP	15P
-	GND (Bank 0)	-	-	-	-	-
P2	BK0_IO51	HSI2B_SINN	25N	BK0_IO31	HSI1B_SINN	15N
N3	BK0_IO52	-	26P	BK0_IO32	-	16P
N4	BK0_IO53	-	26N	BK0_IO33	-	16N
P6	BK0_IO54	PLL_RST0	27P	BK0_IO38	PLL_RST0	19P
P5	BK0_IO55	PLL_RST1	27N	BK0_IO35	PLL_RST1	17N
P3	BK0_IO56	-	28P	BK0_IO36	-	18P
P4	BK0_IO57	-	28N	BK0_IO39	-	19N
R7	BK0_IO58	PLL_FBK0	29P	BK0_IO34	PLL_FBK0	17P
-	GND (Bank 0)	-	-	GND (Bank 0)	-	-
R6	BK0_IO59	PLL_FBK1	29N	BK0_IO37	PLL_FBK1	18N
R1	BK0_IO60	CLK_OUT0	30P	BK0_IO40	CLK_OUT0	20P
-	-	-	-	GND (Bank 0)	-	-
R2	BK0_IO61	CLK_OUT1	30N	BK0_IO41	CLK_OUT1	20N
-	GND (Bank 0)	-	-	-	-	-
R3	GCLK0	-	LVDCCLK0	GCLK0	-	LVDSCLK0
R4	GCLK1	-	LVDSCLK0	GCLK1	-	LVDSCLK0
R5	VCCP0	-	-	VCCP0	-	-
T3	GNDP0	-	-	GNDP0	-	-
T4	GCLK2	-	LVDSCLK1	GCLK2	-	LVDSCLK1
T5	GCLK3	-	LVDSCLK1	GCLK3	-	LVDSCLK1
-	GND (Bank 1)	-	-	-	-	-
T2	BK1_IO0	CLK_OUT2	31P	BK1_IO0	CLK_OUT2	21P

ispXPGA Logic Signal Connections: 900-Ball fpBGA (Continued)

900 fpBGA Ball	LFX1200			LFX500		
	Signal Name	Second Function	LVDS Pair/ Polarity	Signal Name	Second Function	LVDS Pair/ Polarity
-	-	-	-	GND (Bank 1)	-	-
T1	BK1_IO1	CLK_OUT3	31N	BK1_IO1	CLK_OUT3	21N
U2	BK1_IO2	SS_CLKOUT0P	32P	BK1_IO2	SS_CLKOUT0P	22P
-	GND (Bank 1)	-	-	-	-	-
U1	BK1_IO3	SS_CLKOUT0N	32N	BK1_IO3	SS_CLKOUT0N	22N
U3	BK1_IO4	PLL_FBK2	33P	BK1_IO4	PLL_FBK2	23P
U4	BK1_IO5	PLL_FBK3	33N	BK1_IO5	PLL_FBK3	23N
V1	BK1_IO6	SS_CLKIN0P	34P	BK1_IO10	SS_CLKIN0P	26P
V2	BK1_IO7	SS_CLKIN0N	34N	BK1_IO11	SS_CLKIN0N	26N
U5	BK1_IO8	-	35P	BK1_IO12	-	27P
U6	BK1_IO9	-	35N	BK1_IO13	-	27N
V4	BK1_IO10	-	36P	BK1_IO6	-	24P
-	GND (Bank 1)	-	-	GND (Bank 1)	-	-
V3	BK1_IO11	-	36N	BK1_IO7	-	24N
V6	BK1_IO12	PLL_RST2	37P	BK1_IO20	PLL_RST2	31P
V7	BK1_IO13	PLL_RST3	37N	BK1_IO21	PLL_RST3	31N
W1	BK1_IO14	-	38P	BK1_IO8	-	25P
W2	BK1_IO15	-	38N	BK1_IO9	-	25N
W3	BK1_IO16	-	39P	BK1_IO14	-	28P
-	-	-	-	GND (Bank 1)	-	-
W4	BK1_IO17	-	39N	BK1_IO15	-	28N
W5	BK1_IO18	-	40P	BK1_IO16	-	29P
-	GND (Bank 1)	-	-	-	-	-
W6	BK1_IO19	-	40N	BK1_IO17	-	29N
Y6	BK1_IO20	-	41P	NC	-	-
Y5	BK1_IO21	-	41N	NC	-	-
Y4	BK1_IO22	-	42P	NC	-	-
Y3	BK1_IO23	-	42N	NC	-	-
AA5	BK1_IO24	-	43P	NC	-	-
AA4	BK1_IO25	-	43N	NC	-	-
Y2	BK1_IO26	HSI3A_SOUTP	44P	BK1_IO18	HSI2A_SOUTP	30P
-	GND (Bank 1)	-	-	-	-	-
Y1	BK1_IO27	HSI3A_SOUTN	44N	BK1_IO19	HSI2A_SOUTN	30N
AB7	BK1_IO28	-	45P	NC	-	-
AB6	BK1_IO29	-	45N	NC	-	-
AA2	BK1_IO30	HSI3A_SINP	46P	BK1_IO22	HSI2A_SINP	32P
-	-	-	-	GND (Bank 1)	-	-
AA1	BK1_IO31	HSI3A_SINN	46N	BK1_IO23	HSI2A_SINN	32N
AB5	BK1_IO32	-	47P	NC	-	-
AB4	BK1_IO33	-	47N	NC	-	-
AB2	BK1_IO34	HSI3B_SOUTP	48P	NC	-	-
-	GND (Bank 1)	-	-	-	-	-

ispXPGA Logic Signal Connections: 900-Ball fpBGA (Continued)

900 fpBGA Ball	LFX1200			LFX500		
	Signal Name	Second Function	LVDS Pair/ Polarity	Signal Name	Second Function	LVDS Pair/ Polarity
AB1	BK1_IO35	HSI3B_SOUTN	48N	NC	-	-
AC6	BK1_IO36	-	49P	NC	-	-
AC5	BK1_IO37	-	49N	NC	-	-
AC2	BK1_IO38	HSI3B_SINP	50P	NC	-	-
AC1	BK1_IO39	HSI3B_SINN	50N	NC	-	-
AC4	BK1_IO40	-	51P	NC	-	-
AC3	BK1_IO41	-	51N	NC	-	-
AD2	BK1_IO42	HSI4A_SOUTP	52P	NC	-	-
-	GND (Bank 1)	-	-	-	-	-
AD1	BK1_IO43	HSI4A_SOUTN	52N	NC	-	-
AD3	BK1_IO44	-	53P	BK1_IO32	-	37P
AD4	BK1_IO45	-	53N	BK1_IO33	-	37N
AE2	BK1_IO46	HSI4A_SINP	54P	BK1_IO34	-	38P
AE1	BK1_IO47	HSI4A_SINN	54N	BK1_IO35	-	38N
AD5	BK1_IO48	-	55P	BK1_IO25	-	33N
AD6	BK1_IO49	VREF1	55N	BK1_IO24	VREF1	33P
AF2	BK1_IO50	HSI4B_SOUTP	56P	BK1_IO26	HSI2B_SOUTP	34P
-	GND (Bank 1)	-	-	-	-	-
AF1	BK1_IO51	HSI4B_SOUTN	56N	BK1_IO27	HSI2B_SOUTN	34N
AE3	BK1_IO52	-	57P	BK1_IO28	-	35P
AE4	BK1_IO53	-	57N	BK1_IO29	-	35N
AG1	BK1_IO54	HSI4B_SINP	58P	BK1_IO30	HSI2B_SINP	36P
-	-	-	-	GND (Bank 1)	-	-
AG2	BK1_IO55	HSI4B_SINN	58N	BK1_IO31	HSI2B_SINN	36N
AE5	BK1_IO56	-	59P	BK1_IO36	-	39P
AF4	BK1_IO57	-	59N	BK1_IO37	-	39N
AH1	BK1_IO58	-	60P	BK1_IO38	-	40P
-	GND (Bank 1)	-	-	GND (Bank 1)	-	-
AH2	BK1_IO59	-	60N	BK1_IO39	-	40N
AF3	BK1_IO60	-	61P	BK1_IO40	-	41P
AG3	BK1_IO61	-	61N	BK1_IO41	-	41N
AH4	TCK	-	-	TCK	-	-
AJ3	TMS	-	-	TMS	-	-
AK3	TOE	-	-	TOE	-	-
AG5	BK2_IO0	-	62P	BK2_IO0	-	42P
AH5	BK2_IO1	-	62N	BK2_IO1	-	42N
AJ4	BK2_IO2	-	63P	BK2_IO2	-	43P
-	GND (Bank 2)	-	-	GND (Bank 2)	-	-
AK4	BK2_IO3	-	63N	BK2_IO3	-	43N
AG6	BK2_IO4	-	64P	BK2_IO4	-	44P
AH6	BK2_IO5	-	64N	BK2_IO5	-	44N
AJ5	BK2_IO6	-	65P	BK2_IO6	-	45P

ispXPGA Logic Signal Connections: 900-Ball fpBGA (Continued)

900 fpBGA Ball	LFX1200			LFX500		
	Signal Name	Second Function	LVDS Pair/ Polarity	Signal Name	Second Function	LVDS Pair/ Polarity
AK5	BK2_IO7	-	65N	BK2_IO7	-	45N
AE7	BK2_IO8	-	66P	BK2_IO8	-	46P
AF7	BK2_IO9	-	66N	BK2_IO9	-	46N
AG7	BK2_IO10	-	67P	BK2_IO10	-	47P
-	GND (Bank 2)	-	-	GND (Bank 2)	-	-
AH7	BK2_IO11	-	67N	BK2_IO11	-	47N
AE8	BK2_IO12	VREF2	68P	BK2_IO21	VREF2	52N
AF8	BK2_IO13	-	68N	BK2_IO20	-	52P
AJ6	BK2_IO14	-	69P	BK2_IO12	-	48P
AK6	BK2_IO15	-	69N	BK2_IO13	-	48N
AG8	BK2_IO16	-	70P	BK2_IO14	-	49P
AH8	BK2_IO17	-	70N	BK2_IO15	-	49N
AJ7	BK2_IO18	-	71P	BK2_IO16	-	50P
-	GND (Bank 2)	-	-	-	-	-
AK7	BK2_IO19	-	71N	BK2_IO17	-	50N
AF9	BK2_IO20	-	72P	BK2_IO18	-	51P
-	-	-	-	GND (Bank 2)	-	-
AG9	BK2_IO21	-	72N	BK2_IO19	-	51N
AJ8	BK2_IO22	-	73P	NC	-	-
AK8	BK2_IO23	-	73N	NC	-	-
AD10	BK2_IO24	-	74P	NC	-	-
AE10	BK2_IO25	-	74N	NC	-	-
AJ9	BK2_IO26	-	75P	NC	-	-
-	GND (Bank 2)	-	-	-	-	-
AK9	BK2_IO27	-	75N	NC	-	-
AF10	BK2_IO28	-	76P	NC	-	-
AG10	BK2_IO29	-	76N	NC	-	-
AK10	BK2_IO30	-	77P	NC	-	-
AJ10	BK2_IO31	-	77N	NC	-	-
AE11	BK2_IO32	-	78P	NC	-	-
AF11	BK2_IO33	-	78N	NC	-	-
AG11	BK2_IO34	-	79P	NC	-	-
-	GND (Bank 2)	-	-	-	-	-
AH11	BK2_IO35	-	79N	NC	-	-
AE12	BK2_IO36	-	80P	NC	-	-
AF12	BK2_IO37	-	80N	NC	-	-
AJ11	BK2_IO38	-	81P	NC	-	-
AK11	BK2_IO39	-	81N	NC	-	-
AG12	BK2_IO40	-	82P	NC	-	-
AH12	BK2_IO41	-	82N	NC	-	-
AK12	BK2_IO42	-	83P	BK2_IO22	-	53P
-	GND (Bank 2)	-	-	-	-	-

ispXPGA Logic Signal Connections: 900-Ball fpBGA (Continued)

900 fpBGA Ball	LFX1200			LFX500		
	Signal Name	Second Function	LVDS Pair/ Polarity	Signal Name	Second Function	LVDS Pair/ Polarity
AJ12	BK2_IO43	-	83N	BK2_IO23	-	53N
AD13	BK2_IO44	-	84P	BK2_IO24	-	54P
AE13	BK2_IO45	-	84N	BK2_IO25	-	54N
AK13	BK2_IO46	-	85P	BK2_IO26	-	55P
-	-	-	-	GND (Bank 2)	-	-
AJ13	BK2_IO47	-	85N	BK2_IO27	-	55N
AG13	BK2_IO48	-	86P	BK2_IO28	-	56P
AH13	BK2_IO49	-	86N	BK2_IO29	-	56N
AE14	BK2_IO50	-	87P	BK2_IO30	-	57P
-	GND (Bank 2)	-	-	-	-	-
AF14	BK2_IO51	-	87N	BK2_IO31	-	57N
AG14	BK2_IO52	-	88P	BK2_IO32	-	58P
AH14	BK2_IO53	-	88N	BK2_IO33	-	58N
AJ14	BK2_IO54	-	89P	BK2_IO34	-	59P
-	-	-	-	GND (Bank 2)	-	-
AK14	BK2_IO55	-	89N	BK2_IO35	-	59N
AE15	BK2_IO56	-	90P	BK2_IO36	-	60P
AF15	BK2_IO57	-	90N	BK2_IO37	-	60N
AG15	BK2_IO58	-	91P	BK2_IO38	-	61P
-	GND (Bank 2)	-	-	-	-	-
AH15	BK2_IO59	-	91N	BK2_IO39	-	61N
AJ15	BK2_IO60	-	92P	BK2_IO40	-	62P
AK15	BK2_IO61	-	92N	BK2_IO41	-	62N
-	GND (Bank 2)	-	-	GND (Bank 2)	-	-
-	GND (Bank 3)	-	-	GND (Bank 3)	-	-
AK16	BK3_IO0	-	93P	BK3_IO0	-	63P
AJ16	BK3_IO1	-	93N	BK3_IO1	-	63N
AH16	BK3_IO2	-	94P	BK3_IO2	-	64P
-	GND (Bank 3)	-	-	-	-	-
AG16	BK3_IO3	-	94N	BK3_IO3	-	64N
AF16	BK3_IO4	-	95P	BK3_IO4	-	65P
AE16	BK3_IO5	-	95N	BK3_IO5	-	65N
AK17	BK3_IO6	-	96P	BK3_IO6	-	66P
-	-	-	-	GND (Bank 3)	-	-
AJ17	BK3_IO7	-	96N	BK3_IO7	-	66N
AH17	BK3_IO8	-	97P	BK3_IO8	-	67P
AG17	BK3_IO9	-	97N	BK3_IO9	-	67N
AF17	BK3_IO10	-	98P	BK3_IO10	-	68P
-	GND (Bank 3)	-	-	-	-	-
AE17	BK3_IO11	-	98N	BK3_IO11	-	68N
AH18	BK3_IO12	-	99P	BK3_IO12	-	69P
AG18	BK3_IO13	-	99N	BK3_IO13	-	69N

ispXPGA Logic Signal Connections: 900-Ball fpBGA (Continued)

900 fpBGA Ball	LFX1200			LFX500		
	Signal Name	Second Function	LVDS Pair/ Polarity	Signal Name	Second Function	LVDS Pair/ Polarity
AJ18	BK3_IO14	-	100P	BK3_IO14	-	70P
-	-	-	-	GND (Bank 3)	-	-
AK18	BK3_IO15	-	100N	BK3_IO15	-	70N
AE18	BK3_IO16	-	101P	BK3_IO16	-	71P
AD18	BK3_IO17	-	101N	BK3_IO17	-	71N
AJ19	BK3_IO18	-	102P	BK3_IO18	-	72P
-	GND (Bank 3)	-	-	-	-	-
AK19	BK3_IO19	-	102N	BK3_IO19	-	72N
AH19	BK3_IO20	-	103P	NC	-	-
AG19	BK3_IO21	-	103N	NC	-	-
AK20	BK3_IO22	-	104P	NC	-	-
AJ20	BK3_IO23	-	104N	NC	-	-
AF19	BK3_IO24	-	105P	NC	-	-
AE19	BK3_IO25	-	105N	NC	-	-
AH20	BK3_IO26	-	106P	NC	-	-
-	GND (Bank 3)	-	-	-	-	-
AG20	BK3_IO27	-	106N	NC	-	-
AF20	BK3_IO28	-	107P	NC	-	-
AE20	BK3_IO29	-	107N	NC	-	-
AJ21	BK3_IO30	-	108P	NC	-	-
AK21	BK3_IO31	-	108N	NC	-	-
AG21	BK3_IO32	-	109P	NC	-	-
AF21	BK3_IO33	-	109N	NC	-	-
AK22	BK3_IO34	-	110P	NC	-	-
-	GND (Bank 3)	-	-	-	-	-
AJ22	BK3_IO35	-	110N	NC	-	-
AE21	BK3_IO36	-	111P	NC	-	-
AD21	BK3_IO37	-	111N	NC	-	-
AG22	BK3_IO38	-	112P	NC	-	-
AF22	BK3_IO39	-	112N	NC	-	-
AG23	BK3_IO40	-	113P	BK3_IO22	-	74P
-	-	-	-	GND (Bank 3)	-	-
AH23	BK3_IO41	-	113N	BK3_IO23	-	74N
AJ23	BK3_IO42	-	114P	BK3_IO24	-	75P
-	GND (Bank 3)	-	-	-	-	-
AK23	BK3_IO43	-	114N	BK3_IO25	-	75N
AF23	BK3_IO44	-	115P	BK3_IO26	-	76P
AE23	BK3_IO45	-	115N	BK3_IO27	-	76N
AJ24	BK3_IO46	-	116P	BK3_IO28	-	77P
AK24	BK3_IO47	-	116N	BK3_IO29	-	77N
AH24	BK3_IO48	-	117P	BK3_IO21	-	73N
AG24	BK3_IO49	VREF3	117N	BK3_IO20	VREF3	73P

ispXPGA Logic Signal Connections: 900-Ball fpBGA (Continued)

900 fpBGA Ball	LFX1200			LFX500		
	Signal Name	Second Function	LVDS Pair/ Polarity	Signal Name	Second Function	LVDS Pair/ Polarity
AJ25	BK3_IO50	-	118P	BK3_IO30	-	78P
-	GND (Bank 3)	-	-	GND (Bank 3)	-	-
AK25	BK3_IO51	-	118N	BK3_IO31	-	78N
AF24	BK3_IO52	-	119P	BK3_IO32	-	79P
AE24	BK3_IO53	-	119N	BK3_IO33	-	79N
AK26	BK3_IO54	-	120P	BK3_IO34	-	80P
AJ26	BK3_IO55	-	120N	BK3_IO35	-	80N
AH25	BK3_IO56	-	121P	BK3_IO36	-	81P
AG25	BK3_IO57	-	121N	BK3_IO37	-	81N
AK27	BK3_IO58	-	122P	BK3_IO38	-	82P
-	GND (Bank 3)	-	-	GND (Bank 3)	-	-
AJ27	BK3_IO59	-	122N	BK3_IO39	-	82N
AG26	BK3_IO60	-	123P	BK3_IO40	-	83P
AH26	BK3_IO61	-	123N	BK3_IO41	-	83N
AK28	RESET	-	-	RESET	-	-
AJ28	DXP	-	-	DXP	-	-
AH27	DXN	-	-	DXN	-	-
AG28	BK4_IO0	-	124P	BK4_IO0	-	84P
AF27	BK4_IO1	-	124N	BK4_IO1	-	84N
AF28	BK4_IO2	-	125P	BK4_IO2	-	85P
-	GND (Bank 4)	-	-	GND (Bank 4)	-	-
AE26	BK4_IO3	-	125N	BK4_IO3	-	85N
AE27	BK4_IO4	-	126P	BK4_IO4	-	86P
AE28	BK4_IO5	-	126N	BK4_IO5	-	86N
AH30	BK4_IO6	HSI5A_SINP	127P	BK4_IO10	HSI3A_SINP	89P
-	-	-	-	GND (Bank 4)	-	-
AH29	BK4_IO7	HSI5A_SINN	127N	BK4_IO11	HSI3A_SINN	89N
AD25	BK4_IO8	-	128P	BK4_IO12	-	90P
AD26	BK4_IO9	-	128N	BK4_IO13	-	90N
AG29	BK4_IO10	HSI5A_SOUTP	129P	BK4_IO14	HSI3A_SOUTP	91P
-	GND (Bank 4)	-	-	-	-	-
AG30	BK4_IO11	HSI5A_SOUTN	129N	BK4_IO15	HSI3A_SOUTN	91N
AD27	BK4_IO12	VREF4	130P	BK4_IO17	VREF4	92N
AD28	BK4_IO13	-	130N	BK4_IO16	-	92P
AF29	BK4_IO14	HSI5B_SINP	131P	BK4_IO6	-	87P
AF30	BK4_IO15	HSI5B_SINN	131N	BK4_IO7	-	87N
AC25	BK4_IO16	-	132P	BK4_IO8	-	88P
AC26	BK4_IO17	-	132N	BK4_IO9	-	88N
AE29	BK4_IO18	HSI5B_SOUTP	133P	NC	-	-
-	GND (Bank 4)	-	-	-	-	-
AE30	BK4_IO19	HSI5B_SOUTN	133N	NC	-	-
AC28	BK4_IO20	-	134P	NC	-	-

ispXPGA Logic Signal Connections: 900-Ball fpBGA (Continued)

900 fpBGA Ball	LFX1200			LFX500		
	Signal Name	Second Function	LVDS Pair/ Polarity	Signal Name	Second Function	LVDS Pair/ Polarity
AC27	BK4_IO21	-	134N	NC	-	-
AD29	BK4_IO22	HSI6A_SINP	135P	NC	-	-
AD30	BK4_IO23	HSI6A_SINN	135N	NC	-	-
AB24	BK4_IO24	-	136P	NC	-	-
AB25	BK4_IO25	-	136N	NC	-	-
AC29	BK4_IO26	HSI6A_SOUTP	137P	NC	-	-
-	GND (Bank 4)	-	-	-	-	-
AC30	BK4_IO27	HSI6A_SOUTN	137N	NC	-	-
AB27	BK4_IO28	-	138P	NC	-	-
AB26	BK4_IO29	-	138N	NC	-	-
AB30	BK4_IO30	HSI6B_SINP	139P	BK4_IO18	HSI3B_SINP	93P
-	-	-	-	GND (Bank 4)	-	-
AB29	BK4_IO31	HSI6B_SINN	139N	BK4_IO19	HSI3B_SINN	93N
AA26	BK4_IO32	-	140P	NC	-	-
AA27	BK4_IO33	-	140N	NC	-	-
AA30	BK4_IO34	HSI6B_SOUTP	141P	BK4_IO22	HSI3B_SOUTP	95P
-	GND (Bank 4)	-	-	-	-	-
AA29	BK4_IO35	HSI6B_SOUTN	141N	BK4_IO23	HSI3B_SOUTN	95N
Y25	BK4_IO36	-	142P	NC	-	-
Y26	BK4_IO37	-	142N	NC	-	-
Y28	BK4_IO38	-	143P	NC	-	-
Y27	BK4_IO39	-	143N	NC	-	-
W25	BK4_IO40	-	144P	NC	-	-
W26	BK4_IO41	-	144N	NC	-	-
W27	BK4_IO42	-	145P	BK4_IO24	-	96P
-	GND (Bank 4)	-	-	-	-	-
W28	BK4_IO43	-	145N	BK4_IO25	-	96N
V24	BK4_IO44	-	146P	BK4_IO26	-	97P
-	-	-	-	GND (Bank 4)	-	-
V25	BK4_IO45	-	146N	BK4_IO27	-	97N
Y29	BK4_IO46	-	147P	BK4_IO32	-	100P
Y30	BK4_IO47	-	147N	BK4_IO33	-	100N
V27	BK4_IO48	PLL_RST4	148P	BK4_IO20	PLL_RST4	94P
V28	BK4_IO49	PLL_RST5	148N	BK4_IO21	PLL_RST5	94N
W29	BK4_IO50	-	149P	BK4_IO34	-	101P
-	GND (Bank 4)	-	-	GND (Bank 4)	-	-
W30	BK4_IO51	-	149N	BK4_IO35	-	101N
U25	BK4_IO52	-	150P	BK4_IO28	-	98P
U26	BK4_IO53	-	150N	BK4_IO29	-	98N
V29	BK4_IO54	SS_CLKIN1P	151P	BK4_IO30	SS_CLKIN1P	99P
V30	BK4_IO55	SS_CLKIN1N	151N	BK4_IO31	SS_CLKIN1N	99N
U28	BK4_IO56	PLL_FBK4	152P	BK4_IO36	PLL_FBK4	102P

ispXPGA Logic Signal Connections: 900-Ball fpBGA (Continued)

900 fpBGA Ball	LFX1200			LFX500		
	Signal Name	Second Function	LVDS Pair/ Polarity	Signal Name	Second Function	LVDS Pair/ Polarity
U27	BK4_IO57	PLL_FBK5	152N	BK4_IO37	PLL_FBK5	102N
U29	BK4_IO58	SS_CLKOUT1P	153P	BK4_IO38	SS_CLKOUT1P	103P
-	GND (Bank 4)	--	-	-	-	-
U30	BK4_IO59	SS_CLKOUT1N	153N	BK4_IO39	SS_CLKOUT1N	103N
T30	BK4_IO60	CLK_OUT4	154P	BK4_IO40	CLK_OUT4	104P
-	-	-	-	GND (Bank 4)	-	-
T29	BK4_IO61	CLK_OUT5	154N	BK4_IO41	CLK_OUT5	104N
-	GND (Bank 4)	-	-	-	-	-
T28	GCLK4	-	LVDSCLK2	GCLK4	-	LVDSCLK2
T27	GCLK5	-	LVDSCLK2	GCLK5	-	LVDSCLK2
T26	VCCP1	-	-	VCCP1	-	-
R28	GNDP1	-	-	GNDP1	-	-
R27	GCLK6	-	LVDSCLK3	GCLK6	-	LVDSCLK3
R26	GCLK7	-	LVDSCLK3	GCLK7	-	LVDSCLK3
-	GND (Bank 5)	-	-	-	-	-
R29	BK5_IO0	CLK_OUT6	155P	BK5_IO0	CLK_OUT6	105P
-	-	-	-	GND (Bank 5)	-	-
R30	BK5_IO1	CLK_OUT7	155N	BK5_IO1	CLK_OUT7	105N
P30	BK5_IO2	PLL_FBK6	156P	BK5_IO4	PLL_FBK6	107P
-	GND (Bank 5)	-	-	GND (Bank 5)	-	-
P29	BK5_IO3	PLL_FBK7	156N	BK5_IO7	PLL_FBK7	108N
P27	BK5_IO4	-	157P	BK5_IO2	-	106P
P28	BK5_IO5	-	157N	BK5_IO5	-	107N
P26	BK5_IO6	PLL_RST6	158P	BK5_IO6	PLL_RST6	108P
P25	BK5_IO7	PLL_RST7	158N	BK5_IO3	PLL_RST7	106N
N27	BK5_IO8	-	159P	BK5_IO8	-	109P
N28	BK5_IO9	-	159N	BK5_IO9	-	109N
N29	BK5_IO10	HSI7A_SINP	160P	BK5_IO10	HSI4A_SINP	110P
-	GND (Bank 5)	-	-	-	-	-
N30	BK5_IO11	HSI7A_SINN	160N	BK5_IO11	HSI4A_SINN	110N
N25	BK5_IO12	-	161P	BK5_IO12	-	111P
N24	BK5_IO13	-	161N	BK5_IO13	-	111N
M29	BK5_IO14	HSI7A_SOUTP	162P	BK5_IO14	HSI4A_SOUTP	112P
-	-	-	-	GND (Bank 5)	-	-
M30	BK5_IO15	HSI7A_SOUTN	162N	BK5_IO15	HSI4A_SOUTN	112N
M28	BK5_IO16	-	163P	BK5_IO16	-	113P
M27	BK5_IO17	-	163N	BK5_IO17	-	113N
L30	BK5_IO18	HSI7B_SINP	164P	BK5_IO18	HSI4B_SINP	114P
-	GND (Bank 5)	-	-	-	-	-
L29	BK5_IO19	HSI7B_SINN	164N	BK5_IO19	HSI4B_SINN	114N
M26	BK5_IO20	-	165P	BK5_IO20	-	115P
M25	BK5_IO21	-	165N	BK5_IO21	-	115N

ispXPGA Logic Signal Connections: 900-Ball fpBGA (Continued)

900 fpBGA Ball	LFX1200			LFX500		
	Signal Name	Second Function	LVDS Pair/ Polarity	Signal Name	Second Function	LVDS Pair/ Polarity
K30	BK5_IO22	HSI7B_SOUTP	166P	BK5_IO22	HSI4B_SOUTP	116P
-	-	-	-	GND (Bank 5)	-	-
K29	BK5_IO23	HSI7B_SOUTN	166N	BK5_IO23	HSI4B_SOUTN	116N
L28	BK5_IO24	-	167P	BK5_IO24	-	117P
L27	BK5_IO25	-	167N	BK5_IO25	-	117N
L26	BK5_IO26	HSI8A_SINP	168P	BK5_IO26	HSI5A_SINP	118P
-	GND (Bank 5)	-	-	-	-	-
L25	BK5_IO27	HSI8A_SINN	168N	BK5_IO27	HSI5A_SINN	118N
K27	BK5_IO28	-	169P	BK5_IO28	-	119P
K26	BK5_IO29	-	169N	BK5_IO29	-	119N
J30	BK5_IO30	HSI8A_SOUTP	170P	BK5_IO30	HSI5A_SOUTP	120P
-	-	-	-	GND (Bank 5)	-	-
J29	BK5_IO31	HSI8A_SOUTN	170N	BK5_IO31	HSI5A_SOUTN	120N
J26	BK5_IO32	-	171P	NC	-	-
J27	BK5_IO33	-	171N	NC	-	-
H30	BK5_IO34	HSI8B_SINP	172P	NC	-	-
-	GND (Bank 5)	-	-	-	-	-
H29	BK5_IO35	HSI8B_SINN	172N	NC	-	-
J25	BK5_IO36	-	173P	NC	-	-
J24	BK5_IO37	-	173N	NC	-	-
G30	BK5_IO38	HSI8B_SOUTP	174P	NC	-	-
G29	BK5_IO39	HSI8B_SOUTN	174N	NC	-	-
H27	BK5_IO40	-	175P	NC	-	-
H28	BK5_IO41	-	175N	NC	-	-
F30	BK5_IO42	HSI9A_SINP	176P	NC	-	-
-	GND (Bank 5)	-	-	-	-	-
F29	BK5_IO43	HSI9A_SINN	176N	NC	-	-
G27	BK5_IO44	-	177P	NC	-	-
G28	BK5_IO45	-	177N	NC	-	-
E30	BK5_IO46	HSI9A_SOUTP	178P	NC	-	-
E29	BK5_IO47	HSI9A_SOUTN	178N	NC	-	-
H26	BK5_IO48	-	179P	BK5_IO33	-	121N
H25	BK5_IO49	VREF5	179N	BK5_IO32	VREF5	121P
D30	BK5_IO50	HSI9B_SINP	180P	BK5_IO34	HSI5B_SINP	122P
-	GND (Bank 5)	-	-	-	-	-
D29	BK5_IO51	HSI9B_SINN	180N	BK5_IO35	HSI5B_SINN	122N
F28	BK5_IO52	-	181P	BK5_IO36	-	123P
F27	BK5_IO53	-	181N	BK5_IO37	-	123N
C30	BK5_IO54	HSI9B_SOUTP	182P	BK5_IO38	HSI5B_SOUTP	124P
-	-	-	-	GND (Bank 5)	-	-
C29	BK5_IO55	HSI9B_SOUTN	182N	BK5_IO39	HSI5B_SOUTN	124N
G26	BK5_IO56	-	183P	NC	-	-

ispXPGA Logic Signal Connections: 900-Ball fpBGA (Continued)

900 fpBGA Ball	LFX1200			LFX500		
	Signal Name	Second Function	LVDS Pair/ Polarity	Signal Name	Second Function	LVDS Pair/ Polarity
G25	BK5_IO57	-	183N	NC	-	-
F26	BK5_IO58	-	184P	NC	-	-
-	GND (Bank 5)	-	-	-	-	-
E28	BK5_IO59	-	184N	NC	-	-
E27	BK5_IO60	-	185P	BK5_IO40	-	125P
D28	BK5_IO61	-	185N	BK5_IO41	-	125N
C27	CFG0	-	-	CFG0	-	-
B28	DONE	-	-	DONE	-	-
A28	PROGRAMb	-	-	PROGRAMb	-	-
D26	BK6_IO0	INITb	186P	BK6_IO0	INITb	126P
C26	BK6_IO1	CCLK	186N	BK6_IO1	CCLK	126N
B27	BK6_IO2	-	187P	BK6_IO2	-	127P
-	GND (Bank 6)	-	-	GND (Bank 6)	-	-
A27	BK6_IO3	-	187N	BK6_IO3	-	127N
D25	BK6_IO4	CSb	188P	BK6_IO4	CSb	128P
C25	BK6_IO5	Read	188N	BK6_IO5	READ	128N
B26	BK6_IO6	-	189P	BK6_IO6	-	129P
A26	BK6_IO7	-	189N	BK6_IO7	-	129N
F24	BK6_IO8	-	190P	BK6_IO8	-	130P
E24	BK6_IO9	-	190N	BK6_IO9	-	130N
A25	BK6_IO10	-	191P	BK6_IO10	-	131P
-	GND (Bank 6)	-	-	GND (Bank 6)	-	-
B25	BK6_IO11	-	191N	BK6_IO11	-	131N
D24	BK6_IO12	VREF6	192P	BK6_IO21	VREF6	136N
C24	BK6_IO13	-	192N	BK6_IO20	-	136P
A24	BK6_IO14	-	193P	BK6_IO12	-	132P
B24	BK6_IO15	-	193N	BK6_IO13	-	132N
F23	BK6_IO16	-	194P	BK6_IO14	-	133P
E23	BK6_IO17	-	194N	BK6_IO15	-	133N
A23	BK6_IO18	-	195P	BK6_IO16	-	134P
-	GND (Bank 6)	-	-	-	-	-
B23	BK6_IO19	-	195N	BK6_IO17	-	134N
C23	BK6_IO20	-	196P	NC	-	-
D23	BK6_IO21	-	196N	NC	-	-
E22	BK6_IO22	-	197P	NC	-	-
D22	BK6_IO23	-	197N	NC	-	-
G21	BK6_IO24	-	198P	NC	-	-
F21	BK6_IO25	-	198N	NC	-	-
B22	BK6_IO26	-	199P	NC	-	-
-	GND (Bank 6)	-	-	-	-	-
A22	BK6_IO27	-	199N	NC	-	-
E21	BK6_IO28	-	200P	NC	-	-

ispXPGA Logic Signal Connections: 900-Ball fpBGA (Continued)

900 fpBGA Ball	LFX1200			LFX500		
	Signal Name	Second Function	LVDS Pair/ Polarity	Signal Name	Second Function	LVDS Pair/ Polarity
D21	BK6_IO29	-	200N	NC	-	-
A21	BK6_IO30	-	201P	NC	-	-
B21	BK6_IO31	-	201N	NC	-	-
F20	BK6_IO32	DATA7	202P	BK6_IO18	DATA7	135P
-	-	-	-	GND (Bank 6)	-	-
E20	BK6_IO33	DATA6	202N	BK6_IO19	DATA6	135N
D20	BK6_IO34	-	203P	NC	-	-
-	GND (Bank 6)	-	-	-	-	-
C20	BK6_IO35		203N	NC	-	-
F19	BK6_IO36	DATA5	204P	BK6_IO22	DATA5	137P
E19	BK6_IO37	DATA4	204N	BK6_IO23	DATA4	137N
B20	BK6_IO38	-	205P	NC	-	-
A20	BK6_IO39	-	205N	NC	-	-
D19	BK6_IO40	-	206P	NC	-	-
C19	BK6_IO41	-	206N	NC	-	-
A19	BK6_IO42	-	207P	NC	-	-
-	GND (Bank 6)	-	-	-	-	-
B19	BK6_IO43	-	207N	NC	-	-
G18	BK6_IO44	-	208P	BK6_IO24	-	138P
F18	BK6_IO45	-	208N	BK6_IO25	-	138N
A18	BK6_IO46	-	209P	BK6_IO32	-	142P
B18	BK6_IO47	-	209N	BK6_IO33	-	142N
D18	BK6_IO48	-	210P	BK6_IO34	-	143P
-	-	-	-	GND (Bank 6)	-	-
C18	BK6_IO49	-	210N	BK6_IO35	-	143N
F17	BK6_IO50	DATA3	211P	BK6_IO26	DATA3	139P
-	GND (Bank 6)	-	-	GND (Bank 6)	-	-
E17	BK6_IO51	DATA2	211N	BK6_IO27	DATA2	139N
D17	BK6_IO52	-	212P	BK6_IO28	-	140P
C17	BK6_IO53	-	212N	BK6_IO29	-	140N
B17	BK6_IO54	DATA1	213P	BK6_IO30	DATA1	141P
A17	BK6_IO55	DATA0	213N	BK6_IO31	DATA0	141N
F16	BK6_IO56	-	214P	BK6_IO36	-	144P
E16	BK6_IO57	-	214N	BK6_IO37	-	144N
D16	BK6_IO58	-	215P	BK6_IO38	-	145P
-	GND (Bank 6)	-	-	-	-	-
C16	BK6_IO59	-	215N	BK6_IO39	-	145N
B16	BK6_IO60	-	216P	BK6_IO40	-	146P
A16	BK6_IO61	-	216N	BK6_IO41	-	146N
-	GND (Bank 6)	-	-	GND (Bank 6)	-	-
-	GND (Bank 7)	-	-	GND (Bank 7)	-	-
A15	BK7_IO0	-	217P	BK7_IO0	-	147P

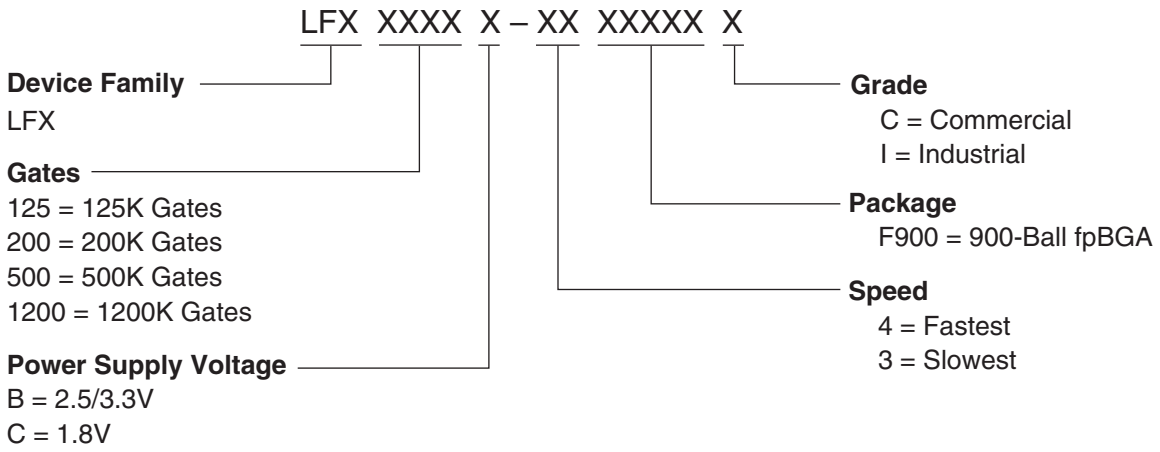
ispXPGA Logic Signal Connections: 900-Ball fpBGA (Continued)

900 fpBGA Ball	LFX1200			LFX500		
	Signal Name	Second Function	LVDS Pair/ Polarity	Signal Name	Second Function	LVDS Pair/ Polarity
B15	BK7_IO1	-	217N	BK7_IO1	-	147N
C15	BK7_IO2	-	218P	BK7_IO2	-	148P
-	GND (Bank 7)	-	-		-	-
D15	BK7_IO3	-	218N	BK7_IO3	-	148N
E15	BK7_IO4	-	219P	BK7_IO4	-	149P
F15	BK7_IO5	-	219N	BK7_IO5	-	149N
A14	BK7_IO6	-	220P	BK7_IO6	-	150P
-	-	-	-	GND (Bank 7)	-	-
B14	BK7_IO7	-	220N	BK7_IO7	-	150N
C14	BK7_IO8	-	221P	BK7_IO8	-	151P
D14	BK7_IO9	-	221N	BK7_IO9	-	151N
E14	BK7_IO10	-	222P	BK7_IO10	-	152P
-	GND (Bank 7)	-	-	-	-	-
F14	BK7_IO11	-	222N	BK7_IO11	-	152N
C13	BK7_IO12	-	223P	BK7_IO12	-	153P
D13	BK7_IO13	-	223N	BK7_IO13	-	153N
B13	BK7_IO14	-	224P	BK7_IO14	-	154P
-	-	-	-	GND (Bank 7)	-	-
A13	BK7_IO15	-	224N	BK7_IO15	-	154N
F13	BK7_IO16	-	225P	BK7_IO16	-	155P
G13	BK7_IO17	-	225N	BK7_IO17	-	155N
A12	BK7_IO18	-	226P	BK7_IO18	-	156P
-	GND (Bank 7)	-	-	-	-	-
B12	BK7_IO19	-	226N	BK7_IO19	-	156N
C12	BK7_IO20	-	227P	NC	-	-
D12	BK7_IO21	-	227N	NC	-	-
A11	BK7_IO22	-	228P	NC	-	-
B11	BK7_IO23	-	228N	NC	-	-
E12	BK7_IO24	-	229P	NC	-	-
F12	BK7_IO25	-	229N	NC	-	-
C11	BK7_IO26	-	230P	NC	-	-
-	GND (Bank 7)	-	-	-	-	-
D11	BK7_IO27	-	230N	NC	-	-
E11	BK7_IO28	-	231P	NC	-	-
F11	BK7_IO29	-	231N	NC	-	-
B10	BK7_IO30	-	232P	NC	-	-
A10	BK7_IO31	-	232N	NC	-	-
D10	BK7_IO32	-	233P	NC	-	-
E10	BK7_IO33	-	233N	NC	-	-
A9	BK7_IO34	-	234P	NC	-	-
-	GND (Bank 7)	-	-	-	-	-
B9	BK7_IO35	-	234N	NC	-	-

ispXPGA Logic Signal Connections: 900-Ball fpBGA (Continued)

900 fpBGA Ball	LFX1200			LFX500		
	Signal Name	Second Function	LVDS Pair/ Polarity	Signal Name	Second Function	LVDS Pair/ Polarity
F10	BK7_IO36	-	235P	NC	-	-
G10	BK7_IO37	-	235N	NC	-	-
A8	BK7_IO38	-	236P	NC	-	-
B8	BK7_IO39	-	236N	NC	-	-
D9	BK7_IO40	-	237P	BK7_IO22	-	158P
-	-	-	-	GND (Bank 7)	-	-
E9	BK7_IO41	-	237N	BK7_IO23	-	158N
A7	BK7_IO42	-	238P	BK7_IO24	-	159P
-	GND (Bank 7)	-	-		-	-
B7	BK7_IO43	-	238N	BK7_IO25	-	159N
C8	BK7_IO44	-	239P	BK7_IO26	-	160P
D8	BK7_IO45	-	239N	BK7_IO27	-	160N
A6	BK7_IO46	-	240P	BK7_IO21	-	157N
B6	BK7_IO47	VREF7	240N	BK7_IO20	VREF7	157P
E8	BK7_IO48	-	241P	BK7_IO28	-	161P
F8	BK7_IO49	-	241N	BK7_IO29	-	161N
C7	BK7_IO50	-	242P	BK7_IO30	-	162P
-	GND (Bank 7)	-	-	GND (Bank 7)	-	-
D7	BK7_IO51	-	242N	BK7_IO31	-	162N
E7	BK7_IO52	-	243P	BK7_IO32	-	163P
F7	BK7_IO53	-	243N	BK7_IO33	-	163N
A5	BK7_IO54	-	244P	BK7_IO34	-	164P
B5	BK7_IO55	-	244N	BK7_IO35	-	164N
C6	BK7_IO56	-	245P	BK7_IO36	-	165P
D6	BK7_IO57	-	245N	BK7_IO37	-	165N
D5	BK7_IO58	-	246P	BK7_IO38	-	166P
-	GND (Bank 7)	-	-	GND (Bank 7)	-	-
C5	BK7_IO59	-	246N	BK7_IO39	-	166N
B4	BK7_IO60	-	247P	BK7_IO40	-	167P
A4	BK7_IO61	-	247N	BK7_IO41	-	167N
A3	TDO	-	-	TDO	-	-
B3	VCCJ	-	-	VCCJ	-	-
C4	TDI	-	-	TDI	-	-

Part Number Description



Ordering Information

Commercial[1]

Part Number	Gates	Voltage	Speed Grade	Package	Balls
LFX1200B-04F900C	1200K	2.5/3.3	-4	fpBGA	900
LFX1200B-03F900C	1200K	2.5/3.3	-3	fpBGA	900
LFX1200C-04F900C	1200K	1.8	-4	fpBGA	900
LFX1200C-03F900C	1200K	1.8	-3	fpBGA	900

Industrial[1]

Part Number	Gates	Voltage	Speed Grade	Package	Balls
LFX1200B-03F900I	1200K	2.5/3.3	-3	fpBGA	900
LFX1200C-03F900I	1200K	1.8	-3	fpBGA	900

1. The ispXPGA family is dual-marked with both Commercial and Industrial grades. The Commercial speed grade is one speed grade faster (i.e. LFX1200B-04FE900C) than the Industrial speed grade (i.e. LFX1200B-03FE900I).

For Further Information

In addition to this data sheet, the following Lattice technical notes may be helpful when designing with the ispXPGA Family:

- *ispXPGA sysMEM Memory Design and Usage Guidelines* (TN1028)
- *Lattice sysCLOCK PLL Design and Usage Guidelines* (TN1003)
- *sysIO Usage Guidelines for Lattice Devices* (TN1000)
- *ispXP Configuration Usage Guidelines* (TN1026)
- *sysHSI Usage Guide* (TN1020)